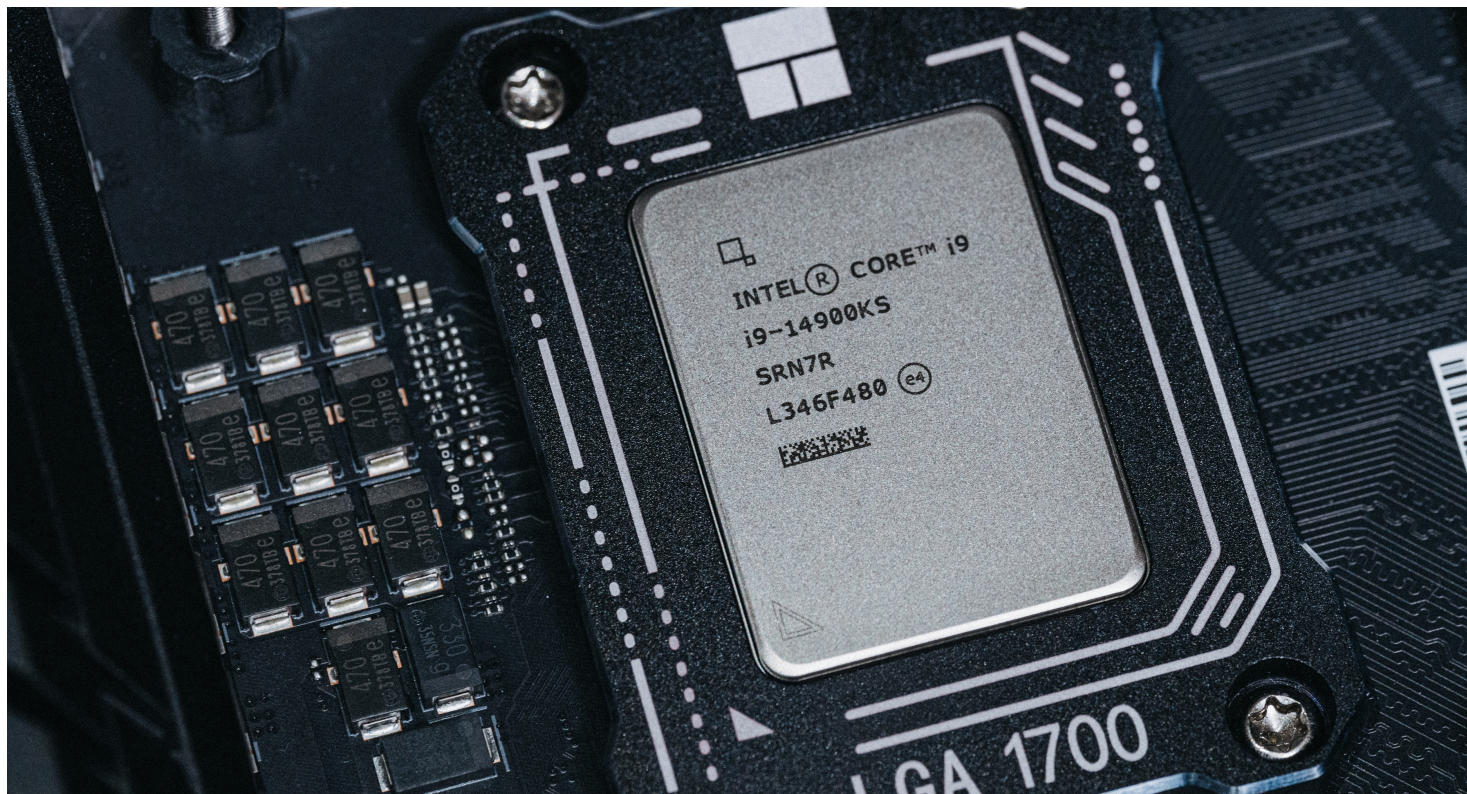




ADAPTIVE TUNING AND OPTIMIZATION OF INTEL PROCESSORS LGA1700 / LGA1851

SVID / AC-DC LOAD-LINE / LLC / CLOCKS / LIMITS / STABILITY

Using the ASUS ROG Maximus Z790 Apex Encore (BIOS 2202) and Core i9-14900KS

REV 2.00 (October 2, 2026)

ADAPTIVE CPU TUNING MANUAL

M. D. PAKHTUNOV / [T.ME/PXTNV](#) | [T.ME/PXTECH](#) | [OCN](#) | [REDDIT](#)

The author's working example. Settings require individual validation.

Z690/Z790: the working method. LGA1851/Z890: limits to applying it with DLVR.

PROJECT REVISION CHANGELOG

Content changes from Rev1.01.

2.00

October 2, 2026

Auto SVID, voltage verification and refinements to the practical method.

- **p. 16.**
Clarified the y-cruncher chapter: what the tests check, how to compare results and what to do after an error. Set the time per component to 60-120 seconds.
- **p. 25.**
Added 9.3, "Auto SVID: Limiting Turbo Ratios," with the 14900KS / Apex Encore gaming profile. P/E ratios suit the CPU and cooling; Ring and HT suit the workload and require revalidation.
- **pp. 25, 26.**
Clarified switching methods: restore SVID, automatic voltages, protections, limits and individual Turbo settings after benchmark FIXED. Auto is the SVID Behavior baseline; evaluate Trained by comparison.
- **pp. 11, 25.**
Scoped the required C1E Enabled state to the observation on Apex Encore / BIOS 2202 / ASUS Advanced OC Profile. Distinguished CPU C-states and explained checking idle power.
- **pp. 14, 26, 27.**
Added Vcore/VOUT/VID comparison and an HWiNFO example in Cinebench. Distinguished Vmin, Minimum and load voltage; explained aggregate Core VIDs and why VID need not equal VOUT.
- **pp. 15, 16.**
Clarified validation stages and criteria, attained P/E/Ring ratios and baseline variation. Added post-failure WHEA lookup; corrected the full BKT, N63 and VT3 names.
- **pp. 12, 9, 28, 29.**
Distinguished datasheet power configurations from the Intel Default Settings BIOS profile. Clarified Auto/Trained history, SKU/VBS/HVCI and glossary definitions; added HWiNFO and CoreCycler sources.

INTRODUCTION

With the release of BIOS 2202 for the Apex Encore, I revisited my system tuning with daily use in mind. I settled on adaptive SVID undervolting through IA AC Load-Line: I kept dynamic clock and voltage control while reducing the load-dependent addition to the voltage request.

The principle of the first version remains unchanged. Here I explain the combination of a selected LLC level, a matching DC Load-Line and an individually tuned AC Load-Line. The working example uses a Core i9-14900KS, an ASUS ROG Maximus Z790 Apex Encore and LLC5. Global SVID offset and fixed Vcore are not mixed into this method.

This manual explains what each setting does and how to validate the result. My profile values are not a universal preset. Even two identical processors on identical motherboards may need different settings; the BIOS version and cooling conditions matter as well.

In this revision, I distinguish confirmed profile settings, readings from the reference screenshots and the limits of simplified models. Similar VID and VOUT readings do not prove that the entire configuration is correct, and a calculated resistance does not become a measured VRM characteristic simply because it is entered in the BIOS.

Daily use requires more than heavy multithreaded testing. High clocks with few active cores, load changes, idle and repeated boots all need testing. The system must maintain performance and computational correctness under the conditions in which it will be used.

LGA1851 and Z890 are discussed here as the boundary of applicability. The workflow carries over, but the electrical behavior of Arrow Lake with DLVR requires separate tuning. An LGA1700 profile and its interpretation of external VOUT cannot be applied directly: first identify the regulated rail and the DLVR mode.

The main part covers SVID control through IA AC Load-Line. Chapter 9 discusses three alternatives: SVID offset for adaptive undervolting, FIXED with a manual VRM target, and Auto SVID with limited Turbo ratios. Save a separate profile for each method and validate it in the required workloads.

The original tests and BIOS recording are retained as material from my working example. A technical review of the text is not a new test run on the computer and does not extend the stability conditions that those tests establish.

BEFORE CHANGING SETTINGS

Tuning beyond the recommended configuration carries a risk of crashes and data corruption. Back up important files, check cooling and prepare a BIOS recovery method in advance.

00 CONTENTS

From the original method and electrical model to BIOS settings, stability testing and material from the working example.

PROJECT REVISION HISTORY

P. 2

CHANGELOG

01	METHOD AND STARTING POINT	P. 6
	Purpose, scope and conditions of the working example	
1.1	Method and Tuning Conditions	6
02	THE ELECTRICAL MODEL	P. 7-8
	Voltage requests, the physical load-line characteristic and telemetry	
2.1	SVID, AC, DC and VRM Output	7
2.2	What Can and Cannot Be Calculated	8
03	SVID AND LLC SETTINGS	P. 9-10
	BIOS settings and switching between LLC4, LLC5, LLC6 and LLC7	
3.1	Key BIOS Settings	9
3.2	LLC4, LLC5, LLC6 and LLC7	10
04	CLOCKS, LIMITS AND PROTECTION	P. 11-12
	Dynamic boost, current, power, temperature and auxiliary settings	
4.1	Clock Speeds, Turbo Boost and Power Saving	11
4.2	Power, Current, Temperature, and VRM	12
05	TUNING AND VALIDATION	P. 13-16
	Tuning, monitoring, testing and y-cruncher component stress tests	
5.1	AC Load-Line Tuning Procedure	13
5.2	Monitoring and the Reference Operating Point	14
5.3	Stability Testing and Diagnostics	15
5.4	y-cruncher: Component Stress Tests	16
06	BIOS 2202 WORKING EXAMPLE	P. 17-19
	Final settings, reference screenshots and the BIOS recording	
6.1	My Working Profile and Its Origins	17
6.2	Reference Screenshots	18
6.3	BIOS 2202 Video Recording	19
07	SOFTWARE AND LINKS	P. 20
	Official sites, downloads and guides for the tools used	
7.1	Software: Websites and Guides	20

00 CONTENTS

Limits to applying the method on other platforms, definitions, sources and alternative tuning methods.

08	LIMITS TO APPLYING THE METHOD ON LGA1851	P. 21
	What stays the same and why DLVR changes the electrical model	

8.1	LGA1851 and Z890: Scope of the Method	21
-----	---------------------------------------	----

09	ALTERNATIVE TUNING METHODS	P. 22-27
	SVID offset, FIXED and Auto SVID: control, validation and limitations	

9.1	SVID Offset Undervolting	22
-----	--------------------------	----

9.2	FIXED: Manual Voltage	23
-----	-----------------------	----

9.2.1	FIXED: Benchmark Tuning	24
-------	-------------------------	----

9.3	Auto SVID: Limiting Turbo Ratios	25
-----	----------------------------------	----

9.3.1	Auto SVID: Validation Under Load	26
-------	----------------------------------	----

9.3.2	Auto SVID: Monitoring Example	27
-------	-------------------------------	----

10	DOCUMENTATION USED	P. 28
	Primary sources, software guides and material from the working example	

10.1	Documentation Used	28
------	--------------------	----

11	GLOSSARY	P. 29-31
	English names and precise explanations of the terms	

11.1	Voltage and Power Delivery	29
------	----------------------------	----

11.2	Clocks, Limits and Protection	30
------	-------------------------------	----

11.3	Measurement and Validation	31
------	----------------------------	----

011.1 METHOD AND TUNING CONDITIONS

The method is adaptive SVID undervolting through IA AC Load-Line. Clocks remain dynamic, no global offset is set, and the external VRM is not assigned a fixed Vcore. With LLC selected, the load-dependent correction to the voltage request is reduced; DC accounts for the load-line characteristic rather than lowering voltage.

In the testing descriptions, per-core means a load on individual cores; load/idle means transitions between load and idle.

Retained	Tuned	Does not replace the method
Adaptive voltage, Turbo and power saving	LLC, applied AC/DC values, finite PL and ICCMAX limits	Global Core SVID Offset and fixed Vcore are separate methods
CEP and thermal protection	AC, based on stability and performance results	Disabling protection to pass a test is not optimization
Testing real usage scenarios	Margin from the identified stability boundary	One screenshot or benchmark does not validate every CPU operating mode

BEFORE YOU BEGIN

- Save the original BIOS profile and know how to recover from an unsuccessful configuration. Do not start with an unvalidated memory overclock.
- For a new setup, use the latest stable BIOS for the motherboard. For affected Raptor Lake processors, Intel recommends microcode 0x12F or later; verify the actual version after boot.
- First test the system with the Intel settings recommended for that CPU. ASUS Advanced OC Profile in my example is not the same as Intel Default Settings.
- Set power, current and temperature limits appropriate for the cooling. Choose repeatable workloads and record both errors and test results.

WHAT THE EVIDENCE ESTABLISHES

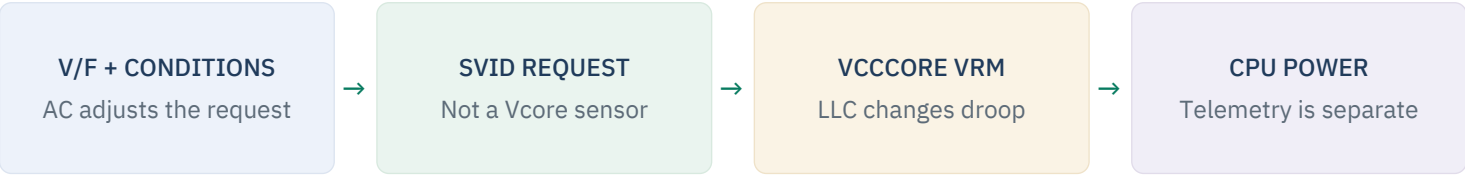
My profile values establish only its configuration. The screenshots establish the runs and sensor readings shown. They are not measurements of the physical VRM load-line characteristic, transient overshoot or CPU lifespan.

WORKING EXAMPLE

Core i9-14900KS, 8P+16E, Hyper-Threading Disabled, 24 threads; Apex Encore, BIOS 2202, LLC5. HT is disabled in my profile, but this is not a required part of the method. Revalidate stability after changing HT, clocks, LLC, BIOS or limits.

02 2.1 SVID, AC, DC AND VRM OUTPUT

Keep three levels distinct: the processor generates a request, the VRM physically powers the CPU, and monitoring shows the available telemetry. Using the same units does not make these quantities interchangeable.



Element	Role in This Method
V/F and SVID	V/F provides the basis for the relationship between frequency and voltage; SVID carries commands and data between the CPU and VRM. Other conditions also affect the operating request.
IA AC Load Line	A parameter for load-dependent adjustment of the request. Reducing it is used here for undervolting; it is not a fixed offset to the entire V/F curve.
CPU LLC	Changes the load-line characteristic of the VCCCORE VRM. Stronger compensation usually reduces steady-state droop, but changes transient response.
IA DC Load Line	A parameter in the load-dependent droop model used by the processor for voltage and power accounting. It is not an IOUT adjustment or a separate undervolt.
Core VID	VID reported by the CPU. Not a physical Vcore measurement, and not necessarily a raw command that can be inserted directly into a VRM calculation.
VOUT / Vcore	VOUT is a voltage reading from VRM telemetry; Vcore Die Sense is a separate motherboard measurement channel. Their agreement must be checked on the specific system.
CEP	This protection responds to droop relative to an internal threshold and may limit the load. An absence of errors does not rule out performance loss caused by its intervention.

THE KEY DISTINCTION

AC changes the voltage request; LLC changes the physical behavior of the VRM; DC participates in the power-accounting model. Adjusting DC to reach a desired Package Power reading or to make VID equal VOUT does not prove that the configuration is correct.

DOCUMENTATION CONSULTED: Intel specifications and explanations; explanations by the HWiNFO author; ASUS BIOS guides and information.

Intel VCCCORE, Intel CEP, HWiNFO: VID and DC Load-line, ASUS ROG Z790 BIOS Manual

02 2.2 WHAT CAN AND CANNOT BE CALCULATED

STEADY-STATE OPERATION

SIMPLIFIED MODEL OF THE EXTERNAL RAIL

$V_{OUT} \approx V_{SVID_command} - I_{OUT} \times R_{VRM}$

This illustrates load-dependent droop with an unchanged VRM command. It does not describe the complete SVID request algorithm, boost dynamics or transient response.

With adaptive control, the command itself changes with frequency, temperature and load. Dividing the voltage difference between idle and a stress test by the current difference, without controlling the request, therefore does not isolate the load-line resistance.

Quantity	What Is Actually Known	What It Does Not Establish
DC = 0.73 mΩ	The DC value adopted for LLC5 from Table 3.2; also used in my profile	A table value does not replace a measurement of transient response
IOUT = 244 A	This Current reading is present in the screenshot	It does not establish equality with the internal current estimate used for AC compensation
Core VID ≈ VOUT	Readings are close in one operating condition	No proof of exact DC calibration or an absence of overshoot
HWiNFO AC/DC	Readback of programmable parameters, when available	Not a direct hardware measurement of power-rail resistance

WHY THE CALCULATED 93 MV IS NOT A MEASURED UNDERVOLT

The arithmetic $244\text{ A} \times (0.73 - 0.35)\text{ m}\Omega = 92.72\text{ mV}$ is correct. However, it describes a conditional case in which the current used for AC compensation is assumed to be 244 A and all other conditions are equal. These assumptions cannot be verified from the screenshot. The number is therefore not used to calculate ready-made AC presets or to promise identical VOUT at different LLC levels.

HANDLING DC IN PRACTICE

- Select LLC and set the corresponding DC from Table 3.2. After boot, check the AC/DC values actually applied; Auto for DC is acceptable if readback shows the required table value.
- After changing LLC, replace DC with the value for the new level and retune AC. Keep DC fixed when tuning AC or SVID offset: it is not an additional undervolting control.
- Do not change CPU Current Reporting to hide power consumption. An incorrect DC model may indirectly change clocks through PL enforcement.
- Measuring the physical load-line and fast overshoot requires suitable equipment. A software log helps check behavior, but does not replace that measurement.

DOCUMENTATION CONSULTED: Intel specifications and explanations; explanations by the HWiNFO author.

Intel VCCCORE, HWiNFO: VID and DC Load-line, HWiNFO: Effective Clock

033.1 KEY BIOS SETTINGS

These names are from ASUS Z790 BIOS. The values belong to the example discussed here; the explanations distinguish the tuning principle from details of the historical export. Submenu paths may change between BIOS revisions.

BIOS setting	Example / manual	Purpose and caveat
SVID Behavior	Auto	The manual uses Auto following my later clarification. This ASUS policy depends on the BIOS; when AC/DC are set manually, verify the applied values.
CPU SVID Support	Enabled	Keeps SVID control and communication active.
Actual VRM Core Voltage	Auto	Does not set a fixed Manual/Override target for the external Vcore VRM.
Global Core SVID Voltage	Auto	No global offset is specified. This does not mean that the entire platform uses Intel Defaults.
Cache SVID Voltage	Auto	Applies no manual adjustment to the Ring/Cache voltage request.
CPU Load-line Calibration	Level 5	LLC for the VCCCORE rail. After changing the level, set DC using Table 3.2 and repeat AC tuning.
Synch ACDC Loadline with VRM Loadline	Disabled	Automatic matching is disabled; still verify the selected AC/DC values after boot.
IA AC Load Line	0.35 mΩ	The value in my working profile, not a universal starting point.
IA DC Load Line	0.73 mΩ	The DC value adopted for LLC5 from Table 3.2; verify that it is applied after boot.
IA VR Voltage Limit	Auto	No separate limit is set in this example. This limit neither measures nor rules out fast overshoot; it does not replace light-load testing.
Voltage Monitor	Die Sense	Voltage sensing at the CPU. On this board, Vcore is compared with VOUT; other boards must be checked separately.
UnderVolt Protection	Disabled in the export	Not a required part of AC undervolting. For a new baseline, Enabled is preferable, with verification that the BIOS settings take effect.

UVP AND BIOS UNDERVOLTING ARE DIFFERENT

ASUS describes Enabled as allowing BIOS undervolting while protecting against runtime undervolting. The method does not require disabling UVP, VBS (Virtualization-Based Security) or HVCI (Hypervisor-Protected Code Integrity). Disabled in the export is a historical setting, not a general instruction.

The TXT dated August 28, 2026 records SVID Behavior = Trained. The recommendation later changed to Auto; no new hardware run followed. The TXT and video document the earlier profile.

03 3.2 LLC4, LLC5, LLC6 AND LLC7

For ASUS motherboards with an IA DC Load Line setting, this method adopts the LLC/DC mapping in the table below. Applying it to all such ASUS boards is an assumption of the method, not a proven characteristic of every model. These numbers do not automatically determine AC.

LLC	DC, mΩ	Practical Behavior	What to Do with AC
Level 4	1.00	More droop than LLC5; different behavior during load transitions	Retune AC. Do not carry over the minimum AC from another level.
Level 5	0.73	The level used in my main working example	My profile uses AC 0.35 mΩ. This is an individual result, not a general AC preset.
Level 6	0.49	Less steady-state droop; different transient response	Repeat AC tuning. A lower AC number does not guarantee better efficiency or stability.
Level 7	0.24	Even stronger droop compensation; not a target simply to obtain flat Vcore	Do not treat it as equivalent to LLC5. At the lowest available AC, do not add another undervolt without separately validating the baseline.

SWITCHING TO ANOTHER LEVEL

1. SAVE THE STARTING POINT

Record LLC, AC/DC, voltage settings, limits and the result of the same workload.

2. SELECT LLC AND SET DC

For LLC4/5/6/7, set DC to 1.00/0.73/0.49/0.24 mΩ, respectively. Disable Synch ACDC for independent AC control; verify after boot that the values have taken effect.

3. START FROM A REPRODUCIBLE BASELINE

Do not start immediately at the previous minimum AC. AC = DC can serve as a reference configuration, but does not guarantee correct voltage or an absence of overcompensation.

4. REPEAT TUNING AND TESTING

Compare voltage, power and the result, then test heavy, light and varying loads. Changing LLC changes more than a single steady-state VOUT number.

NO UNIVERSAL DIVISOR

AC is not calculated by dividing the LLC number or the table DC value by 1.5 or 2. DC sets the adopted model baseline; AC is tuned for stability and results. Other manufacturers may number their LLC levels differently.

04 4.1 CLOCK SPEEDS, TURBO BOOST AND POWER SAVING

In my example, ratios are not fixed manually. This preserves dynamic operation, but Auto with ASUS Advanced OC Profile, ABT, and manual limits cannot be described as a fully stock Intel configuration. Here, boost means an automatic frequency increase; all-core means a load on all cores.

BIOS setting	Value	Practical meaning
Performance Core Ratio	Auto	No manual P-core ratios; the upper bins are determined by the CPU and the active BIOS policy.
Efficient Core Ratio	Auto	No manually assigned E-core ratios.
Min. / Max. CPU Cache Ratio	Auto / Auto	Ring/Cache operates dynamically, rather than continuously at its maximum x50.
Ring Down Bin	Enabled	Allows Ring to downclock under the relevant conditions.
Intel Adaptive Boost Technology	Enabled	Additional multithreaded boost when headroom is available. This is not the same as the two-core maximum of x62.
Turbo Boost Max Technology 3.0	Enabled	Uses preferred P-cores for high clock speeds with a small number of threads.
TVB Voltage Optimizations	Enabled	Temperature-dependent optimization of the voltage request; not a manual ratio.
Enhanced TVB	Enabled	The temperature conditions for boost remain active.
Overclocking TVB	Auto	No separate manual TVB table in this profile.
AVX2 / Ratio Offset / Guardband	Enabled / Auto / Auto	AVX2 is enabled; the ratio reduction (Ratio Offset) and voltage margin (Guardband) were not changed manually.
SpeedStep / Speed Shift	Enabled / Enabled	Dynamic control of operating states is retained.
Enhanced C-states / CPU C-states	Enabled / Auto	C1E locked Enabled on the author's Apex Encore / BIOS 2202 / Advanced OC Profile; CPU C-states is separate (9.3).
Hyper-Threading	Disabled	This is how my CPU is configured: 24 threads. The method does not require disabling HT.

TEST MAXIMUM CLOCK SPEEDS SEPARATELY FROM HEAVY ALL-CORE LOADS

Under the heavy load shown in the screenshot, the P-cores run at approximately x56-x57 and the E-cores at x43. The recorded maxima of x62/x45/x50 occurred at other times. Stability under a heavy load does not automatically validate the upper P-core bins.

If an error occurs only at high boost on one or two P-cores, first separate that operating mode from all-core operation. Limiting ratios and adjusting V/F are separate actions; do not mask the problem by changing DC or disable ABT as a universal way to eliminate x62.

DOCUMENTATION CONSULTED: ASUS BIOS guides and information; Intel specifications and explanations.

04 4.2 POWER, CURRENT, TEMPERATURE, AND VRM

BIOS setting	In my profile	Meaning
ASUS MultiCore Enhancement	Disabled - Enforce All limits	Enforces the specified limits. Manually setting 320 W still does not make them Intel Defaults.
Long / Short Duration Package Power Limit	320 / 320 W	PL1/PL2 limit power; a limit does not specify required power consumption.
Package Power Time Window	56 s	A power-averaging parameter. With equal PL1/PL2, there is no specified transition from 320 → 253 W after 56 seconds.
CPU Core/Cache Current Limit Max.	400 A	CPU ICCMAX; not equivalent to the slowly polled IOUT Maximum.
Unlimited ICCMAX	Disabled	The specified ICCMAX current limit remains active.
Dual Tau Boost	Disabled	The separate Tau policy is not used in this example; this does not disable the current limit.
IA CEP / SA CEP	Enabled / Enabled	Protections for the respective domains are retained.
Maximum CPU Core Temperature / Thermal Monitor	100 °C / Enabled	100 °C is the ceiling in this example, not a target temperature for daily operation.
CPU Current Reporting	100%	Do not distort reported current to bypass power control.
Switch Microcode	Current Microcode	Uses the current BIOS microcode branch, not an older version to bypass restrictions.

POWER CONFIGURATIONS IN THE INTEL DATASHEET

Processors	Datasheet configuration	PL1 / PL2	Tau	ICCMAX
13600K/KF, 14600K/KF	Standard, 125-W SKU	125 / 181 W	56 s	200 A
13700K/KF, 14700K/KF	Standard, 125-W SKU	125 / 253 W	56 s	307 A
13900K/KF, 14900K/KF	Standard, 125-W SKU	125 / 253 W	56 s	307 A
13900K/KF, 14900K/KF	Extreme Config	253 / 253 W	56 s	400 A
13900KS, 14900KS	Standard, 150-W SKU	253 / 253 W	56 s	307 A
13900KS, 14900KS	Extreme Config	320 / 320 W	56 s	400 A

These are datasheet power configurations; the full Intel Default Settings BIOS profile includes other parameters. SKU identifies a specific CPU model. My example uses the 14900KS Extreme configuration, but lower limits may suit the cooling and workload. For another SKU, use its documented limits.

SECONDARY SETTINGS FOR MY VRM

Setting	Value	Role in the method
CPU Current Capability	100%	An external VRM setting, not a replacement for CPU ICCMAX
Switching Frequency / Duty / Phase	500 kHz / Extreme / Optimized	Settings from the example, not required improvements for AC undervolting
CPU Power Thermal Control	125 °C	A VRM protection threshold, not an operating temperature target
CPU Input Voltage LLC	Level 2	A separate CPU Input rail; not CPU VCCCORE LLC. It is not tuned for IA AC LL

LIMITS DO NOT GUARANTEE SERVICE LIFE

Keeping protections enabled does not make every undervolt stock or unconditionally safe. Monitor voltage, temperature, and performance in all required operating modes. The IOUT Maximum of 259 A in the screenshot does not prove there is margin below ICCMAX 400 A during fast transients.

DOCUMENTATION CONSULTED: Intel specifications and explanations; ASUS BIOS guides and information.

Intel Datasheet, Intel VCCCORE, ASUS ROG Z790 BIOS Manual, Intel Vmin Update

05 5.1 AC LOAD-LINE TUNING PROCEDURE

Change one significant parameter at a time. First establish a reproducible baseline, then find a stable AC value while keeping LLC, DC, frequency policy, and limits unchanged. Memory must already be validated; otherwise, errors cannot be confidently linked to the latest CPU change.

The goal of AC undervolting is the lowest reasonable AC, not the absolute minimum or an undervolt pushed to the floor: balance lower voltage, power consumption, and temperature with full baseline performance, correct computation, and no unwanted CEP intervention. An excessively low AC may produce no WHEA events, BSODs, or crashes, yet CEP may already be reducing Effective Clocks through clock stretching and reducing performance. The absence of WHEA does not prove that the undervolt is optimal.

1. RECORD THE BASELINE

Save the profile, BIOS/microcode version, HT, memory settings, limits, temperatures, and results of the selected tests. For a new system, first validate the recommended Intel configuration.

2. CHOOSE OPERATING LIMITS

PL1/PL2, ICCMAX, and the temperature ceiling must suit the cooling. Do not change them while tuning AC.

3. CHOOSE A MODERATE LLC

In my example, this is Level 5. The matching DC values for ASUS are given in 3.2; the entire profile does not transfer automatically. Do not chase minimum Vdroop just for a good-looking graph.

4. SEPARATE AC AND DC

For manual tuning, disable Synch ACDC. Set DC using Table 3.2 and verify AC/DC after boot. Do not use DC to lower reported power.

5. VALIDATE THE INITIAL AC

In this method, after selecting LLC and verifying the applied DC value, setting AC = DC is recommended as a reproducible starting point, not a universal optimum or a value guaranteed to be minimal, safe, or a target. Before lowering AC, validate and record the baseline: test result, Effective Clocks, VOUT/voltage, and the absence of computational errors and signs of CEP intervention. Then lower only AC; DC remains tied to LLC.

6. LOWER AC AND COMPARE RESULTS

Lower **the AC value itself** by 0.02-0.05 mΩ per iteration. If errors or reproducible performance loss appear, return to the previous validated value and refine the boundary with smaller steps of 0.01-0.02 mΩ. **These numbers are step sizes, not target AC values.** Check errors, WHEA, the test result, and Effective Clocks.

In the original example, AC started at 0.40 mΩ and was then reduced to 0.35-0.30 mΩ. These values illustrate one specific configuration; they do not define a mandatory starting point or a universal lower boundary.

7. SEPARATE THE LOAD TYPES

Test heavy multithreaded operation separately from single-threaded or lightly threaded high boost and load/idle transitions. Lowering AC does not guarantee a solution to a problem at the upper V/F point.

8. BACK AWAY FROM THE BOUNDARY AND REPEAT

If an error or performance loss occurs, undo the last step. Keep the final AC above the boundary you found, with a margin confirmed by repeated testing in warm conditions.

OPTIMIZATION CRITERION

Voltage, power, or temperature has decreased with comparable performance in the same scenario, with no new errors or hidden performance loss. When limited by PL, the benefit may appear as higher clock speeds rather than lower power consumption.

WHEN TO RETURN TO THE STARTING POINT

If errors persist after reverting AC or appear in a different operating mode, separately check the CPU, Ring, IMC/memory, and baseline stability. Raising AC is not a universal fix for every y-cruncher error.

05

5.2 MONITORING AND THE REFERENCE OPERATING POINT

Sensor / metric	How to use it
Core VIDs	The collapsed row averages core VIDs, not their maximum or measured Vcore. Expand the group; compare the same interval (9.3.1).
VRM Vcore Voltage (VOUT)	Assess the output voltage of the corresponding VRM when a reliable telemetry channel is available.
Vcore / Die Sense	Compare with VOUT on this board. Account separately for differences in measurement points, accuracy, and polling.
VRM Vcore Current (IOUT)	Assess rail current and its relationship to the load. Slow sampling does not capture every fast peak.
CPU Package / IA Power	Monitor the effect of PL and the consistency of the model. Package power and a single VRM rail do not have to match to the watt.
Core Effective Clocks	Averaged clock speed accounting for core activity and sleep. Compare with the test result under a sustained, comparable load.
Limit Reasons / WHEA	Limit reasons and hardware errors. The absence of WHEA does not rule out CEP activation or a computational error.
CPU / VRM temperatures	Record current and maximum values, cooling conditions, and throttling flags.

Y-CRUNCHER SCREENSHOT: DISTINGUISH CURRENT FROM MAXIMUM

Metric	Current in the screenshot	Maximum over the interval
Core VIDs (aggregate)	1.278 V	1.472 V
Vcore / VRM VOUT	1.288 / 1.288 V	1.430 / 1.409 V
VRM IOUT	244 A	259 A
CPU Package Power	313.696 W	318.643 W
Core Max	75 °C	94 °C (summer)
VR VCC Temperature	53 °C	54 °C

1.288 V × 244 A ≈ 314.3 W is close to the current Package reading of 313.7 W, but does not prove DC calibration. These are different channels, and their sampling is not guaranteed to be synchronized in hardware. Maxima in different rows may have occurred at different times.

WHAT SOFTWARE MONITORING CANNOT SHOW

A software voltage maximum does not rule out fast overshoot. A gap between Core Clock and Effective Clock at idle is normal and does not, by itself, prove CEP intervention. On the system shown, SVID POUT reaches 255 W and stops reflecting further increases; this channel cannot be used as the sole power measurement.

DOCUMENTATION CONSULTED: explanations by the HWiNFO author; Intel specifications and explanations; material from the working example.

HWiNFO: VID and DC Load-line, HWiNFO: Effective Clock, Intel VCCCORE, Author's Screenshots

05

5.3 STABILITY TESTING AND DIAGNOSTICS

Time alone does not guarantee stability. Record the actual P/E/Ring, workload and limit reasons: passing under limits does not validate the upper ratios. Compare small gains with variation across several baseline runs.

Test scenario	What to check	Condition for proceeding
5-10 min after an AC step	Reproducible load and result, errors, and temperatures	No new errors or unexplained performance loss
y-cruncher SVT + VT3	20-30 min: quick screening; 45-60 min: candidate; then longer tests of the required modes	Both tests complete without errors; limit flags are understood
OCCT / changing loads	Variable data sets and core cycling; separately, reproducible load/idle transitions	No errors, reboots, or performance loss
Per-core / small thread counts	Every P-core, including preferred cores; upper clock speeds under suitable conditions	No errors at clock speeds actually reachable in this mode
Idle, sleep/wake, cold boot	Power-state transitions and repeatable startup behavior	No hangs, occasional app crashes, or new WHEA events
Real workloads and a warm room	Combined load, noise, heat, and expected performance	The profile meets the stated daily-use scenario

QUICK DIAGNOSTICS

Observation	Do not jump to conclusions	Next step
SVT / VT3 error	This is not a definitive test of the cores alone: Ring, IMC, DRAM, and power delivery may be involved	With validated memory unchanged, undo the last AC step and repeat
Error only at high boost	Heavy all-core testing did not validate this mode	Check the specific cores and bins; do not use DC as a fix
Low Effective Clock	This is normal at idle; under load, it can have different causes	Compare the result, core activity, and limit reasons
Failure when the load is removed	Software has not proven that overshoot was the cause	Repeat transitions and restore the baseline; after changing LLC, recheck AC/DC
Unexpected change in Package Power	The DC model, limits, or a different frequency mode may be involved	Check the applied settings and repeat the same load

TESTS COMPLEMENT ONE ANOTHER

Cinebench does not replace other tests; OCCT Variable is not a full load/idle cycle. After a failure, open Event Viewer → Windows Logs → System, filter WHEA-Logger for the run interval and save event details. Examine the source and error type: WHEA does not automatically identify CPU cores as the cause.

FOR MORE DEMANDING SCENARIOS: BKT, BBP, AND SFTV4

Add BKT, BBP and SFTv4 one at a time. BKT broadens arithmetic coverage; SFTv4 is an in-cache FFT with a focus similar to OCCT CPU. BBP/SFTv4 may be harder than VT3 on this CPU; monitor current and heat. Provide CPU cooling and VRM airflow. If overheating occurs, stop and reconsider limits while retaining protections.

LOWER VOUT DOES NOT MEAN LESS VDROOP

At higher current with the same LLC, VOUT may fall: with an unchanged request, droop increases. Adaptive SVID also changes the CPU request. Do not strengthen LLC just for a voltage number; compare current, clocks, temperatures and results. Components and sequence: 5.4.

DOCUMENTATION CONSULTED: software and Windows documentation; explanations by the HWiNFO author.

y-cruncher Version History, OCCT CPU, OCCT CPU + RAM, HWiNFO: Effective Clock, Microsoft WHEA

05 5.4 Y-CRUNCHER: COMPONENT STRESS TESTS

Use Component Stress Tester, not the π benchmark. The screenshot shows the Windows 0.8.7.9547b menu, not a new CPU test. I record the version, binary, threads and memory: the instruction set depends on the binary; AVX2 describes this run. Mem/Thread is memory per thread and varies by component.

```
C:\Users\pntn\Desktop\y-cruncher v0.8.7.9547b\y-cruncher v0.8.7.9547b\y-cruncher...
Component Stress Tester

1 Logical Cores:      24
2 Memory:            30.4 GiB ( 1.27 GiB per thread )
3 NUMA Mode:         Local - Memory allocated from local thread.
4/5 Time Limit:      120 seconds per test / Run Forever
6 Stop on Error:      Enabled

7/8 Enable All Tests / Disable All Tests
9/10 Load/Save Configuration File

# Tag Test Name Mem/Thread Component CPU-----Mem
11 BKT Basecase + Karatsuba 27.8 KiB Scalar Integer -|-----
12 BBP BBP Digit Extraction small AVX2 Float |-----
13 SFTv4 Small In-Cache FFTv4 229 KiB AVX2 Float -|-----
14 SNT Small In-Cache N63 21.3 MiB AVX2 Integer --|-----
15 SVT Small In-Cache VT3 10.3 MiB AVX2 Float --|-----
16 FFTv4 Fast Fourier Transform (v4) 246 MiB AVX2 Float -----|
17 N63 Classic NTT (v2) 1.27 GiB AVX2 Integer ---|-----
18 VT3 Vector Transform (v3) 1.23 GiB AVX2 Float ----|-----

0 Start Stress-Testing!

option:
```

A PRACTICAL STARTING POINT

- Logical Cores: the thread count of the profile being tested; here, HT Disabled, 24.
- Memory: for large tests, 80-90% of free RAM, leaving room for the OS, without paging.
- NUMA: Local for the standard configuration in this example.
- Time Limit: 60-120 s per component, not for the entire session.
- Stop on Error: Enabled.

First select the required components; then choose 0 - Start Stress-Testing.

WHAT EACH COMPONENT DOES

Tag	Algorithm	Primary load	Role in CPU undervolting
BKT	Basecase + Karatsuba*	Scalar integer multiplication; small working set	Additional arithmetic coverage for the CPU
BBP	BBP Digit Extraction	Vector floating-point arithmetic, small working set	CPU computation; not a check of all allocated RAM
SFTv4	Small In-Cache FFTv4	Floating-point arithmetic; an in-cache fast Fourier transform (FFT)	CPU/cache and cooling; similar in focus to OCCT CPU
SNT	Small In-Cache N63	An in-cache integer number-theoretic transform (NTT)	Tests CPU/cache with a different type of math
SVT	Small In-Cache VT3	Small VT3: in-cache vector computation	Checks CPU/cache alongside the large VT3 test
FFTv4	Fast Fourier Transform v4	FFT with a large working set; dependent on RAM bandwidth	Mixed CPU/cache/IMC/RAM load
N63	Classic 64-bit NTT v2	64-bit integer NTT; large working set	An independent combined CPU and RAM load
VT3	Vector-Scalable Transform v3	Vector transform; large working set, CPU + IMC + RAM	Tests the profile under a mixed load; replacement for legacy VST

* The BKT name in Command Lines.txt includes Toom-Cook; the developer states that Toom-3 was removed.

HOW I COMPARE THE RESULTS

SVT is the small, in-cache VT3; VT3 succeeds VST. If SVT passes but VT3 fails, I check the whole profile with a large working set: CPU/cache, Ring, IMC, RAM and power delivery. This is a clue, not a RAM diagnosis; both tests failing does not locate the cause either. With validated memory unchanged, I undo the last change to the CPU profile, repeat the check and add an independent RAM test. FFTv4 exercises the CPU and memory together, not just DIMMs.

TEST DURATION AND SCOPE

SVT + VT3: 20-30 minutes for screening; 45-60 for a candidate; up to 60-90 if needed for a thermal plateau. These are practical stages, not a standard: a plateau alone does not prove stability. Add varied loads and repeat starts rather than an endless run. I start BKT/BBP/SFTv4 briefly and monitor heat. Also check per-core boost, load/idle and real workloads (5.3).

DOCUMENTATION CONSULTED: software and Windows documentation.

y-cruncher: Official Release, y-cruncher Version History, y-cruncher FAQ, y-cruncher: Memory Allocation

06 6.1 MY WORKING PROFILE AND ITS ORIGINS

The settings below belong to a previously tuned CPU, not a proposed preset for every CPU. I retain the numbers from the first guide, while distinguishing the historical export from later clarifications in the manual.

Setting	Value	Status / meaning
CPU / motherboard	14900KS / Apex Encore	BIOS 2202; ASUS Advanced OC Profile
P / E / Ring Ratio	Auto / Auto / Auto	Not fixed all-core clock speeds
Hyper-Threading	Disabled	8P+16E, 24 threads; a fact about this example
SVID Behavior	Auto in the manual	Archived TXT: Trained; the later clarification is not a new measurement
CPU LLC	Level 5	Selected VCCCORE VRM level
IA AC / DC Load Line	0.35 / 0.73 mΩ	AC is my result; DC is the table value for LLC5 (3.2)
Synch ACDC	Disabled	Independent AC tuning
Actual / Global Core / Cache Voltage	Auto / Auto / Auto	No fixed Vcore or global offset
PL1 / PL2	320 / 320 W	Selected Extreme operating envelope for the 14900KS
Tau / ICCMAX	56 s / 400 A	Not a margin estimate based on a single IOOUT Maximum
IA CEP / SA CEP	Enabled / Enabled	Protections remain enabled
UnderVolt Protection	Disabled in the export	Do not treat disabling it as mandatory for a new setup
ABT / TBM 3.0	Enabled / Enabled	Dynamic frequency policy
TVB Voltage Opt. / Enhanced TVB	Enabled / Enabled	Temperature-dependent mechanisms are retained
CPU Current Reporting	100%	No intentional distortion of current reporting
Ring Down Bin / Thermal Monitor	Enabled / Enabled	Ring can downclock; thermal protection is active

THE PRINCIPLE OF THE FIRST VERSION IS RETAINED

A selected moderate LLC + verified applied AC/DC values + individually tuned AC + active protections + finite limits + separate heavy- and light-load tests. Not maximum clock speed at any cost, and not fixed Vcore.

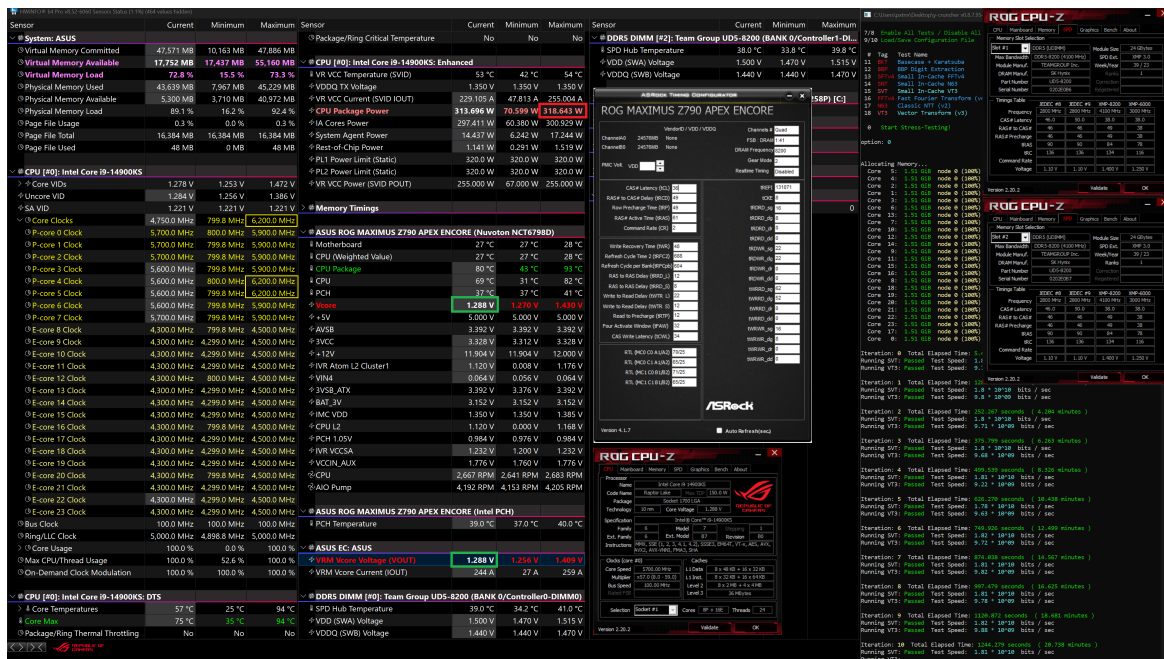
The text profile and BIOS recording remain historical materials. They may contain Trained and other OS, memory, or peripheral settings that are outside the method and are not recommendations in this CPU manual.

DOCUMENTATION CONSULTED: material from the working example; ASUS BIOS guides and information; Intel specifications and explanations.

Author's BIOS Profile, Author's Screenshots, ASUS ROG Z790 BIOS Manual, Intel UVP

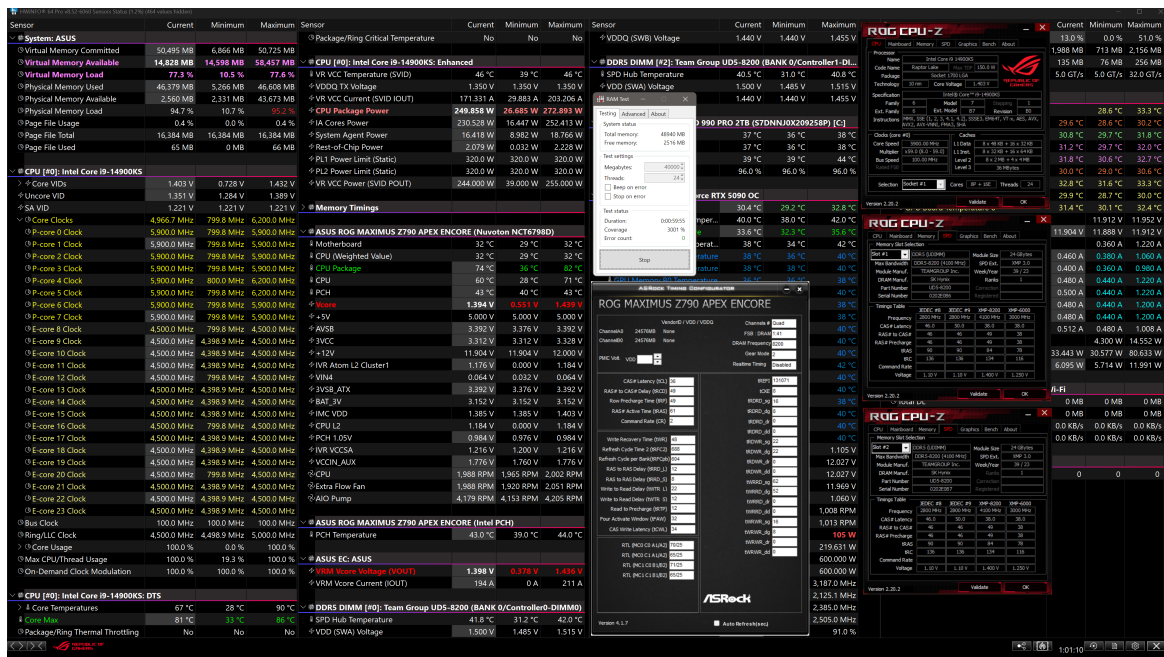
06 6.2 REFERENCE SCREENSHOTS

These are earlier reference materials, not new test runs. Both images are clickable and link to the originals.



CPU: Y-CRUNCHER SVT / VT3

The screenshot shows 20.738 min. The half-hour SVT/VT3 duration comes from my report of the run, not the elapsed time visible in this image.



RAM TEST: 3001%, 0 ERRORS

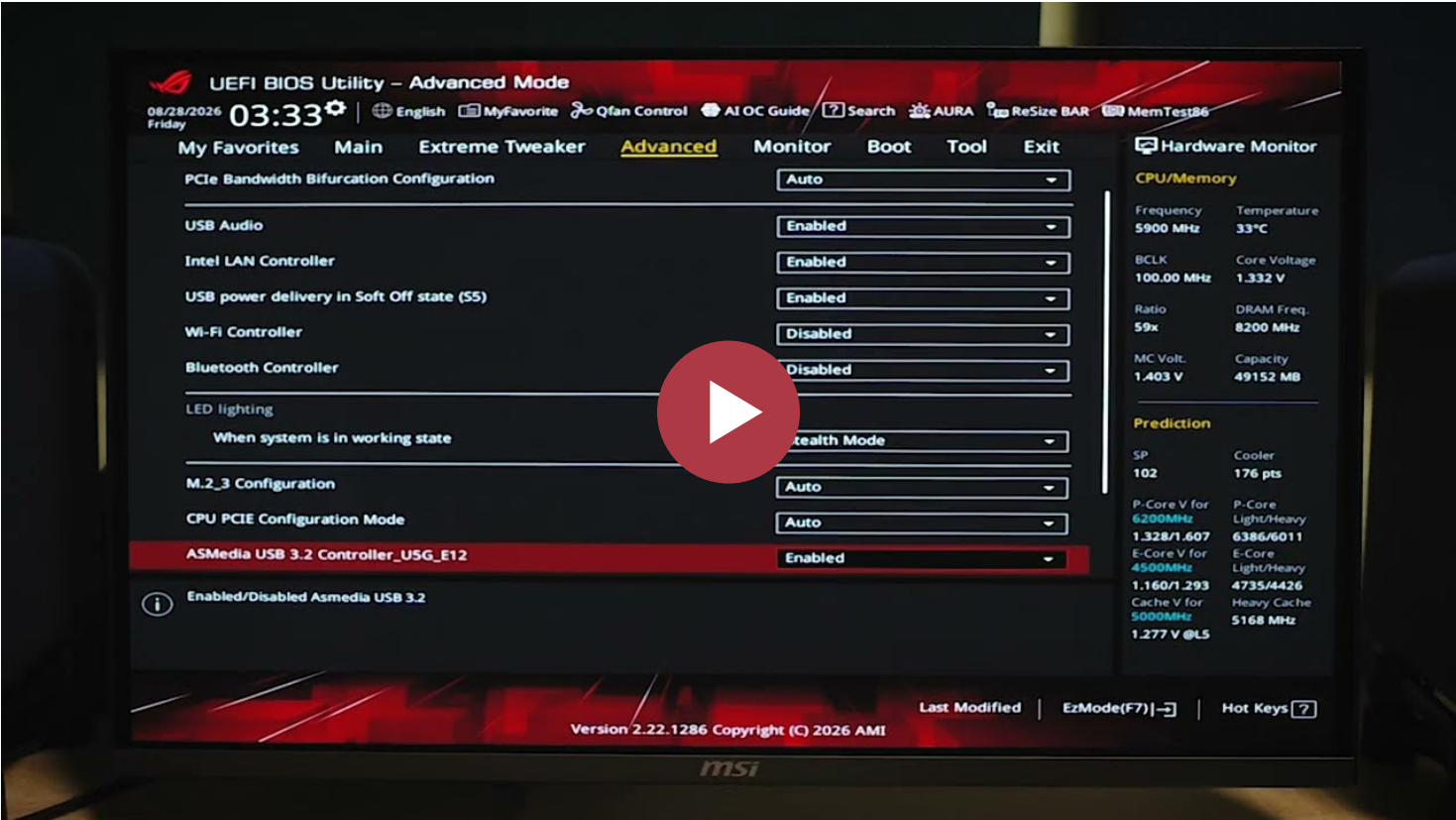
Ring in the screenshot: Current 4500 MHz (x45), Maximum 5000 MHz (x50). This run does not establish continuous operation at Ring x50.

High-resolution screenshots: bit.ly/2202hw

BIOS text profile: bit.ly/2202txt

06 6.3 BIOS 2202 VIDEO RECORDING

My recording of the original daily-use BIOS profile settings.



Z790 APEX ENCORE + 14900KS | 48GB@8200-36 | DAILY USE [BIOS 2202]

WATCH THE RECORDING ON YOUTUBE

youtu.be/Unt3nLivOZM

HISTORICAL MATERIAL

The recording and TXT are historical material. The later SVID Behavior = Auto clarification in the manual does not change the recording or constitute a new measurement; the archived TXT still contains Trained.

07 7.1 SOFTWARE: WEBSITES AND GUIDES

The test version and settings form part of the validation record. Links lead to official sites and guides; choosing a tool does not replace understanding the operating condition being tested.

HWINFO

Log sensor readings: VR VOUT / IOUT where available, VID, Effective Clock, temperature and limit flags. Save the log from each validation run.

[Official download](#)

[In this manual: 5.2](#)

CPU-Z

Check the CPU model, clocks, ratios, core count and thread count. A configuration snapshot is useful for reporting, but does not confirm stability.

[Official site](#)

[In this manual: 5.2](#)

Y-CRUNCHER

Component Stress Tester: SVT/VT3 and additional BKT, BBP and SFTv4 tests. Record the version/binary, threads, memory and duration. Compare load intensity on the specific system; an error does not automatically identify the cause.

[Official site and download](#) · [FAQ and troubleshooting](#)

[In this manual: 5.4](#)

OCCT

Test CPU and CPU + RAM with explicitly recorded test settings; core cycling is a separate check. Variable mode does not mean alternating load and idle.

[Official download](#) · [CPU guide](#)

[In this manual: 5.3](#)

CINEBENCH

Compare performance, temperature and sustained clocks during rendering. Use the same version and conditions; a successful run does not replace comprehensive stability testing.

[Official Maxon download](#)

[In this manual: 5.3](#)

KARHU RAM TEST

A memory validation run after CPU / Ring tuning. Record allocated memory, duration, coverage and errors; this is not a complete CPU stability test.

[Official site](#)

[In this manual: 6.2](#)

CORECYCLER

Additional sequential loading of individual cores; the official project supports Intel Active-Core Turbo. On a hybrid CPU, check P/E-core and HT affinity and test engine compatibility, and leave automatic voltage adjustment disabled.

[Official repository](#)

[In this manual: 5.3](#)

08 8.1 LGA1851 AND Z890: SCOPE OF THE METHOD

On Arrow Lake, an additional DLVR regulation stage operates between the external voltage regulator and the corresponding CPU domains. External VOUT therefore cannot automatically be treated as the final P-core, E-core, or Ring voltage after the internal regulators.



Transfers as a workflow	Requires separate LGA1851 tuning
Save a baseline, check BIOS and cooling	Select the mode and understand the purpose of the DLVR voltages
Limit power, current, and temperature	Use the limits for the specific Core Ultra, not the 14900KS
Change one setting and compare results	Re-establish what AC/DC and LLC mean for the relevant power rail
Separate heavy loads, per-core testing, and transitions	Distinguish external VOUT, internal requests, and available domain sensors
Check real workloads and repeatability	The DC table does not replace selecting the rail and DLVR mode; AC and voltages are tuned separately

DO NOT SWITCH A DAILY-USE SYSTEM TO BYPASS JUST TO MAKE IT SIMILAR

DLVR bypass mode is not a requirement for transferring this method. ASUS recommends Regulation Mode in the relevant guide. Specific P/E/Ring DLVR settings depend on the motherboard and BIOS version and require a separate chapter.

WHAT LGA1851 ON THE COVER MEANS

This revision explains the general tuning sequence and the limits of transferring it. It does not yet provide a complete guide to electrical tuning on Z890. No applicability percentage is given: there is no reproducible criterion for such an estimate.

FOR OTHER INTEL PLATFORMS

Even on LGA1700, the available feature set depends on the CPU, chipset, and BIOS. This example does not provide a ready-to-use profile for mobile or OEM systems, locked SKUs, or other generations. LLC names and limit values must be checked separately.

DOCUMENTATION CONSULTED: Intel specifications and explanations; ASUS BIOS guides and information.

Intel Core Ultra 200S / DLVR, ASUS ROG Z890 BIOS Manual, Intel VCCCORE

09 9.1 SVID OFFSET UNDERVOLTING

For LGA1700 / ASUS Z790, tune a negative SVID offset with LLC, AC/DC and SVID Behavior held constant. Manual AC is compatible with subsequent offset tuning, but an existing AC undervolt does not guarantee additional margin. Evaluate AC, offset and the VRM load-line together as a single configuration.

PREFERRED OPTION FOR DAILY USE

Of the two alternatives discussed here - SVID offset and FIXED - I recommend trying adaptive SVID offset first for daily use. The request remains dynamic, without a single manual VRM voltage target. This is a practical choice, not a proven energy advantage over AC undervolting or FIXED.

BIOS setting	Starting setting	Purpose / limitation
Global Core SVID Voltage	Adaptive Mode	Adjusts the CPU request, not the manual VRM output
Offset Mode Sign / Offset Voltage	"-" sign; magnitude set separately	Start with no offset specified; 0.010 V = 10 mV
Actual VRM Core Voltage / Cache SVID Voltage	Auto / Auto	Do not add a manual VRM setting or a separate Ring offset
Additional Turbo Mode CPU Core Voltage	Auto	Do not specify a separate turbo voltage
CPU Load-line Calibration	Choose and hold constant	A validated level, not necessarily LLC6
SVID Behavior	Chosen baseline	Auto or another previously validated Behavior
IA AC Load Line	Auto or manual AC	Choose before tuning offset; do not lower both together
IA DC Load Line	Match to LLC: Table 3.2	Not automatically equal to AC; not an undervolting control. Verification - 5.2
Limits / CEP / UVP	As in the main method	Finite PL/ICCMAX; protections enabled (4.2)

TUNING SEQUENCE: BASELINE FIRST, THEN OFFSET

- Save the profile and record the BIOS/microcode, clocks, memory and results. Before tuning offset, hold LLC, SVID Behavior and AC/DC constant. For independent manual AC/DC, set Synch ACDC to Disabled; verify the applied values after boot.
- Validate the baseline without a global offset, using finite limits and protections. For a manual AC undervolt, use a previously validated setting with margin, not AC at its stability limit. If errors or performance loss occur, do not add a negative offset.
- Change only the offset in steps such as 5-10 mV, saving BIOS settings and rebooting. Do not lower AC at the same time. Compare VID, VOUT, performance and Effective Clocks under comparable conditions. If results worsen, undo the step and retain margin.
- Repeat 5.3-5.4: heavy load, P/E-cores and peak boost, idle, transitions, sleep/wake and real workloads. After changing LLC, AC/DC, Behavior, Synch or the BIOS/profile, validate the baseline and offset again.

SVID BEHAVIOR: CHOOSE AND HOLD THE BASELINE CONSTANT

Choose Behavior before tuning offset and do not change it during tuning. Auto is a starting option, not a requirement. Keep a validated Trained or other Behavior setting as a separate baseline. After changing Behavior, recheck the applied AC/DC, voltages and performance. Auto for AC and Behavior refers to separate fields; manual AC does not prove that Behavior is fully disabled. BIOS 2202 precedence rules have not been confirmed.

Global does not promise the same shift for P/E/cache: a shared power rail does not mean identical requests or V/F relationships. CEP may limit performance; do not disable UVP as a routine step for BIOS undervolting. LGA1851 is covered separately (8.1).

A benefit is confirmed by maintaining performance with lower energy use, or increasing performance with comparable energy use and cooling. Lower VID, temperature or Package Power readings alone are not enough.

DOCUMENTATION CONSULTED: ASUS BIOS guides and information; Intel specifications and explanations.

ASUS ROG Z790 BIOS Manual, Intel VCCCORE, Intel FSP: V/F and Offset, Intel UVP, Intel: Tuning and Validation, ASUS: SVID Behavior Auto

09 9.2 FIXED: MANUAL VOLTAGE

My starting point: LGA1700, 14900KS, ASUS ROG Maximus Z790 Apex Encore / BIOS 2202; LLC6, P/E/Ring 5800/4500/5000, 1.35 V, HT Off. The remaining fields form a validation plan, not an export; the clocks and HT setting are specific to this example, not requirements for FIXED.

FIXED sets a manual VRM voltage target; clocks are controlled separately.

In steady state: $VOUT \approx VOverride - IOUT \times RLL$ (RLL is the load-line slope).

A 1.350 V target does not equal VOUT under every load: current, LLC and transient overshoot must be considered separately.

F7: E = Extreme Tweaker; D = E > Digi+ VRM; I = E > Internal CPU Power Management; T = E > Tweaker's Paradise. C = Advanced > CPU Configuration; A = C > CPU - Power Management Control. Tau = Package Power Time Window.

BIOS setting / path	LLC6: main branch	LLC5: separate trial
D: CPU Load-line Calibration	Level 6	Level 5
I: IA AC Load Line / IA DC Load Line	0.49 / 0.49 mΩ	0.73 / 0.73 mΩ
D: Synch ACDC Loadline with VRM Loadline	Disabled	Disabled
E: Actual VRM Core Voltage > CPU Core Voltage Override	Manual Mode / 1.350 V	Manual Mode / 1.350 V
E: SVID Behavior / I: CPU SVID Support	Auto / Enabled	Auto / Enabled
E: Global Core SVID Voltage / Cache SVID Voltage	Auto / Auto	Auto / Auto
E: Performance / Efficient Core Ratio; ALL-Core Ratio Limit	Sync All Cores; 58 / 45	Sync All Cores; 58 / 45
E: Min./Max. CPU Cache Ratio; Ring Down Bin	Auto / 50; Enabled	Auto / 50; Enabled
E: ASUS MultiCore Enhancement	Disabled - Enforce All limits	Disabled - Enforce All limits
I: Long / Short Duration Package Power Limit; Tau	253 / 253 W; 56 s	253 / 253 W; 56 s
I: CPU Core/Cache Current Limit Max.; Unlimited ICCMAX	307 A; Disabled	307 A; Disabled
I: IA CEP / SA CEP; T: UnderVolt Protection	Enabled (all)	Enabled (all)
I: Maximum CPU Core Temperature; D: CPU Current Reporting	90 °C; 100%	90 °C; 100%
D: CPU Voltage Suspension; C: Hyper-Threading	Disabled (both)	Disabled (both)
A: CPU C-states / Thermal Monitor	Enabled / Enabled	Enabled / Enabled

Choose DC for the selected LLC from Table 3.2. AC = DC is the reference baseline for this trial, not a requirement for FIXED mode. 253 W / 307 A / 90 °C are the trial limits; Ring 50 is the ceiling. For comparison with SVID offset, keep clocks, HT, memory, limits and cooling identical.

SEQUENCE: LLC6 FIRST, THEN A SEPARATE LLC5 BRANCH

1. Save the profile; use BCLK 100 MHz and keep memory settings unchanged. ABT and Overclocking TVB = Disabled; V/F, per-core offsets, CPU Core/Cache Boot Voltage = Auto. Enter the LLC6 column settings, press F10 and reboot; verify AC/DC, ratios, HT and limits.
2. Use a short load to check VOUT/IOUT and temperature. Before lowering Override, validate the starting 1.350 V setting using 5.3-5.4. If errors or unexplained performance loss occur, review the baseline first instead of continuing to lower it.
3. Lower only Override in 0.005 V steps; check VOUT/IOUT, temperature, Effective Clocks and the result of the same test. If performance drops, check for limits; the absence of errors does not mean success. If results worsen, undo the step and retain margin.
4. For LLC5, restore the starting Override of 1.350 V and change LLC/AC/DC as shown in the table. At the same Override and current, LLC5 produces more Vdroop than LLC6; compare VOUT using measurements. This is a separate trial. If it fails, return to LLC6 or lower clocks; do not automatically raise voltage.
5. Revalidate each branch using 5.3-5.4, including warm-up, load/idle and sleep/wake. Power/current/temperature limits may lower clocks: such a run does not validate stability at 58/45/50.

A TARGET IS NOT A MEASUREMENT AND DOES NOT GUARANTEE SAFETY

Do not adjust DC solely to make VID = VOUT. Matching DC to LLC does not confirm Package Power accuracy under Override; verify power consumption and limit behavior separately (5.2). CEP Enabled does not rule out performance loss from internal limiting caused by Vdroop. Keep protections enabled. Software monitoring does not guarantee that brief voltage overshoot is captured; a 1.35 V target alone does not guarantee safety. Z890 / DLVR is covered separately (8.1).

09 9.2.1 FIXED: BENCHMARK TUNING

LGA1700 / ASUS Z790. Supplement to 9.2: the goal is the highest possible result in the selected benchmark, not a universal daily-use profile. A successful run does not prove system stability under other loads. E/D/I/C/A paths are as defined in 9.2.

BIOS settings	What to change or check against the 9.2 baseline
E: Performance / Efficient Core Ratio; Min./Max. CPU Cache Ratio	Tune P/E and Ring for the test and cooling. Choose Sync All Cores or By Core Usage according to the load; ABT and Overclocking TVB = Disabled. Setpoints do not guarantee sustained clocks: account for Ring Down Bin, Core / Effective Clocks and the actual Ring clock.
I: Long / Short Duration Package Power Limit; Package Power Time Window	Raise PL1/PL2 when they are the limiting factor; Auto may be retained if the actual limits do not constrain the test. MCE = Enabled - Remove All limits is a separate option, not a synonym for Auto. Tau controls power averaging; with PL1 = PL2 there is no transition to a lower limit.
I: CPU Core/Cache Current Limit Max.; Unlimited ICCMAX	Raise ICCMAX when current is the limiting factor. For an extended range: Unlimited ICCMAX = Enabled; check the applied ICCMAX and Limit Reasons. This does not disable all protections or replace the separate VRM CPU Current Capability limit.
E: Actual VRM Core Voltage > CPU Core Voltage Override; D: CPU Load-line Calibration	Tune Override for performance, not minimum Vcore. Here: LLC6 / DC 0.49 mΩ or LLC7 / DC 0.24 mΩ (3.2). Compare VOUT, droop and heat; LLC7 increases compensation and the risk of overshoot. Maximum LLC is not needed by default.
C: Hyper-Threading / Active Efficient Cores; A: CPU C-states / SpeedStep / Speed Shift	HT = Enabled (ON) is the baseline: Cinebench Multi Core results are usually higher. Active Efficient Cores = All is the starting point for a multithreaded test; choose the active core configuration by results. CPU C-states = Enabled as in 9.2; change it in a separate trial. EIST / Speed Shift are covered below.
I: IA CEP / SA CEP; A: Thermal Monitor	Before disabling CEP, check VOUT, errors and Limit Reasons for power, current and temperature. A Core / Effective Clocks gap alone does not prove CEP is active. Settings and scope are given below.

RELATED CPU FEATURES: BENCHMARK FIXED ONLY

BIOS setting	Value for benchmark FIXED
A: Intel SpeedStep (EIST)	Disabled *
A: Intel Speed Shift	Disabled
I: IA CEP Enable	Disabled
I: SA CEP Enable	Disabled
A: Thermal Monitor	Enabled
A: Turbo Mode	Enabled

EIST / Speed Shift: Disabled for predictable ratios without dynamic P-state / HWP control; this is not daily-use advice and does not fix the clock frequency. * If Turbo depends on EIST, leave EIST Enabled and verify the turbo ratio.

IA CEP can reduce Effective Clocks under aggressive Vcore / load-line settings even without a crash. Disabled removes this response.

SA CEP: Disabled is the same choice for the System Agent. Its contribution to a CPU benchmark may be less noticeable and depends on the BIOS / load; disabling it does not guarantee a gain. Disabling both CEP features removes their protective function.

Thermal Monitor: Enabled retains hardware thermal limiting. If it activates, temperature is the limiting factor; do not disable it for a higher score. The independent emergency THRMTRIP shutdown does not replace this protection.

BRIEF PROCEDURE

1. Save the daily-use profile and a separate benchmark BIOS profile based on 9.2.
2. Choose the benchmark version and mode; hold memory, BCLK, OS/background activity, threads and cooling conditions constant.
3. Change one parameter at a time; when changing LLC, match DC to it while keeping the other conditions unchanged.
4. Compare 2-3 runs by score, Effective Clocks, temperature and Limit Reasons. Discard runs with errors or invalid results; if results worsen, undo the step.
5. Save the best confirmed configuration separately; restore the daily-use profile after benchmarking.

A SHORT RUN DOES NOT GUARANTEE SAFETY

Good cooling does not eliminate electrical risks: CPU degradation, crashes and data corruption are possible. There is no universally safe Override. Back up important data in advance.

DOCUMENTATION CONSULTED: ASUS BIOS guides and information; Intel specifications and explanations; explanations by the HWiNFO author.

ASUS ROG Z790 BIOS Manual, Intel Datasheet, Intel CEP, Intel: Tuning and Validation, HWiNFO: Effective Clock

09 9.3 AUTO SVID: LIMITING TURBO RATIOS

Limit the upper P-core and E-core Turbo ratios while leaving voltage control automatic. Choose ratios and clock speeds for the individual CPU silicon and cooling capability. The CPU uses SVID; no manual Vcore or negative offset is set. Ratios define a ceiling, not a constant clock speed: Turbo remains enabled.

Reducing the upper boost limit may lower the voltage request and heat, but does not guarantee undervolting at the same frequency. Single-threaded and light-load performance may decrease.

MY GAMING PROFILE: CORE I9-14900KS + Z790 APEX ENCORE

Apex Encore / BIOS 2202 / ASUS Advanced OC Profile. This motherboard profile is selected separately from Intel Default Settings and does not mean AI Overclocking.

Setting	Author's example
CPU profile	ASUS Advanced OC Profile
Performance Core Ratio / ALL-Core Ratio Limit	Sync All Cores / 58
Efficient Core Ratio / ALL-Core Ratio Limit	Sync All Cores / 45
Min./Max. CPU Cache Ratio / Ring Down Bin	Auto / 50 / Enabled
Hyper-Threading (HT)	Disabled - my gaming profile
Enhanced C-states (C1E)	Enabled - required state
CPU C-states	Disabled; Auto is a separate choice
Actual VRM Core Voltage / Global Core SVID Voltage	Auto / Auto
SVID Behavior	Auto
Manual offsets and V/F adjustments	Not set
CPU Load-line Calibration	Level 6
IA AC Load Line / IA DC Load Line	Auto / 0.49 mΩ
Synch ACDC Loadline with VRM Loadline	Disabled
PL1 / PL2 / CPU Core/Cache Current Limit Max.	320 W / 320 W / 400 A
Maximum CPU Core Temperature	100 °C - a ceiling, not a target
Turbo Mode	Enabled

Choose HT for the workload with any method. In my experience, HT Enabled requires a lower Ring ratio and revalidation; the value is individual. Ring x50 is a ceiling: Ring Down Bin Enabled permits downclocking.

On this board and BIOS, I observe C1E locked Enabled: this field must remain enabled. CPU C-states is separate: Auto or Disabled, as here. The C1E field does not prove idle-state use; with CPU C-states Disabled, check idle power. Check gaming performance separately.

SVID Behavior = Auto is the starting point. Trained uses an ASUS prediction based on CPU, clocks and LLC; an advantage is not guaranteed. Compare with identical P/E/Ring, HT and limits, changing only Behavior; recheck applied AC/DC and stability.

PREPARATION AND VALIDATION

When changing methods, load a saved validated baseline, especially after benchmark FIXED. Restoration and individual Turbo settings: 9.3.1. After boot, record AC/DC; do not infer AC Auto from LLC. LLC6 / DC 0.49 mΩ is this example (3.2); DC is not an undervolting control. Screenshot: 9.3.2.

09 9.3.1 AUTO SVID: VALIDATION UNDER LOAD

After benchmark FIXED, restore the baseline: CPU SVID Support, EIST/SpeedStep, HWP/Speed Shift, IA/SA CEP, UVP and Thermal Monitor = Enabled; Current Reporting = 100%, finite PL/ICCMAX, Unlimited ICCMAX = Disabled. Actual/Global/Cache and manual P/E voltages = Auto, no offsets/V/F adjustments; Voltage Suspension = Disabled.

MY PROCEDURE FOR COMPARING VCORE AND VOUT

1. RECORD THE SETTINGS

Remove prior ratio/OC TVB adjustments, then apply the limits in 9.3. Recommended Turbo baseline (4.1): ABT, TBM 3.0, TVB Voltage Optimizations, Enhanced TVB = Enabled; OC TVB = Auto. This is preparation, not a new profile export. Record BIOS/microcode, AC/DC, LLC, Behavior, P/E/Ring, HT, limits and the test mode.

2. WAIT FOR A STEADY LOAD

Test Cinebench, the y-cruncher component and the OCCT mode separately. Save an HWiNFO log; after warm-up, compare one interval without pauses or component changes. For fresh minima, reset Min/Max after the load settles.

3. COMPARE VCORE AND VRM VCORE VOLTAGE (VOUT)

On this system, my method expects Current and logged values to remain close throughout the cycle with small fluctuations. Exact equality is not required: sensing points, accuracy and polling differ. Two independent Minimum values do not describe one moment.

4. CHECK RESULTS AND REPEATABILITY

Apply 5.3-5.4: errors/WHEA, temperatures, Effective Clocks, actual P/E/Ring, limits and results. Under limits, only attained clocks are validated. Compare small gains with baseline variation; matching voltages does not prove stability.

MUST "SVID VMIN" MATCH VCORE AND VOUT?

No. Collapsed Core VIDs is an aggregate average of core VIDs, not the highest request or a direct command to the external VRM. Expand the group and read individual cores over the same interval. SVID is an interface; the CPU reports VID, while Vcore/VOUT are measurement channels.

The three rows may remain close throughout the cycle, but this is not required. Do not adjust DC to force VID = VOUT: the reading does not replace checks of the model, performance and stability.

VMIN, MINIMUM AND VOLTAGE UNDER LOAD

Vmin is the lowest voltage sufficient for stable operation under specified conditions; testing locates its boundary. Minimum in HWiNFO is the lowest sample recorded since statistics were reset. Steady-state load voltage alone does not establish that Vmin has been reached. Different sensors may reach their minima at different times; software polling can miss brief transients.

9.3.2 AUTO SVID: MONITORING EXAMPLE

HWINFO® 64 Pro v8.54-6090 Sensors Status (0.8%) (423 values hidden)								Cinebench 2026.1.3			
Sensor	Current	Minimum	Maximum	Sensor	Current	Minimum	Maximum	Sensor	Current	Minimum	Maximum
System: ASUS				Core Max	81 °C	33 °C	86 °C	VCCIN_AUX	1.824 V	1.824 V	1.840 V
Virtual Memory Committed	19,825 MB	6,841 MB	19,836 MB	Package/Ring Thermal Throttling	No	No	No	CPU	1,406 RPM	1,210 RPM	1,415 RPM
Virtual Memory Available	45,498 MB	45,487 MB	58,482 MB	Package/Ring Critical Temperature	No	No	No	Extra Flow Fan	1,539 RPM	1,431 RPM	1,562 RPM
Virtual Memory Load	30.3 %	10.4 %	30.3 %	Package/Ring Power Limit Exceeded	No	No	No	AIO Pump	4,179 RPM	2,257 RPM	4,205 RPM
Physical Memory Used	16,374 MB	5,193 MB	16,374 MB								
Physical Memory Available	32,564 MB	32,564 MB	43,746 MB								
Physical Memory Load	33.4 %	10.6 %	33.4 %								
Page File Usage	0.0 %	0.0 %	0.0 %								
Page File Total	16,384 MB	16,384 MB	16,384 MB								
Page File Used	0 MB	0 MB	0 MB								
CPU [#0]: Intel Core i9-14900KS											
Core VIDs	1.239 V	0.737 V	1.311 V	VR VCC Temperature (SVID)	48 °C	38 °C	48 °C				
Uncore VID	1.284 V	0.798 V	1.321 V	VDDQ TX Voltage	1.350 V	1.350 V	1.350 V				
SA VID	1.221 V	1.221 V	1.221 V	VR VCC Current (SVID IOUT)	225.121 A	0.000 A	251.019 A				
Core Clocks	4,820.8 MHz	799.8 MHz	5,800.0 MHz	CPU Package Power	274.980 W	41.042 W	281.584 W				
P-core 0 Clock	5,700.0 MHz	799.8 MHz	5,800.0 MHz	IA Cores Power	257.634 W	31.051 W	266.934 W				
P-core 1 Clock	5,700.0 MHz	799.8 MHz	5,800.0 MHz	System Agent Power	15.469 W	0.000 W	21.617 W				
P-core 2 Clock	5,700.0 MHz	799.8 MHz	5,800.0 MHz	Rest-of-Chip Power	0.996 W	0.000 W	2.480 W				
P-core 3 Clock	5,700.0 MHz	799.8 MHz	5,800.0 MHz	PL1 Power Limit (Static)	320.0 W	320.0 W	320.0 W				
P-core 4 Clock	5,700.0 MHz	799.8 MHz	5,800.0 MHz	PL2 Power Limit (Static)	320.0 W	320.0 W	320.0 W				
P-core 5 Clock	5,700.0 MHz	799.8 MHz	5,800.0 MHz	VR VCC Power (SVID POUT)	255.000 W	5.000 W	255.000 W				
P-core 6 Clock	5,700.0 MHz	799.8 MHz	5,800.0 MHz								
P-core 7 Clock	5,800.0 MHz	799.8 MHz	5,800.0 MHz								
E-core 8 Clock	4,400.0 MHz	799.8 MHz	4,400.0 MHz								
E-core 9 Clock	4,400.0 MHz	799.8 MHz	4,400.0 MHz								
E-core 10 Clock	4,400.0 MHz	799.8 MHz	4,400.0 MHz								
E-core 11 Clock	4,400.0 MHz	799.8 MHz	4,400.0 MHz								
E-core 12 Clock	4,400.0 MHz	799.8 MHz	4,400.0 MHz								
E-core 13 Clock	4,400.0 MHz	800.0 MHz	4,400.0 MHz								
E-core 14 Clock	4,400.0 MHz	799.8 MHz	4,400.0 MHz								
E-core 15 Clock	4,400.0 MHz	799.8 MHz	4,400.0 MHz								
E-core 16 Clock	4,400.0 MHz	799.8 MHz	4,400.0 MHz								
E-core 17 Clock	4,400.0 MHz	799.8 MHz	4,400.0 MHz								
E-core 18 Clock	4,400.0 MHz	799.8 MHz	4,400.0 MHz								
E-core 19 Clock	4,400.0 MHz	800.0 MHz	4,400.0 MHz								
E-core 20 Clock	4,300.0 MHz	799.8 MHz	4,400.0 MHz								
E-core 21 Clock	4,300.0 MHz	799.8 MHz	4,400.0 MHz								
E-core 22 Clock	4,300.0 MHz	800.0 MHz	4,400.0 MHz								
E-core 23 Clock	4,300.0 MHz	800.0 MHz	4,400.0 MHz								
Bus Clock	100.0 MHz	100.0 MHz	100.0 MHz								
Ring/LLC Clock	5,000.0 MHz	2,499.4 MHz	5,000.0 MHz								
Core Usage	99.4 %	0.0 %	100.0 %								
Max CPU/Thread Usage	100.0 %	-1.0 %	100.0 %								
On-Demand Clock Modulation	100.0 %	100.0 %	100.0 %								
CPU [#0]: Intel Core i9-14900KS: DTS											
Core Temperatures	77 °C	27 °C	86 °C								

Sensor	Current	Minimum	Maximum
ASUS ROG MAXIMUS Z790 APEX ENCORE (Intel PCH)			
PCH Temperature	42.0 °C	40.0 °C	47.0 °C
ASUS EC: ASUS			
VRM Vcore Voltage (VOUT)	1.227 V	0.750 V	1.534 V
VRM Vcore Current (IOUT)	213 A	1 A	241 A
DDR5 DIMM [#0]: Team Group UD5-8200 (BANK 0/Controller0-DIM...			
SPD Hub Temperature	36.8 °C	28.2 °C	36.8 °C
VDD (SWA) Voltage	1.485 V	1.470 V	1.515 V
VDDQ (SWB) Voltage	1.440 V	1.425 V	1.455 V
DDR5 DIMM [#2]: Team Group UD5-8200 (BANK 0/Controller1-DIM...			
SPD Hub Temperature	35.5 °C	27.8 °C	35.5 °C
VDD (SWA) Voltage	1.500 V	1.470 V	1.515 V
VDDQ (SWB) Voltage	1.440 V	1.425 V	1.455 V
S.M.A.R.T.: Samsung SSD 990 PRO 2TB (S7DNNJ0X209258P) [C:]			
Drive Temperature	39 °C	36 °C	41 °C
Drive Temperature 2	39 °C	36 °C	41 °C
Drive Temperature 3	42 °C	38 °C	48 °C
Drive Remaining Life	96.0 %	96.0 %	96.0 %
ASUS ROG ASTRAL GeForce RTX 5090 OC			
GPU Temperature	29.5 °C	26.7 °C	33.3 °C
GPU Memory Junction Temperature	38.0 °C	36.0 °C	42.0 °C
GPU Hot Spot Temperature	32.6 °C	29.6 °C	35.8 °C
GPU Memory Chip Temperatures	37 °C	32 °C	42 °C
GPU Memory A0 Temperature	36 °C	34 °C	40 °C
GPU Memory A1 Temperature	38 °C	34 °C	40 °C
GPU Memory B0 Temperature	36 °C	32 °C	38 °C
GPU Memory B1 Temperature	36 °C	34 °C	40 °C
GPU Memory C0 Temperature	36 °C	32 °C	40 °C
GPU Memory C1 Temperature	36 °C	32 °C	40 °C
GPU Memory D0 Temperature	36 °C	34 °C	40 °C
GPU Memory D1 Temperature	38 °C	34 °C	40 °C
GPU Memory E0 Temperature	36 °C	34 °C	40 °C
GPU Memory E1 Temperature	38 °C	36 °C	42 °C
GPU Memory F0 Temperature	38 °C	36 °C	42 °C
GPU Memory F1 Temperature	38 °C	34 °C	40 °C
GPU Memory G0 Temperature	34 °C	32 °C	38 °C
GPU Memory G1 Temperature	38 °C	34 °C	40 °C
GPU Memory H0 Temperature	38 °C	34 °C	40 °C

Cinebench 2026

Maxon Cinebench

PERFORMANCE

GPU

CPU (Multiple Threads) Running ... 05:27

CPU (Single Core)

CPU (Single Thread)

MP Ratio

YOUR SYSTEM

Processor Intel Core i9-14900KS

Cores x GHz 24 Cores @ 3.19 GHz

GPU NVIDIA GeForce RTX 5090 (CUDA, Driv...

Operating System Windows 11, 64 Bit, Professional Editio...

Info

RANKING (How We Measure)

CPU (Multiple Threads)

1. 128C @ 3 GHz, Ampere Ultra Max Processor 18495

2. 32C @ 3.6* GHz, Apple M3 Ultra 12082

3. 24C @ 3.69 GHz, Intel Core Ultra 9 285K 9132

4. 24C @ 3.19 GHz, Intel Core i9-14... Running ... (8513 pts)

5. 16C @ 3.9* GHz, Apple M4 Max 7829

6. 32C/64T @ 3 GHz, AMD Ryzen Threadripper 2990... 4568

7. 12C @ 2.98 GHz, Snapdragon X 12-core X1E80100 3717

8. 8C/16T @ 3.8 GHz, AMD Ryzen 7 5800X 8-Core Pr... 3441

ROG CPU-Z

CPU Mainboard Memory SPD Graphics Bench About

Processor

Name Intel Core i9 14900KS

Code Name Raptor Lake Max TDP 150.0 W

Package Socket 1700 LGA

Technology 10 nm Core Voltage 1.234 V

Specification

Family Intel® Core™ i9-14900KS

Ext. Family 6

Model 7

Stepping 1

Revision B0

Clocks (core #0)

Core Speed 5698.63 MHz

Multiplier x57.0 (8.0 - 59.0)

Bus Speed 100.00 MHz

Caches

L1 Data 8 x 48 KB + 16 x 32 KB

L1 Inst. 8 x 32 KB + 16 x 64 KB

Level 2 8 x 2 MB + 4 x 4 MB

Level 3 36 MBytes

Selection Socket #1

Cores 8P + 16E

Threads 24

Version 2.20.2

Validate

OK

GPU PCIe Slot (PEG) Power 11.222 W

Windows Hardware Errors (WHEA)

Total Errors

Current: Core VIDs (aggregate) 1.239 V; Vcore 1.217 V; VOUT 1.227 V. The 10 and 12 mV differences between rows are observations, not universal tolerances. Minimum includes idle. This recording shows an E-core maximum of x44; Table 9.3 uses x45. The frame illustrates sensor readings during a run, not a completed validation of the 9.3 profile.

10

10.1 DOCUMENTATION USED

Primary and technical material used to review the method. Official documentation is distinguished from community observations and the author's archived material.

INTEL: PROCESSORS AND ELECTRICAL MODEL

- Intel. Core 13th/14th Gen Datasheet, Vol. 1, 743844-015 (May 2025), pp. 64-67, 103-104, 182, 186-192.
- Intel. VCCCORE DC Specifications. Datasheet 743844, Rev. 015 (May 2025).
- Intel. Current Excursion Protection (CEP). 743844-015, Section 13.1.5, p. 187.
- Intel Support. Undervolt Protection / Intel XTU. Article 000094219, revision dated April 7, 2026.
- Intel Support. Vmin Shift Instability - Latest Information. Article 000102331, revision dated July 21, 2026.
- Intel. Core i9-14900KS Product Specifications, SKU 237504. Accessed September 8, 2026.
- Intel. 14th Gen Core Desktop Processors Product Brief: TBM 3.0, TVB and ABT.
- Intel. Core Ultra 200S Advocacy Deck (September 2025), slide 51: Overclocking Overhauled / DLVR.
- Intel. RaptorLake-S FSP, FspmUpd.h: CoreVoltageOverride / Offset and V/F. Copyright 2023; accessed September 8, 2026.
- Intel. Overclocking CPU with Intel Extreme Tuning Utility. Accessed September 8, 2026.

MOTHERBOARDS AND BIOS

- ASUS. ROG Z790 Series BIOS Manual, Intel 14th Gen, E22758 (October 2023), pp. 20-27, 41-49, 53-57, 68-70.
- Jiaszzz_ASUS / ASUS Support. SVID Behavior Auto on Prime Z790-P, BIOS 1658 (July 4, 2024).
- ASUS. ROG Maximus Z790 Apex Encore - BIOS & Firmware. BIOS 2202 (August 20, 2026).
- ASUS. ROG Maximus Z790 Apex Encore - official motherboard page. Accessed September 8, 2026.
- ASUS. ROG Z890 Series BIOS Manual, E25061 (January 2025), pp. 55-56: DLVR Mode and P/E/Ring domains.
- ASUS. ROG STRIX Z790 BIOS Manual, E23196: SVID Behavior, ratio limits, Ring and Auto voltage, pp. 21, 24-27, 45, 52-54.
- ASUS. FAQ 1053456 (August 23, 2024): Intel Default Settings and ASUS Advanced OC Profile.
- Shamino / ROG Forum. SVID Behavior Trained: prediction using CPU, frequencies and VRM load-line. Accessed October 1, 2026.

MONITORING

- Martin / HWiNFO. Another question about DC loadline and VID (June 23, 2025).

MONITORING (CONTINUED)

- Martin / HWiNFO. Effective clock vs instant (discrete) clock (October 15, 2019).
- Martin / HWiNFO. Vcore vs VR VOUT (Vcore)? (October 15, 2024): VID request and voltage measurements.
- Martin / HWiNFO. Copy and paste, reply #2: averaging group rows. Accessed October 3, 2026.

SOFTWARE AND TESTING

- Alexander J. Yee. y-cruncher: official site and Component Stress Tester.
- Alexander J. Yee. y-cruncher Version History: SVT, VT3 and legacy VST. Accessed September 8, 2026.
- OCCT. Stability Testing Configuration: CPU + RAM. Accessed September 8, 2026.
- Karhu Software. RAM Test: official site and FAQ. Accessed September 8, 2026.
- Microsoft Learn. WHEA Hardware Error Events. Accessed September 8, 2026.
- OCCT. Stability Testing Configuration: CPU. Accessed September 8, 2026.
- Alexander J. Yee. y-cruncher 0.8.7.9547b (Windows Only); Command Lines.txt: BKT, BBP, SFTv4.
- Alexander J. Yee. y-cruncher - Frequently Asked Questions. Accessed September 8, 2026.
- Alexander J. Yee. y-cruncher User Guides - Memory Allocation. Accessed September 8, 2026.
- sp00n / CoreCycler. Official README: core cycling, Intel Active-Core Turbo. Accessed October 3, 2026.

COMMUNITY OBSERVATIONS

- Snafu42 / ASUS ROG Forum. CPU Load-line Calibration vs. SVID Behavior. STRIX Z790-E, BIOS 2503 (October 2, 2024).
- SkatterBench #53 (January 22, 2023). Motherboard Auto-Rules: AC/DC and LLC changes with Turbo Ratios.
- SkatterBench #67 (December 16, 2023). V/F and automatic/adaptive voltage control.

AUTHOR'S MATERIAL

- Maxim Pakhtunov. APEX_2202_final.txt - archived BIOS 2202 export dated August 28, 2026.
- Maxim Pakhtunov. Archived HWiNFO / y-cruncher / RAM Test screenshots; HWiNFO / Cinebench capture dated October 1, 2026.
- Maxim Pakhtunov. Z790 APEX ENCORE + 14900KS | 48GB @ 8200-36 | DAILY USE [BIOS 2202]. Video recording.

11

11.1 VOLTAGE AND POWER DELIVERY

CPU requests, the VRM and sensors operate at different levels. Click a term to open the relevant discussion.

Term	Full Name	Explanation
SVID	Serial Voltage Identification	The command and telemetry interface between the CPU and VRM, not a Vcore sensor. Distinguish it from CPU-reported Core VIDs and the ASUS SVID Behavior policy (9.1, 9.3).
VID / Core VID	Voltage Identification	The CPU reports VID; it is not measured Vcore or necessarily a direct SVID command. Collapsed Core VIDs averages the core group, not its maximum. Expand it for detail (9.3.1).
V/F	Voltage / Frequency	The voltage-frequency relationship underlying adaptive control. The final operating request also depends on load, temperature and active adjustments.
AC LL	IA AC Load Line	Load-dependent adjustment of the voltage request. The main method lowers AC; 9.1 chooses and holds it constant beforehand, then changes the global offset. Manual AC and offset are not mutually exclusive.
DC LL	IA DC Load Line	A parameter in the droop model used for voltage and power accounting. This method chooses DC by LLC from 3.2. It is not IOOUT calibration or a separate undervolting control.
LLC / Vdroop	Load-line Calibration / Voltage Droop	LLC changes the VRM load-line; Vdroop is its steady-state, load-dependent voltage drop. Stronger LLC does not guarantee better stability during load transitions.
VRM / VCCCORE	Voltage Regulator Module / Core Power Rail	The VRM converts power for the processor; VCCCORE denotes the power rail discussed here. Its voltage, current and power cannot be equated with the entire CPU Package.
VOUT / Vcore	VRM Output Voltage / Core Voltage	VOUT is regulator telemetry; Vcore is a motherboard sensing channel, Die Sense in the example. Measurement points and polling differ; equality is not required. Compare within the same interval (9.3.1).
IOOUT / POUT	VRM Output Current / Power	The regulator output current and power reported by telemetry. Checking $P \approx U \times I$ requires simultaneous readings from the same domain without sensor saturation.
Package / IA Power	CPU Package / IA Cores Power	Power estimates for the processor package and IA domain. Their coverage differs; a separate VRM power rail does not have to match Package Power.
Current Reporting	CPU Current Reporting	Scales the reported current. The manual retains 100%; deliberately underreporting current does not reduce actual consumption and may compromise accurate power control.
CPU Input Voltage LLC	CPU Input Voltage Load-line Calibration	Adjusts the load-line characteristic of the separate auxiliary CPU Input rail. This is not VCCCORE rail LLC or a setting for the main VRM's 12 V input.
Adaptive	Adaptive Voltage	Dynamically controls the voltage request according to CPU operating conditions. Section 9.1 retains adaptive mode and sets a negative offset separately; this is not fixed Vcore.
SVID offset	Global Core SVID Voltage Offset	An adjustment to the request with a "+" or "-" sign; negative for undervolting (9.1). It is not equivalent to a VRM offset or AC LL and does not guarantee an identical shift in all physical voltages.
FIXED	Manual VRM Voltage / Voltage Override	In 9.2, a manual Actual VRM Core Voltage target. It does not fix the clock frequency, eliminate Vdroop or prove the absence of power saving; verify actual behavior through measurements.
DLVR	Digital Linear Voltage Regulator	An additional voltage regulation stage in Arrow Lake. Its presence changes the interpretation of external VOUT and prevents direct transfer of Z790 electrical settings.
SVID Behavior	Auto / Trained	An ASUS policy. Auto depends on the BIOS; Trained uses a prediction for SVID settings. An advantage of Trained is not guaranteed. After changing it, check applied AC/DC values and load behavior (9.3).

REQUEST, MODEL AND MEASUREMENT ARE DIFFERENT LEVELS

AC/DC values are model parameters, not measurements of the physical load-line. Similar VID and VOUT values do not prove DC calibration; software monitoring does not rule out fast overshoot.

DOCUMENTATION CONSULTED: Intel specifications and explanations; ASUS BIOS guides and information; explanations by the HWiNFO author.

Intel VCCCORE, ASUS ROG Z790 BIOS Manual, HWiNFO: VID and DC Load-line

11

11.2 CLOCKS, LIMITS AND PROTECTION

Terms for frequency policy, power and current limits, and protections. The saved BIOS value and the actual reason for limiting operation are checked separately. Click a term to open the relevant discussion.

Term	Full Name	Explanation
P-core / E-core / HT	Performance Core / Efficient Core / Hyper-Threading	Performance P-cores and Efficient E-cores. HT provides two threads per P-core; it is off in the gaming profile, but can be enabled for the task with any method. Recheck Ring and CPU stability after a change.
Ratio / bin / Ring	Frequency Multiplier / Frequency Step / Ring Interconnect	Ratio is the frequency multiplier; bin is a frequency step. Ring is the interconnect and associated cache. Max. Cache Ratio sets a ceiling; Ring Down Bin allows reductions according to operating conditions.
ABT	Intel Adaptive Boost Technology	A mechanism for increasing multithreaded performance when operating conditions provide headroom. It is not the same as the maximum frequency of preferred cores with a small number of threads.
TBM 3.0	Intel Turbo Boost Max Technology 3.0	Uses preferred cores capable of higher frequencies. Their stability is checked with lightly threaded loads, which a heavy all-core test cannot replace.
TVB	Intel Thermal Velocity Boost	A temperature-dependent boost mechanism. TVB Voltage Optimizations adjusts the voltage request with temperature, while Enhanced TVB concerns the temperature conditions of the frequency policy.
PL1 / PL2	Power Limit 1 / Power Limit 2	Processor power limits. They set limits, not required power consumption; equal PL1 and PL2 do not specify a later transition to a lower limit.
Tau / Dual Tau Boost	Power Averaging Time Window / Dual Tau Boost	Tau relates to power averaging, not an exact PL2 timer. Dual Tau Boost is a separate Tau management policy, not a way to disable the current limit.
ICCMAX / Unlimited ICCMAX	Maximum Current Limit / Unlimited ICCMAX	ICCMAX is the CPU current limit. On ASUS Z790, Unlimited ICCMAX permits a range above 511.75 A; it does not disable all protections and is not VRM Current Capability.
CEP	Current Excursion Protection	A response to a voltage drop below an internal threshold: Effective Clocks and performance may decrease without errors. Disabled in 9.2.1 is a benchmark exception that removes this protection, not daily-use advice.
IA / SA	Intel Architecture / System Agent	Labels for different processor domains in settings and telemetry. For example, IA CEP and SA CEP apply to different domains rather than duplicating a single setting.
MCE	ASUS MultiCore Enhancement	ASUS policy for multithreaded operation. Disabled - Enforce All Limits enforces the specified limits, but manual values do not automatically become Intel Defaults.
Thermal limit / Throttling	Temperature Limit / Performance Throttling	A temperature threshold triggers thermal throttling, which reduces performance. Power, current, and other limits can also cause throttling.
C-states / Speed Shift	Processor Idle States / Intel Speed Shift Technology	C-states are idle states; Speed Shift / HWP provides hardware control of active P-states. Disabling HWP does not disable C-states or fix the frequency.
UVP	Undervolt Protection	Protection against software lowering voltage below the boot-time level. Disabling it is not a prerequisite for tuning voltage through BIOS.
EIST / HWP	Enhanced Intel SpeedStep / Hardware P-states	EIST manages operating states through the OS; HWP makes hardware selections within OS policy. They are disabled conditionally in 9.2.1: check whether Turbo depends on EIST.
Thermal Monitor / THRMTRIP	Thermal Monitor / Thermal Trip	Thermal Monitor reduces power to control CPU temperature; it is enabled in 9.2.1. THRMTRIP is an independent emergency shutdown, not a replacement for normal thermal protection.
C1E / Enhanced C-states	Enhanced C1 State	Enhanced C1. Author observation: Apex Encore / BIOS 2202 / ASUS Advanced OC Profile locks this field Enabled. CPU C-states is separate; the field does not prove idle-state entry (9.3).

PROTECTION DOES NOT REPLACE OPERATING MARGIN

The temperature ceiling is not a target for daily use. Unlimited ICCMAX, Dual Tau Boost, VRM Current Capability, and CPU Current Reporting serve different functions; treating them as one way to bypass limits is incorrect.

DOCUMENTATION CONSULTED: Intel specifications and explanations.

Intel Datasheet, Intel CEP, Intel UVP, Intel Turbo Technologies

11

11.3 MEASUREMENT AND VALIDATION

Terms for reproducible tuning and validation. A successful test validates only the loads, clock speeds, and conditions actually tested, not every possible CPU workload. Click a term to open the relevant discussion.

Term	Full Name	Explanation
Baseline	Reference Configuration	A saved starting configuration with known settings and results. AC, offset, or manual-voltage steps are compared against it; return to it if unexplained deterioration occurs.
Vmin	Minimum Operating Voltage	The lowest voltage sufficient for stable operation under specified conditions. It is not a sensor Minimum or simply the current load voltage. The identified boundary needs margin and repeat testing (9.3.1).
Steady state	Steady-state Load	An established load condition useful for comparable measurements. It does not fully describe applying or removing a load, or exiting power-saving states.
Transient / Overshoot	Load Transient / Voltage Overshoot	A transient event when the load changes, with a possible brief voltage overshoot. A failure during a transition does not, by itself, prove that overshoot was the cause.
Effective Clocks	Core Effective Clocks	Effective clock speed over a measurement interval, accounting for core activity and sleep. Compare it with the regular clock speed, utilization, and the result of the same test.
Clock stretching	Clock Stretching	Reduced effective work execution despite an apparently high clock speed. A gap between Core Clocks and Effective Clocks alone does not prove CEP intervention, especially at idle.
Limit Reasons	Performance Limit Reasons	Flags indicating why operation is being limited. They help distinguish power, current, and temperature limits; a recorded maximum flag does not always describe the current moment under load.
WHEA	Windows Hardware Error Architecture	Windows hardware events: System → WHEA-Logger, during the run (5.3). Examine source/error type. WHEA does not automatically identify CPU cores; no events does not prove stability.
y-cruncher	Component Stress Tester	BKT, BBP, SFTv4, and SVT supplement CPU/cache validation; VT3 uses a large working set. Components and the run sequence are covered in detail in 5.4.
AVX / AVX2	Advanced Vector Extensions / Advanced Vector Extensions 2	Vector instruction sets that change the nature of the computational load. Passing a heavy AVX test does not validate stability at upper clock speeds in light or lightly threaded workloads.
Microcode	Processor Microcode	Internal fixes to processor behavior, distributed through BIOS among other channels. Record the version with the profile; repeat key checks after an update.
Cold boot / Sleep-wake	Cold Boot / Sleep and Wake	Starting from a powered-off state and transitioning from sleep to wake. Check that settings are applied consistently and that there are no hangs, reboots, or new errors after power-state changes.
Daily envelope	Daily-use Operating Envelope	The combination of allowed clock speeds, voltages, power, current, and temperatures for daily workloads. Assess it together with cooling, noise, and actual performance.
DC verification	DC Load-line Verification	Checking the applied DC against the LLC table (3.2) and checking the model in comparable operating modes (5.2). A single VID/VOUT match does not prove the entire configuration is correct.
Energy / task	Energy per Completed Task	Energy per correctly completed instance of the same task. Compare it alongside execution time and conditions; lower power due to reduced performance does not prove better efficiency.
Current / Minimum	Current / Minimum / Maximum	Current, lowest and highest readings since statistics were reset. Minima in different rows need not be simultaneous; without a reset they may come from idle (9.3.1).
IMC / RAM / DRAM	Integrated Memory Controller / Random Access Memory / Dynamic RAM	IMC is the CPU integrated memory controller; RAM is system memory, and DRAM is its dynamic type. An error in a combined CPU and memory test does not by itself identify the faulty component.

SEPARATE OBSERVATION FROM CONCLUSION

Record the test version and mode, duration, room temperature and result. Compare readings within the same load interval; Current, Minimum and Maximum are not interchangeable. Tests must cover heavy and lightly threaded loads, power-state transitions and real tasks.

DOCUMENTATION CONSULTED: explanations by the HWiNFO author; software and Windows documentation; Intel specifications and explanations.

HWiNFO: Effective Clock, y-cruncher, Intel Core Ultra 200S / DLVR

