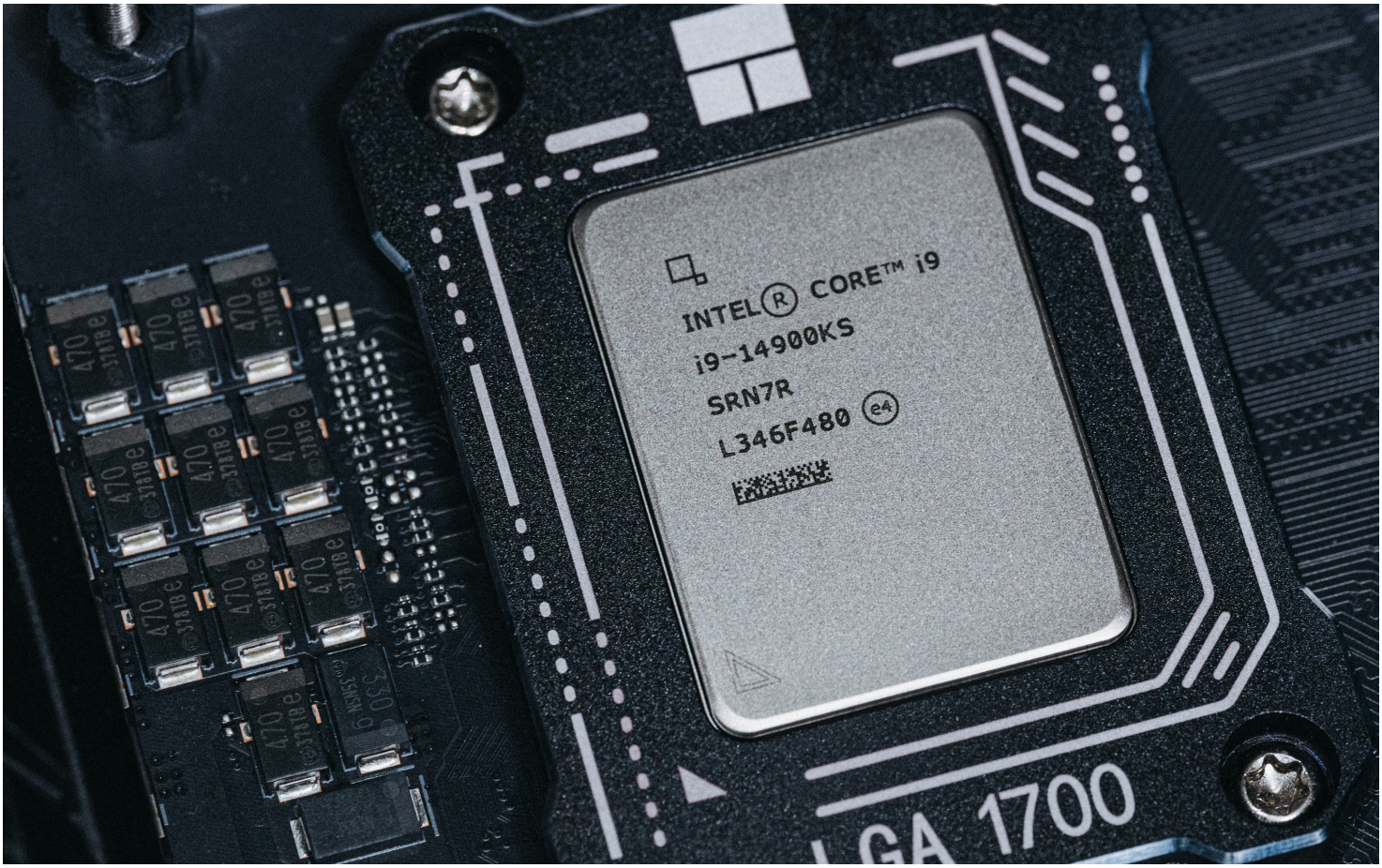
2026



ADAPTIVE TUNING AND OPTIMIZATION OF INTEL PROCESSORS LGA1700 / LGA1851

SVID / AC-DC LOAD-LINE / LLC / CLOCKS / LIMITS / STABILITY

ROG Maximus Z790 Apex (BIOS 3202)
ROG Maximus Z790 Apex Encore (BIOS 2202)
ROG Maximus Z890 Apex (BIOS 3402)

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A COMPLETE GUIDE TO TUNING AND OPTIMIZING INTEL PROCESSORS

MAXIM PAKHTUNOV / T.ME/PXTNV | T.ME/PXTECH | OCN | REDDIT

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01 / Introduction

For daily use on the Apex Encore with BIOS 2202, I chose undervolting through IA AC Load-Line. Lowering AC reduces the load-dependent addition to the voltage request while retaining dynamic clocks.

The method combines a selected LLC, matching DC Load-Line and individually tuned AC Load-Line. My example uses a Core i9-14900KS and ASUS ROG Maximus Z790 Apex Encore with LLC5; Chapter 7 contains the profile settings and supporting material.

This guide explains the parameters and tuning sequence. Find working values for your own CPU, accounting for the motherboard, BIOS and cooling.

First we examine the voltage request, VRM operation and sensor readings, then move to BIOS settings and testing. The calculation model, reference screenshots and author's profile each have their own conditions, stated alongside the example.

Test the working profile under heavy multithreaded load, at individual cores' peak boost, during load/idle transitions, after sleep and through repeated starts. Section 6.3 gives the full protocol.

Chapter 9 covers the Z890 Apex with a Core Ultra 7 270K Plus. P-cores, E-cores, Ring and the external supply are tuned in sequence with DLVR behavior taken into account.

The main part covers SVID control through IA AC Load-Line. Chapter 10 discusses three alternatives: SVID offset for adaptive undervolting, FIXED with a manual VRM target, and Auto SVID with limited Turbo ratios. Save a separate profile for each method and validate it in the required workloads.

The archived tests, text profile and BIOS recording show the original conditions of the author's example. Section 7.1 explains their provenance and later clarifications in the text.

> **BEFORE CHANGING SETTINGS**
>
> Tuning beyond the recommended configuration carries a risk of instability and data corruption. Back up important files, check cooling and prepare a BIOS recovery method in advance.

02 / Method and Starting Point

2.1 Method and Tuning Conditions

IA AC Load-Line allows voltage to be reduced while clocks remain dynamic. With LLC held constant, lowering AC reduces the load-dependent addition to the CPU voltage request. Match DC to the VRM load-line and keep it unchanged while tuning AC. Actual VRM Core Voltage and Global Core SVID Voltage remain on Auto in the main profile.

In the testing descriptions, per-core means a load on individual cores; load/idle means transitions between load and idle.

Retained	Tuned	Method scope
Adaptive voltage, Turbo and power saving	LLC, applied AC/DC values, finite PL and ICCMAX limits	Global Core SVID Offset and fixed Vcore are separate methods
CEP and thermal protection	AC, based on stability and performance results	Keep CEP and thermal protections enabled while tuning AC
Testing real usage scenarios	Margin from the identified stability boundary	Screenshots show individual operating modes; Section 6.3 lists the checks for a working profile.

Before You Begin

- Save the original BIOS profile and prepare a recovery procedure. Check baseline system operation with memory at its standard settings.
- For a new setup, use the latest stable BIOS for the motherboard. For affected Raptor Lake processors, Intel recommends microcode 0x12F or later; verify the actual version after boot.
- Test the system with Intel's recommended settings for this CPU. If errors persist with an up-to-date BIOS and standard memory settings, pause voltage tuning and diagnose the CPU, memory, motherboard and cooling. Send the logs to the system manufacturer, seller or Intel if failures recur.
- For individual AC tuning, save a separate comparison baseline with the chosen LLC/DC, frequency policy and power, current and temperature limits appropriate for the cooling. The ASUS Advanced OC Profile used in my example is selected separately from Intel Default Settings. Section 6.1 describes the AC = DC starting point and its checks.

WORKING EXAMPLE MATERIALS

The profile table records BIOS settings, while the reference screenshots show readings from individual runs. Sections 7.1–7.3 describe their conditions and provenance.

Working Example

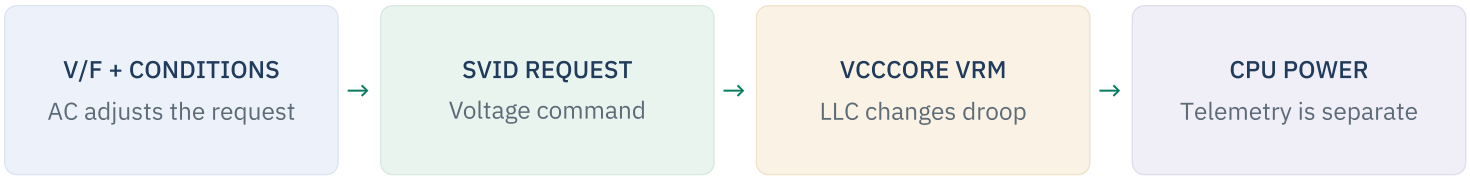
Core i9-14900KS, 8P+16E, Hyper-Threading Disabled, 24 threads; Apex Encore, BIOS 2202, LLC5. My profile uses HT Disabled; choose HT to suit your workload. Revalidate stability after changing HT, clocks, LLC, BIOS or limits.

Sources: Intel Vmin Update · APEX ENCORE BIOS · Intel UVP

03 / The Electrical Model

3.1 SVID, AC, DC and VRM Output

On LGA1700, the shared VCCCORE rail supplies the P/E-cores and Ring. Global Core SVID Voltage adjusts the core request, Cache SVID Voltage adjusts the Ring request, and Actual VRM Core Voltage controls the external regulator for that rail. After changing a request, check Vcore/VOUT, clocks and workload performance.



Element	Role in This Method
V/F and SVID	V/F defines the relationship between frequency and voltage. The CPU adjusts its operating request for load and temperature; SVID carries commands and data between the CPU and VRM.
IA AC Load Line	Changes the load-dependent addition to the voltage request. This method reduces AC to lower voltage.
CPU LLC	Changes the load-line characteristic of the VCCCORE VRM. Stronger compensation usually reduces steady-state droop, but changes transient response.
IA DC Load Line	Defines the load-droop model used by the CPU to account for voltage and power. Select DC to match LLC and keep it unchanged while tuning AC.
Core VID	A voltage value reported by the CPU. Section 6.2 explains how to read Core VIDs and compare them with measurements.
VOUT / Vcore	VOUT is a voltage reading from VRM telemetry; Vcore Die Sense is a separate motherboard measurement channel. Their agreement must be checked on the specific system.
CEP	When voltage falls below the internal threshold, the protection limits core activity. Assess its effect through performance and Effective Clocks (6.2).

AC, LLC AND DC TUNING SEQUENCE

Select LLC first and match DC to it. Then tune AC with the same limits and frequency policy. Repeat tuning after changing LLC, as this changes voltage droop and behavior during load transitions.

Sources: Intel VCCCORE · Intel CEP · HWiNFO: VID and DC Load-line · ASUS ROG Z790 BIOS Manual · Intel: Processor Power Rails

3.2 Calculating load droop

Steady-State Operation

Simplified Model of the External Rail

VOUT ≈ VSVID_command - IOUT × RVRM At steady load with an unchanged VRM command, voltage droop is IOUT × RVRM and increases with current.

In adaptive mode, the CPU changes the voltage command with frequency, temperature and load. To calculate load-line resistance from voltage and current differences, hold the command constant and let each measurement point settle.

Quantity	What the value represents	How to check it
DC = 0.73 mΩ	The DC value adopted for LLC5 from Table 4.2; also used in my profile	Measure the load-line and transient behavior on the VRM rail.
IOUT = 244 A	This Current reading is present in the screenshot	Use the current from the AC-compensation model in its calculation; 244 A is an illustrative assumption here.
Core VID ≈ VOUT	Readings are close in one operating condition	Compare logs from several operating modes with the applied AC/DC values; measure fast transients separately.
HWiNFO AC/DC	Readback of programmable parameters, when available	Compare the AC/DC readback with the selected BIOS values.

CALCULATION EXAMPLE: 93 mV

For this worked example, assume an AC-compensation current of 244 A with all other conditions held constant: 244 A × (0.73 - 0.35) mΩ = 92.72 mV. The difference illustrates the model at that current. Tune the working AC using the procedure in 6.1, comparing voltage and workload performance.

SETTING DC

- Select LLC and set the corresponding DC from Table 4.2. After boot, check the AC/DC values actually applied; Auto for DC is acceptable if readback shows the required table value.
- After changing LLC, set DC for the new level and retune AC. Hold DC constant while tuning AC or SVID offset, as it controls the power-accounting model.
- Keep CPU Current Reporting at 100%. The reported-current scale and DC model affect power accounting and can change clocks through the power limits.
- A software log is useful for comparing steady operating modes within the sensors' polling rate. Use measurement equipment to investigate fast voltage transients.

Sources: Intel VCCCORE · HWiNFO: VID and DC Load-line · HWiNFO: Effective Clock

04 / SVID and LLC Settings

4.1 Key BIOS Settings

The option names follow ASUS Z790 BIOS; the values come from my working example. Section 7.1 covers the profile's history. Submenu paths depend on the BIOS version.

BIOS setting	Value used in the guide	Purpose and checks
SVID Behavior	Auto	An ASUS policy for SVID settings. With manual AC/DC, check the applied values after boot; Section 7.1 explains the use of Auto in this profile.
CPU SVID Support	Enabled	Keeps SVID control and communication active.
Actual VRM Core Voltage	Auto	The external VRM follows the dynamic voltage request.
Global Core SVID Voltage	Auto	The core voltage request is controlled automatically; tune SVID offset in a separate series (10.1).
Cache SVID Voltage	Auto	Ring/Cache uses an automatic voltage request.
CPU Load-line Calibration	Level 5	LLC for the VCCCORE rail. After changing the level, set DC using Table 4.2 and repeat AC tuning.
Synch ACDC Loadline with VRM Loadline	Disabled	Automatic matching is disabled; still verify the selected AC/DC values after boot.
IA AC Load Line	0.35 mΩ	The value in my working profile; choose the initial AC separately for another sample.
IA DC Load Line	0.73 mΩ	The DC value adopted for LLC5 from Table 4.2; verify that it is applied after boot.
IA VR Voltage Limit	Auto	Sets VMAX for the IA VR in millivolts. Application depends on the CPU and BIOS; my profile uses Auto. After a change, check voltage under light load and during transitions using the procedure in 6.2.
Voltage Monitor	Die Sense	Voltage sensing at the CPU. On this board, Vcore is compared with VOUT; other boards must be checked separately.
UnderVolt Protection	Disabled in the export	For a new configuration, select Enabled and check that BIOS voltage settings are applied.

UVP DURING BIOS VOLTAGE TUNING

ASUS describes UVP Enabled as allowing voltage tuning through BIOS while limiting reductions from the operating system relative to the voltage established at boot. Check that BIOS undervolting is applied while retaining the existing VBS and HVCI settings.

The archived TXT dated 28 August 2026 contains SVID Behavior = Trained. Section 7.1 covers the later Auto recommendation and the original profile settings.

Sources: ASUS ROG Z790 BIOS Manual · Intel UVP · HWiNFO: VID and DC Load-line

4.2 LLC4, LLC5, LLC6 and LLC7

For my Z790 Apex Encore / BIOS 2202 example, I use the LLC/DC table: LLC5 corresponds to 0.73 mΩ and LLC6 to 0.49 mΩ. After boot, I check the applied DC and tune AC using 6.1. For another motherboard or BIOS, check the correspondence between its levels first.

LLC	DC, mΩ	Practical Behavior	What to Do with AC
Level 4	1,00	More droop than LLC5; different behavior during load transitions	Retune AC with the selected DC held constant.
Level 5	0,73	The level used in my main working example	My profile uses AC 0.35 mΩ. Tune AC individually for another sample.
Level 6	0,49	Less steady-state droop; different transient response	Retune AC and compare efficiency with LLC5 under the same workload.
Level 7	0,24	Stronger voltage-droop compensation; choose it based on load-transition testing.	Compare with LLC5. Once the lowest available AC is reached, tune any further offset in a separate series using 10.1.

Switching to Another Level

Save the Starting Point

Record LLC, AC/DC, voltage settings, limits and the result of the same workload.

Select LLC and Set DC

For LLC4/5/6/7, set DC to 1.00/0.73/0.49/0.24 mΩ, respectively. Disable Synch ACDC for independent AC control; verify after boot that the values have taken effect.

CHECK THE INITIAL AC

After changing LLC, set the reference AC = DC as described in 6.1. Check voltage and temperature under the baseline workload, then begin tuning AC.

Repeat Tuning and Testing

Compare voltage, power and performance. Test load transitions separately: the new LLC changes both steady-state droop and transient behavior.

> **TUNING AC**
>
> For each LLC level, find AC by reducing it in steps and testing as described in 6.1. LLC numbers identify a manufacturer's own modes; testing determines the working AC.

Sources: ASUS ROG Z790 BIOS Manual · Intel VCCCORE · ROG Forum: LLC / SVID

05 / Clocks, Limits and Protection

5.1 Clock Speeds, Turbo Boost and Power Saving

In my example, ratios are controlled automatically: ASUS Advanced OC Profile, ABT and the manual limits determine the available frequency range. Boost means an automatic frequency increase; all-core means a workload using all cores.

BIOS setting	Value	Practical meaning
Performance Core Ratio	Auto	The CPU and BIOS policy select the upper P-core ratios automatically.
Efficient Core Ratio	Auto	E-core ratios are selected automatically.
Min. / Max. CPU Cache Ratio	Auto / Auto	Ring/Cache operates dynamically. Test the ×50 maximum separately from the other operating modes.
Ring Down Bin	Enabled	Allows Ring to downclock under the relevant conditions.
Intel Adaptive Boost Technology	Enabled	Additional multithreaded boost when headroom is available. The two-core ×62 maximum belongs to a separate workload mode.
Turbo Boost Max Technology 3.0	Enabled	Uses preferred P-cores for high clock speeds with a small number of threads.
TVB Voltage Optimizations	Enabled	Adjusts the voltage request with temperature. Manual ratios are configured separately.
Enhanced TVB	Enabled	The temperature conditions for boost remain active.
Overclocking TVB	Auto	The BIOS controls TVB automatically.
AVX2 / Ratio Offset / Guardband	Enabled / Auto / Auto	AVX2 is enabled; Ratio Offset and Guardband remain on Auto.
SpeedStep / Speed Shift	Enabled / Enabled	Dynamic control of operating states is retained.
Enhanced C-states / CPU C-states	Enabled / Auto	C1E locked Enabled on the author's Apex Encore / BIOS 2202 / Advanced OC Profile; CPU C-states is separate (10.3).
Hyper-Threading	Disabled	My example uses 24 threads; choose HT to suit your workload.

> **TESTING PEAK BOOST**
>
> In the heavy-load screenshot, the P-cores run at about ×56–×57 and the E-cores at ×43. The ×62/×45/×50 maxima were recorded at other times. Test the upper ratios with a separate workload on one or a few cores (6.3).

If errors occur only at high boost on one or two P-cores, test those cores at the affected frequency step. Then adjust ratio or V/F separately while keeping DC unchanged. ABT controls multithreaded boost; test the ×62 maximum with a lightly threaded workload.

Sources: ASUS ROG Z790 BIOS Manual · Intel Turbo Technologies · Intel Core i9-14900KS

5.2 Power, Current, Temperature, and VRM

BIOS setting	In my profile	Meaning
ASUS MultiCore Enhancement	Disabled - Enforce All limits	Enforces the configured limits. The manual 320 W setting is the author's chosen limit; compare it with Intel Defaults separately.
Long / Short Duration Package Power Limit	320 / 320 W	PL1/PL2 set power limits; actual consumption depends on the workload and may be lower.
Package Power Time Window	56 s	Tau controls power averaging. With PL1 = PL2 = 320 W, long- and short-duration power control use the same limit.
CPU Core/Cache Current Limit Max.	400 A	The CPU's ICCMAX current limit. IOUT Maximum is the highest sample from slowly polled telemetry; assess these quantities separately.
Unlimited ICCMAX	Disabled	The configured ICCMAX is applied.
Dual Tau Boost	Disabled	The example uses the standard Tau policy; ICCMAX operates separately.
IA CEP / SA CEP	Enabled / Enabled	Protections for the respective domains are retained.
Maximum CPU Core Temperature / Thermal Monitor	100 °C / Enabled	100 °C is the temperature ceiling for this example. Leave margin below it for daily use.
CPU Current Reporting	100%	Keeps reported current at a 100% scale for power control.
Switch Microcode	Current Microcode	Uses the current BIOS microcode.

POWER CONFIGURATIONS IN THE INTEL DATASHEET

Processors	Datasheet configuration	PL1 / PL2	Tau	ICCMAX
13600K/KF, 14600K/KF	Standard, 125-W SKU	125 / 181 W	56 s	200 A
13700K/KF, 14700K/KF	Standard, 125-W SKU	125 / 253 W	56 s	307 A
13900K/KF, 14900K/KF	Standard, 125-W SKU	125 / 253 W	56 s	307 A
13900K/KF, 14900K/KF	Extreme Config	253 / 253 W	56 s	400 A
13900KS, 14900KS	Standard, 150-W SKU	253 / 253 W	56 s	307 A
13900KS, 14900KS	Extreme Config	320 / 320 W	56 s	400 A

The table lists power configurations from Intel's datasheet; the full Intel Default Settings profile includes additional parameters. SKU identifies a particular CPU model. I use Extreme for my 14900KS; for another CPU, take its initial limits from its documentation and match them to the cooling.

Secondary settings for my VRM

Setting	Value	Role in the method
CPU Current Capability	100%	An external VRM setting; configure CPU ICCMAX separately.
Switching Frequency / Duty / Phase	500 kHz / Extreme / Optimized	My sample's VRM settings; hold them constant while tuning AC.
CPU Power Thermal Control	125 °C	The VRM protection threshold; keep operating temperature below it.
CPU Input Voltage LLC	Level 2	Controls the separate CPU Input rail. Keep this setting unchanged while tuning IA AC LL; CPU LLC controls VCCCORE.

MONITORING POWER DELIVERY UNDER LOAD

Monitor voltage, temperature and performance in every working mode (6.2–6.3). IOUT Maximum = 259 A in the screenshot is the highest software sample with ICCMAX set to 400 A. Investigating fast current peaks requires a separate measurement.

Sources: Intel Datasheet · Intel VCCCORE · ASUS ROG Z790 BIOS Manual · Intel Vmin Update

06 / Tuning and Validation

6.1 AC Load-Line Tuning Procedure

Tune AC with LLC, DC, frequency settings and limits held constant. Validate the baseline CPU profile and memory first; then change one parameter at a time and compare performance with the baseline.

The aim of AC undervolting is to reduce voltage and energy use while retaining performance and correct computation. Compare test results, Effective Clocks and errors at each step. Section 6.2 explains CEP and how to read these indicators.

Record the baseline

Save the profile, BIOS/microcode version, HT, memory settings, limits, temperatures, and results of the selected tests. For a new system, first validate the recommended Intel configuration.

Choose operating limits

Choose PL1/PL2, ICCMAX and the temperature ceiling to suit the cooling. Keep them unchanged throughout AC tuning.

Choose a moderate LLC

My example uses Level 5. Section 4.2 covers LLC selection and changing levels.

Separate AC and DC

Disable Synch ACDC, set DC using Table 4.2, and check the applied AC/DC values after boot. Hold DC constant while tuning AC.

CHECK THE INITIAL AC

After selecting LLC and matching DC, set the reference AC = DC. Check voltage, temperature and baseline workload performance. Stop tuning and investigate the baseline configuration if errors, overheating or performance loss occur. Save the test result, Effective Clocks and VOUT, then reduce AC only.

Lower AC and compare results

Reduce AC by 0.02–0.05 mΩ per iteration. If errors or repeatable performance loss occur, return to the previous validated value and refine the threshold in 0.01–0.02 mΩ steps. These values specify the step size; testing determines the target AC. Check errors, WHEA, test performance and Effective Clocks at every step.

In my original example, I started at AC 0.40 mΩ and reduced it to 0.35–0.30 mΩ. Those values belong to that configuration; determine the starting point and lower threshold separately for another sample.

Separate the load types

Test warmed-up multithreaded workloads, peak boost on a cool system and load/idle transitions. Section 6.3 lists the full set of operating modes and the recording procedure.

Back away from the boundary and repeat

If an error or performance loss occurs, undo the last step. Keep the final AC above the boundary you found, with a margin confirmed by repeated testing in warm conditions.

Optimization criterion

Compare the same test, amount of work and warm-up phase. With performance unchanged, a gain appears as lower voltage, heat or energy per task; at the PL ceiling, it appears as better performance within the same power budget. Section 7.1 covers energy calculation and 6.3 covers stability testing.

When to return to the starting point

If errors persist after reverting AC or appear in another operating mode, check the CPU, Ring, IMC/memory and baseline stability separately. Establish the cause of the y-cruncher error before raising AC further.

Sources: ASUS ROG Z790 BIOS Manual · Intel Vmin Update · Intel UVP · Intel CEP

6.2 Monitoring and the Reference Operating Point

Sensor / metric	How to use it
Core VIDs	In the collapsed group, Current contains the mean of its cores' current VIDs. Expand the group to view individual cores and compare the same workload interval; Vcore is measured through a separate channel. See 10.3.1 for a detailed comparison.
VRM Vcore Voltage (VOUT)	Assess the output voltage of the corresponding VRM when a reliable telemetry channel is available.
Vcore / Die Sense	Compare with VOUT on this board. Account separately for differences in measurement points, accuracy, and polling.
VRM Vcore Current (IOUT)	Reports rail current at the telemetry polling rate. Investigating fast peaks requires a separate measurement.
CPU Package / IA Power	Package Power estimates whole-processor power; IA Power estimates the IA domain. Compare them with limits and clocks; POUT refers to a particular VRM rail.
Core Effective Clocks	Averaged clock speed accounting for core activity and sleep. Compare with the test result under a sustained, comparable load.
Limit Reasons / WHEA	Limit Reasons reports limiting conditions; WHEA records hardware errors. Also check computation errors and test performance.
CPU / VRM temperatures	Record current and maximum values, cooling conditions, and throttling flags.

y-cruncher screenshot: distinguish Current from Maximum

Metric	Current in the screenshot	Maximum over the interval
Core VIDs (aggregate)	1.278 V	1.472 V
Vcore / VRM VOUT	1.288 / 1.288 V	1.430 / 1.409 V
VRM IOUT	244 A	259 A
CPU Package Power	313.696 W	318.643 W
Core Max	75 °C	94 °C (summer)
VR VCC Temperature	53 °C	54 °C

The current samples give 1.288 V × 244 A ≈ 314.3 W; Package reports 313.7 W. This illustrates how the readings compare in that operating mode. Assess the DC model across several workloads, accounting for channel coverage and polling times. Each row accumulates its Maximum independently.

CHECKING CEP AND SENSOR READINGS

Effective Clocks account for core activity and pauses. They are naturally lower than Core Clocks at idle; under load, compare the gap with utilization and completed work. CEP responds to voltage droop and can reduce internal core activity. If performance falls after an AC reduction, revert the last step and check the limiting conditions. On the system shown, SVID POUT reaches 255 W and then remains at that level; also monitor power through Package and the available VRM telemetry. Fast voltage spikes require a separate measurement.

Sources: HWiNFO: VID and DC Load-line · HWiNFO: Effective Clock · Intel VCCCORE · Author screenshots

HOW TO READ LIMIT REASONS

Flag / group	Practical meaning	What to compare
IA: Max Turbo Limit	The Turbo ceiling for the current number of active cores has been reached. This can be a normal outcome of frequency control.	Current P/E/Ring clocks, active core count and performance; the active Turbo policy determines the available ratio.
PL1 / PL2 · Power Limit	The workload has reached the active power budget, and frequency adjusts to it.	Applied PL1/PL2, Package Power, duration and performance during the same workload interval.
CPU / VRM thermal limits	The CPU limits heat; the external VRM can also request throttling. Labels such as Thermal Throttling, PROCHOT and VR Thermal Alert depend on the platform.	CPU and VRM temperatures, current flags, cooling, and whether the event coincides with a frequency drop.
Current / EDP Other	A group of electrical limits with several possible causes, including ICCMAX, a VRM limit and motherboard power-delivery capability.	Identify the active flag and compare it with configured limits, current and clocks. Change the relevant limit once the cause is established.

I read flags over the same workload interval as clocks and performance. Current describes the present state; Yes in Maximum may remain from an earlier phase. I reset statistics before a controlled comparison. See Intel's Current/EDP guidance and the HWiNFO author's explanation of Max Turbo Limit.

Sources: Intel: Current / EDP · HWiNFO: Max Turbo Limit · ASUS ROG Z790 BIOS Manual

6.3 Stability Testing and Diagnostics

Test the profile with varied workloads and repeated runs. Record the program version and settings, component, instruction set, threads and core affinity, actual P/E/Ring and Effective Clocks, limits, temperature and cooling, duration, errors and the completed result. The attained clocks define what was tested; compare small gains with baseline variation.

Test scenario	What to check	Condition for proceeding
5-10 min after an AC step	Reproducible load and result, errors, and temperatures	Correct computation with performance retained
y-cruncher SVT + VT3	20-30 min: quick screening; 45-60 min: candidate; then longer tests of the required modes	Both tests complete correctly and active limits are recorded
OCCT / changing loads	Variable data sets and core cycling; separately, reproducible load/idle transitions	Cycles complete correctly with performance retained
Per-core / small thread counts	Each P-core, including preferred cores; peak clocks on a cool system with active limits recorded	Correct computation at the attained clocks
Idle, sleep/wake, boot	Power-state transitions and repeatable boot behavior	Transitions complete correctly and repeatably. Restore a validated setting if new WHEA events appear.
Real workloads and a warm room	Combined load, noise, heat, and expected performance	The profile meets the stated daily-use scenario

Quick diagnostics

Observation	Possible explanation	Next step
SVT / VT3 error	An error can originate in the cores, Ring, IMC, DRAM or power circuitry.	With validated memory unchanged, undo the last AC step and repeat
Error only at high boost	Lightly threaded workloads reach higher clocks than a heavy all-core load.	Test the affected cores and frequency steps with DC unchanged
Low Effective Clock	This is normal at idle; under load, it can have different causes	Compare the result, core activity, and limit reasons
Failure when the load is removed	A failure during a power-state transition; inspect the voltage waveform as the load is removed using hardware measurements.	Repeat transitions and restore the baseline; after changing LLC, recheck AC/DC
Unexpected change in Package Power	The DC model, limits, or a different frequency mode may be involved	Check the applied settings and repeat the same load

ADDITIONAL WORKLOADS AND ERROR LOGS

Cinebench tests rendering, while OCCT Variable changes data sets; run load/idle cycling separately. After a failure, open Event Viewer → Windows Logs → System, filter WHEA-Logger events for the test period and save the details. The event source and type help determine the next diagnostic step.

ADDITIONAL BKT, BBP AND SFTV4 TESTS

Run BKT, BBP and SFTv4 individually while monitoring current and CPU/VRM temperatures. BBP/SFTv4 may be heavier than VT3 on a particular CPU. If overheating occurs, stop the test, check cooling and reduce limits while retaining protections. Section 6.4 explains the components.

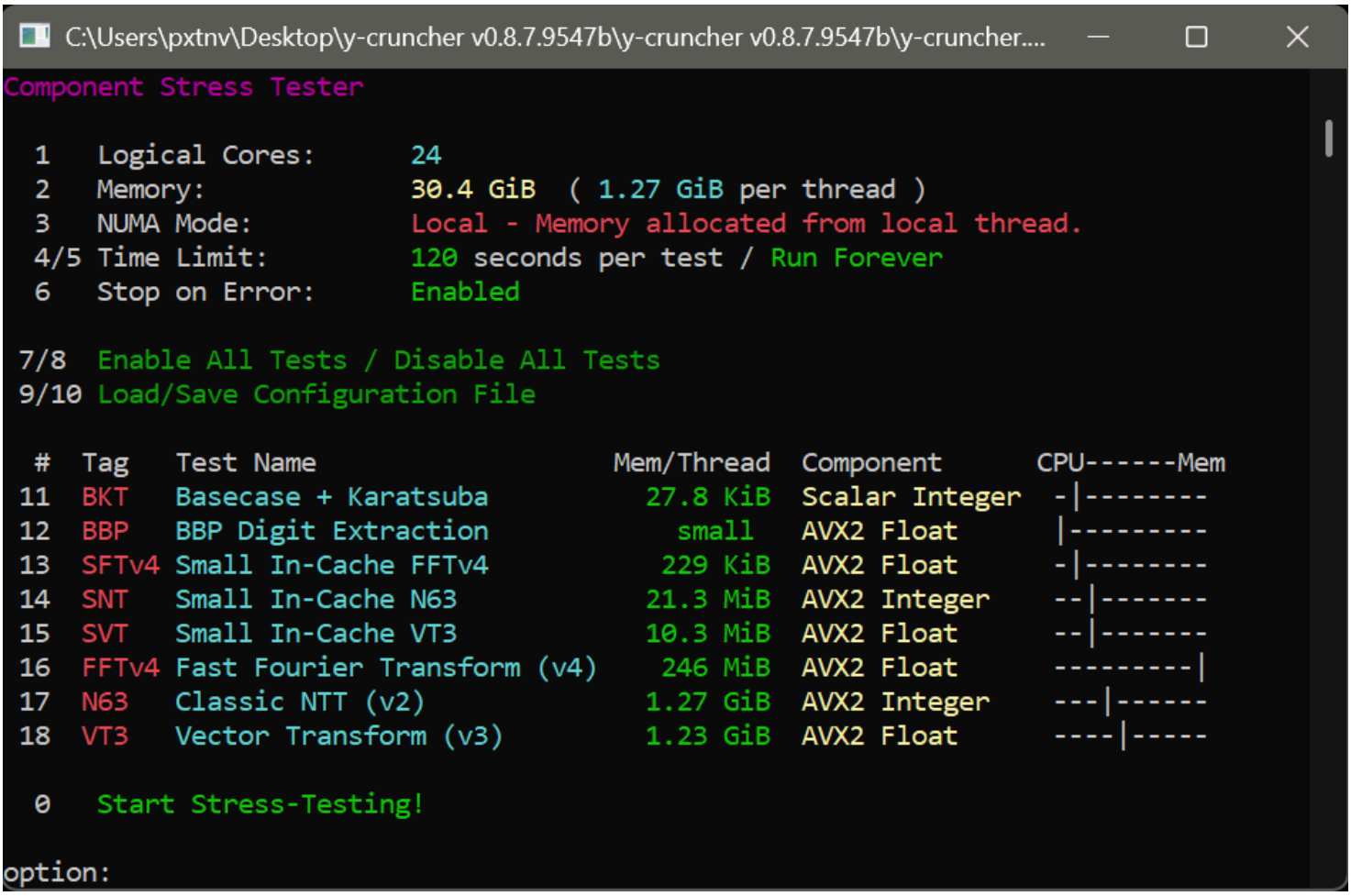
VOUT AND VDROOP AS CURRENT CHANGES

At higher current with an unchanged VRM command, droop increases; in adaptive mode, the CPU request also changes. Before changing LLC, compare VOUT, current, clocks, temperature and performance. Section 4.2 covers changing levels, and 6.4 covers workload components.

Sources: y-cruncher Version History · OCCT CPU · OCCT CPU + RAM · HWiNFO: Effective Clock · Microsoft WHEA

6.4 y-cruncher: Component Stress Tests

Component Stress Tester runs individual computational workloads; the π benchmark is a separate mode. The screenshot shows the Windows menu of y-cruncher 0.8.7.9547b. Record the version, executable, threads and memory: the executable selects the instruction set, with AVX2 used here. Mem/Thread reports memory per thread for each component.



A PRACTICAL STARTING POINT

- Logical Cores: the thread count of the profile being tested; here, HT Disabled, 24.
- Memory: for large tests, 80-90% of free RAM, leaving room for the OS, without paging.
- NUMA: Local for the standard configuration in this example.
- Time Limit: 60–120 s per component; total session duration is the sum of the component runs.
- Stop on Error: Enabled.

First select the required components; then choose 0 - Start Stress-Testing.

WHAT EACH COMPONENT DOES

Tag	Algorithm	Primary load	Role in CPU undervolting
BKT	Basecase + Karatsuba*	Scalar integer multiplication; small working set	Additional arithmetic coverage for the CPU
BBP	BBP Digit Extraction	Vector floating-point arithmetic, small working set	Tests CPU computation; use a different workload to test the full RAM allocation.
SFTv4	Small In-Cache FFTv4	Floating-point arithmetic; an in-cache fast Fourier transform (FFT)	CPU/cache and cooling; similar in focus to OCCT CPU
SNT	Small In-Cache N63	An in-cache integer number-theoretic transform (NTT)	Tests CPU/cache with a different type of math

Tag	Algorithm	Primary load	Role in CPU undervolting
SVT	Small In-Cache VT3	Small VT3: in-cache vector computation	Checks CPU/cache alongside the large VT3 test
FFTv4	Fast Fourier Transform v4	FFT with a large working set; dependent on RAM bandwidth	Mixed CPU/cache/IMC/RAM load
N63	Classic 64-bit NTT v2	64-bit integer NTT; large working set	An independent combined CPU and RAM load
VT3	Vector-Scalable Transform v3	Vector transform; large working set, CPU + IMC + RAM	Tests the profile under a mixed load; replacement for legacy VST

* The BKT name in Command Lines.txt includes Toom-Cook; the developer states that Toom-3 was removed.

HOW I COMPARE THE RESULTS

If SVT passes and VT3 fails, test the profile with a large data set: CPU/cache, Ring, IMC, RAM and power delivery. With validated memory, first revert the latest CPU change and rerun the test, then add an independent RAM check. Use the same sequence if both components fail.

RUN DURATION

For SVT + VT3, I use 20–30 minutes for screening and 45–60 minutes to test a candidate. If needed, I extend the run to 60–90 minutes to reach a thermal plateau. I start BKT/BBP/SFTv4 with short runs while monitoring heat, then test the other operating modes in 6.3.

Sources: y-cruncher release · y-cruncher Version History · y-cruncher FAQ · y-cruncher memory allocation

07 / BIOS 2202 Working Example

7.1 My Working Profile and Its Origins

My working example is a Core i9-14900KS on a Z790 Apex Encore with BIOS 2202. The table combines the original profile settings and later clarifications, with their provenance recorded in the relevant rows. Use the protocol below to keep measurement conditions consistent when comparing changes.

Setting	Value	Status / meaning
CPU / motherboard	14900KS / Apex Encore	BIOS 2202; ASUS Advanced OC Profile
P / E / Ring Ratio	Auto / Auto / Auto	P/E/Ring clocks follow dynamic control.
Hyper-Threading	Disabled	8P+16E, 24 threads; a fact about this example
SVID Behavior	Auto in the manual	The TXT dated 28 August 2026 contains Trained. Auto is a later recommendation in the guide; the archived runs used the original profile.
CPU LLC	Level 5	Selected VCCCORE VRM level
IA AC / DC Load Line	0.35 / 0.73 mΩ	AC is my result; DC is the table value for LLC5 (4.2)
Synch ACDC	Disabled	Independent AC tuning
Actual / Global Core / Cache Voltage	Auto / Auto / Auto	Dynamic voltage with the global offset left unset
PL1 / PL2	320 / 320 W	Selected Extreme operating envelope for the 14900KS
Tau / ICCMAX	56 s / 400 A	The author's profile limits. Section 6.2 covers current and transient measurements.
IA CEP / SA CEP	Enabled / Enabled	Protections remain enabled
UnderVolt Protection	Disabled in the export	Select Enabled for a new baseline configuration (4.1).
ABT / TBM 3.0	Enabled / Enabled	Dynamic frequency policy
TVB Voltage Opt. / Enhanced TVB	Enabled / Enabled	Temperature-dependent mechanisms are retained
CPU Current Reporting	100%	Unscaled current reporting
Ring Down Bin / Thermal Monitor	Enabled / Enabled	Ring can downclock; thermal protection is active

DAILY-USE PROFILE

This profile combines dynamic voltage with LLC5, a tuned AC, matching DC and active protections. Use the workloads in 6.3 to assess its operating range.

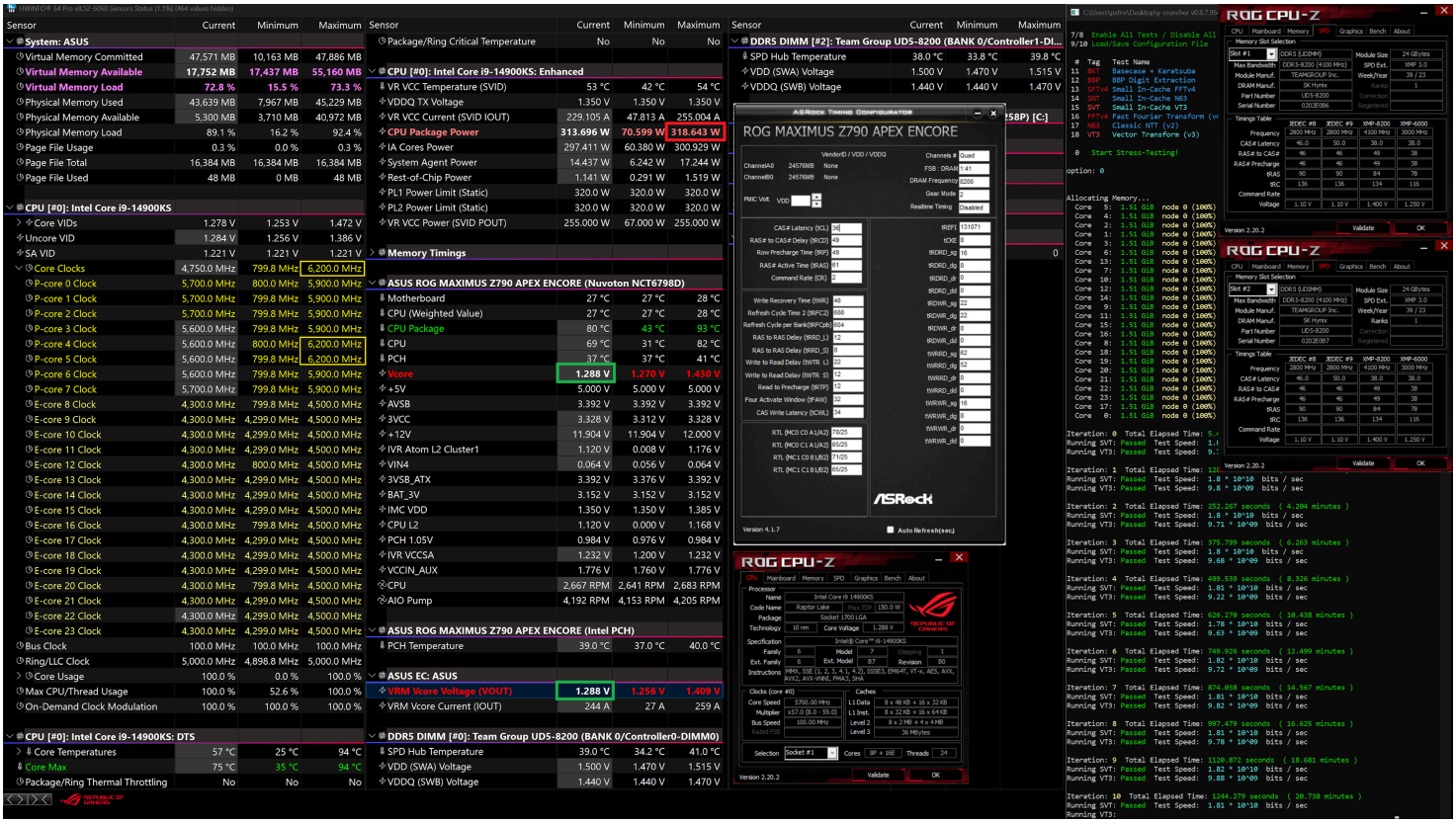
The TXT and video preserve the system's original state, including memory, OS and peripherals. Use the table's settings and explanations to tune the CPU; review other archived settings according to their purpose.

Sources: Author BIOS profile · Author screenshots · ASUS ROG Z790 BIOS Manual · Intel UVP

To compare two profiles, save logs of the same scenario with identical memory, HT, clocks or clock limits, cooling and measurement interval. Record performance and completion time, then calculate energy per task: E ≈ Pavg × t, where Pavg is mean power over the entire interval. Use the same channel for both configurations: Package for the processor, or a whole-system measurement.

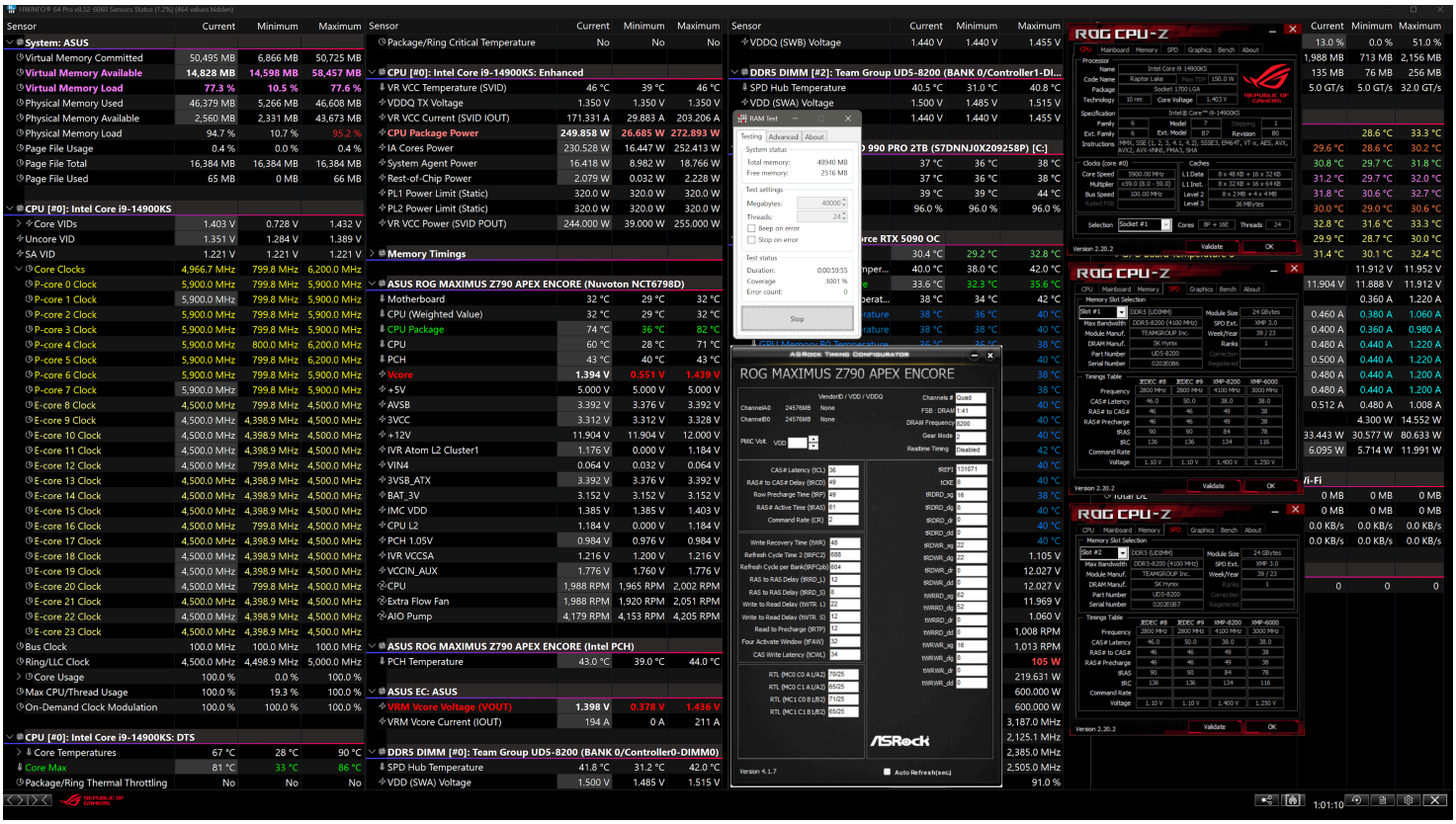
7.2 Reference Screenshots

The screenshots come from reference runs of the original profile. Click an image to open the original.



CPU: Y-CRUNCHER SVT / VT3

The frame records 20.738 minutes of testing. I separately reported a half-hour SVT/VT3 run.



RAM TEST: 3001%, 0 ERRORS

Ring in the screenshot: Current 4500 MHz (×45), Maximum 5000 MHz (×50). To test operation at ×50, track its frequency throughout the workload.

BIOS text profile: bit.ly/2202txt

7.3 BIOS 2202 Video Recording

My recording of the original daily-use BIOS profile settings.

Z790 APEX ENCORE + 14900KS | 48GB@8200-36 | DAILY USE [BIOS 2202]

WATCH THE RECORDING ON YOUTUBE youtu.be/Unt3nLivOZM

> **PROFILE ARCHIVE**
>
> The TXT and video show the original configuration. Section 7.1 explains the change in SVID Behavior from Trained to Auto.

08 / LGA1851 tuning

8.1 LGA1851: TUNING THE Z890 APEX WITH A CORE ULTRA 7 270K PLUS

The main example is an ASUS ROG Maximus Z890 Apex with a Core Ultra 7 270K Plus from the 200S Plus family. It has 8 P-cores, 16 E-cores and 24 threads, and supports up to DDR5-7200. The 5.5 GHz maximum is reached through Turbo Boost Max Technology 3.0 under suitable conditions. ASUS lists this CPU as compatible with the original Z890 Apex. Start with standard ratio control to test the operating points used in normal operation.

Choose limits and frequencies first, then record the baseline result. Tune offsets in sequence: P-cores → E-cores → Ring → external supply. Check performance and stability after each change.

For another motherboard, OEM system or SKU, check the available features, option names and limits. Table 8.1.3 lists separate configurations for neighboring models.

Sources: Intel: Core Ultra 7 270K Plus · ASUS: Z890 Apex CPU Support

8.1.1 DLVR POWER DELIVERY AND TRANSFERRING SETTINGS

In **DLVR Regulation** mode, the external VRM supplies the processor's internal regulators. Each P-core has its own regulation; E-cores are arranged in groups of four, and Ring has a separate voltage. The 270K Plus has four E-core clusters. The external rail is called VCCIA/VCore Input; Intel's electrical tables call it VCCCORE.



Distinguish these readings:

Reading	Meaning
Domain VID	Requested operating point of the P-cores, E-core cluster or Ring
DLVR Voltage	Available measurement of an internal domain
VR VOUT	Output voltage of the motherboard's external regulator

DLVR requires voltage headroom between its input and output, depending on load and control algorithms. DC tuning relies on the external rail's load-line and consistent measurements at the same power-delivery level.

Transfer the original Z790 settings as follows:

Original setting	Application to the Z890 Apex
LLC5 = 0.73 mΩ; LLC6 = 0.49 mΩ	Retain these as Z790 Apex Encore / BIOS 2202 data. Determine the Z890 correspondence separately.
AC tuning or a global offset	Start with separate P/E DLVR offsets
14900KS frequencies and limits	Replace with the installed Core Ultra's parameters
HT On/Off	Each physical core of the 270K Plus has one thread
Change log and load-transition checks	Retain in full

When comparing with a published profile, record its CPU, BIOS, clocks and cooling. A text export also helps check settings outside the screenshot.

> **REGULATION IN THIS PROCEDURE**
>
> This procedure uses Regulation Mode. Power Gate bypasses the internal regulators; switching to it requires separate power-delivery tuning.

Sources: ASUS E25061 · Falkentyne: Z890/DLVR measurements · Intel: Core Ultra 200S / DLVR · Intel: Raptor Lake VCCCORE

8.1.2 BASELINE BIOS CONFIGURATION

As checked on **29 October 2026**, the original Apex has **BIOS 3402**, released on 23 September, with **ME 19.0.11.2289v0.4**. ASUS recommends updating through EZ Flash; the ME version remains after a later BIOS rollback.

Save the current profile and text export, load **Optimized Defaults**, and select **Intel Default Settings → Performance**. Then explicitly set the limits in the next section.

Start with standard P/E/Ring/NGU/D2D frequencies and JEDEC memory or a separately validated memory profile. Keep AI Overclocking and Intel 200S Boost disabled. Record the frequencies applied on Auto: they depend on the CPU and firmware.

The main menu is **Advanced Mode → Extreme Tweaker**. Names follow ASUS manual E25061; use F9 to find an option in the installed BIOS.

BIOS option	Starting value
CPU DLVR Mode	Regulation Mode
Actual VRM Core Input Voltage	Auto
Performance Core DLVR Voltage	Auto
Efficient Core DLVR Voltage	Auto
Ring DLVR Voltage	Auto
DIGI + VRM → CPU Load-line Calibration	Auto
Internal CPU Power Management → IA AC Load Line / IA DC Load Line	Auto / Auto
CPU SVID Support; IA CEP Enable	Enabled
Unlimited ICCMAX	Disabled
Tweaker’s Paradise → UnderVolt Protection	Enabled

CPU SVID Support, IA CEP Enable and Unlimited ICCMAX are in Internal CPU Power Management. These are the starting settings chosen for this procedure.

Record the initial SVID Behavior, Synch ACDC Loadline with VRM Loadline, Segment2 Loadline and Core Voltage Suspension settings. Keep them unchanged while tuning domain offsets.

UVP permits BIOS undervolting and restricts runtime undervolting in the operating system relative to the voltage established at boot.

Test the baseline with the workload you will use for comparison. If errors occur, stop voltage tuning and diagnose the baseline profile. Record air or coolant temperature and pump and fan speeds.

Record BIOS, ME, microcode and monitoring versions. The Intel Platform Performance Package uses Windows 11 25H2; keep software versions and APO/Binary Optimization states unchanged during comparisons.

Sources: ASUS: Z890 Apex BIOS · ASUS E25061 · Intel Platform Performance Package

8.1.3 POWER AND CURRENT LIMITS

For the first pass, use the explicitly defined control configuration:

CPU	PL1	PL2	Tau	ICCMAX
Core Ultra 7 270K Plus	125 W	250 W	56 s	347 A
Core Ultra 9 285K; Core Ultra 7 265K/KF	125 W	250 W	56 s	347 A
Core Ultra 5 245K/KF	125 W	159 W	56 s	242 A

PL1/PL2/Tau come from Intel's Recommended Value column. The ICCMAX values of 347 and 242 A are selected here as control limits using the maximum currents in the functional VCCCORE Performance specification. Before entering them, record the ICCMAX applied by the ASUS preset and monitor current and temperatures during testing. The same specification gives **IccMAX.App = 245 A** for the 270K Plus as its application-current parameter; this procedure uses an ICCMAX setting of 347 A.

Set these options in **Internal CPU Power Management**:

- **Long Duration Package Power Limit** — PL1;
- **Short Duration Package Power Limit** — PL2;
- **Package Power Time Window** — Tau;
- **CPU Core/Cache Current Limit Max.** — ICCMAX, in amperes.

CPU Current Capability sets the external VRM limit as a percentage. Tau controls power averaging; the duration of high power also depends on load history and other limits.

If the intended daily profile uses **PL1 = PL2 = 250 W** for the 270K Plus, choose that mode before taking baseline measurements. Recheck voltage tuning after changing limits. Also record the temperature limit and cooling configuration.

At the PL1 ceiling, undervolting can improve performance at the same power by freeing headroom for higher clocks. A series may therefore produce either lower temperatures for the same result or more completed work within the same power limit.

Sources: Intel 832586-007 · Intel: power specifications · Intel: VCCCORE DC specifications

8.1.4 TUNING P-CORE VOLTAGE

Use identical test, memory and cooling settings. Record scores or completion time, temperature, power and Effective Clocks.

Run the baseline test three times under identical conditions, then run it the same number of times with the selected offset. Compare results against the baseline variation.

First change:

1. **Performance Core DLVR Voltage → Offset Mode**.
2. **Offset Mode Sign → –**.
3. **Offset Voltage → 0.010 V**.
4. Save settings and reboot.

Enter a positive magnitude in the numeric field; select the sign separately. The 10 mV step is a search increment to validate on the individual sample.

After booting, check that the setting was retained, inspect available domain readings, and repeat the original workload. If the result remains acceptable, increase the magnitude of the negative offset in 10 mV steps.

If there is a computation error, WHEA event, freeze, restart or repeatable performance loss, reduce the magnitude of the negative offset. Back away from the identified threshold and test that margin with different workloads.

After the multithreaded test, check P-cores in sequence, light single-threaded tasks, idle and wake from sleep using the protocol in 6.3.

If readings and performance stay unchanged, check that the offset applied, and inspect the active profile and other corrections. External VOUT may stay unchanged because of other domains' requests; assess P-offset using P-core readings and completed work.

If the system stops at POST after a change, the Apex's **Safe Boot** button starts BIOS with temporary safe settings while retaining the entered values for editing. Restore the last working offset. **ReTry** repeats startup with the same settings for another POST attempt.

Sources: ASUS E25061 · ASUS E25943

8.1.5 E-CORES AND RING

Save the validated P-core profile. Repeat the procedure in **Efficient Core DLVR Voltage**, starting with a **–10 mV** offset. Test E-cores separately and together with P-cores.

On the 270K Plus, each E-core cluster shares one voltage across four cores. When tuning individually, test every core in the group and confirm membership using the installed CPU's topology.

Keep Ring on Auto until P/E tuning is complete. Tune it in a separate series through **Ring DLVR Voltage**, retaining the same Ring/NGU/D2D frequencies, memory and controller voltages.

In NeoLine's published 270K Plus + Apex settings, Adaptive mode and negative P/E offsets are combined with a positive Ring offset. The author identifies BIOS 9931 in the post containing the export. This is an overclock with raised frequencies and removed limits; its published results describe that particular system. The useful lesson for this method is the independent tuning of the domains.

If errors appear after a Ring change, restore the previous offset and rerun the workload. Resume tuning once the baseline is stable again.

Sources: ASUS E25061 · NeoLine: BIOS screenshots · NeoLine: profile context

8.1.6 INDIVIDUAL OFFSETS AND V/F

Move to a specific P-core, E-core cluster or frequency range after locating the limitation. A typical case is passing multithreaded workloads while one core errors at high single-threaded boost.

First reduce the magnitude of the global offset and confirm repeatability. Then use **Specific Performance Core**, **Specific Efficient Core** or the corresponding V/F offsets. Read the point frequencies again for the installed processor. Check field units: the global DLVR Offset is entered in volts, while V/F Point Offset is in millivolts; **0.010 V equals 10 mV**.

A manually specified Additional Turbo Mode Voltage in Adaptive mode is associated with OC Ratio. The resulting operating point depends on the factory curve, adjacent points and interpolation. Use offsets or V/F adjustments to lower the stock curve.

SkatterBencher #101 describes V/F tuning on a 270K Plus + Z890 Hero, where usable offsets differed across frequencies. Test each changed operating point separately on your own CPU.

When moving to V/F tuning, record any global corrections still applied. Change one point or one parameter per comparison, retaining the same frequencies and limits.

Sources: ASUS E25061 · SkatterBencher #101

8.1.7 EXTERNAL SUPPLY, LLC AND AC/DC

LLC determines the external VRM's load-line; AC affects operating voltage, while DC affects power estimation. Segment2 introduces a second part of the characteristic when used.

Tune the external supply after validating P/E/Ring. Save the profile and record LLC, AC/DC and voltage limits. For the first trial step, select **Actual VRM Core Input Voltage → Offset Mode**, sign **–**, magnitude **0.010 V**. After rebooting, compare external VOUT, domain voltages and performance. Hold LLC, AC/DC and Core Voltage Suspension constant; validate each step before proceeding.

The aim is to reduce losses while retaining DLVR regulation headroom. Test steady loads, sharp transitions, application launches and brief boost. Revert the last input-rail change if behavior deteriorates.

After tuning the external supply, supplement CPU Package Power with VRM POUT/IOUT and the task result. Measurement scope differs: the external IA rail supplies only part of the CPU package. Wall power covers the whole system, including PSU losses.

On Quasarzone, godrepus initially reported **140 W** for a 270K Plus + Apex. In an update on 14 April, the author reported a rise to **190 W** after LLC/AC/DC adjustments, with the temperature unchanged. This observation shows why power-accounting settings must be considered when comparing profiles.

Use the same completed work, measurement channel and power-accounting settings for comparisons. Calculate energy using 7.1, and add temperature data and any available independent measurements.

Sources: ASUS E25061 · godrepus: power-reporting correction

8.1.8 NGU, D2D AND MEMORY

Tune Ring, NGU, D2D and memory separately. NGU/NoC relates to the SoC interconnect and System Agent supply; D2D connects the processor's tiles.

Intel lists a stock **D2D frequency of 3.0 GHz** for 200S Plus. Keep NGU on Auto and record the applied ratio. Intel's table lists 3.0 GHz for NGU, while SkatterBencher #101 reports 2.6 GHz; use the actual readback for your system.

Reports from 270K Plus + Apex owners show variation:

System	Published result
jstewart0131, DDR5-8400	D2D 32×; reports 60,000% Karhu and 2 hours of VT3. DDR5-8600 produced errors
Motor_Attention1865, DDR5-8200	D2D 30×; describes one TM5 anta777 cycle, with VT3 testing planned

Keep standard clocks for the baseline. Validate interconnect overclocking on your own sample using the full protocol: these two reports use different workloads and test durations.

Intel 200S Boost permits NGU/D2D up to **3.2 GHz** and DDR5 up to **8000 MT/s** with one DIMM per channel. Profile boundaries are **VCCSA ≤ 1.20 V, VDD2 ≤ 1.4 V, and module VDD/VDDQ ≤ 1.4 V**. Achievable frequencies depend on the system.

If the working profile will use 200S Boost or manual memory overclocking, introduce it as a separate stage and retest it together with the CPU offsets. Restore the last changed parameter first if errors appear.

Sources: Intel 200S Boost · SkatterBencher #101 · jstewart0131: DDR5-8400 · Motor_Attention1865: DDR5-8200

8.1.9 VALIDATING RESULTS AND SAVING THE PROFILE

Save a complete HWiNFO log:

Group	Data
Clocks	Core Clocks, Core Effective Clocks, utilization of the loaded cores
Voltages	Domain VIDs, available DLVR channels, external VR VOUT
Power	CPU Package Power, available VRM IOUT/POUT
Limits	Temperatures, Performance Limit Reasons
Validation	Scores or completion time, calculation errors, new WHEA events and restarts

Record full sensor-group names. Falkentyne's work on a 285K QS and Z890 Apex, with the ASUS ROG team's involvement, describes a limited number of internal channels and a ground reference shared with the input supply, affecting accuracy under load. Check the available channels separately on the 270K Plus and compare modes under identical measurement conditions.

The monitoring version also matters: HWiNFO 8.52 corrected NGU reporting.

If performance falls, compare Effective Clocks, utilization and limiting conditions using 6.2, then revert the last offset change and rerun the test.

Observation	Action
Performance retained, temperature or power lower	Continue testing other workloads
Same power, better performance	Check use of headroom within the chosen limits
Lower score at similar Core Clocks	Revert the last step; inspect Effective Clocks, utilization and limit reasons
Error on one core or at idle	Reduce the global offset magnitude, then locate the affected operating point
Memory-test error after a CPU change	Restore the last CPU offset and repeat the test
Errors remain at the original offsets	Check baseline configuration, memory and interconnects

Compare equivalent test phases. Record boost after idle separately from a sustained warmed-up workload. For small gains, repeat the original profile after the candidate to assess heating and background-process effects.

Use a repeatable benchmark for an initial comparison, followed by a CPU computation test and core cycling in OCCT. After changing memory or interconnects, add VT3 and a memory test; record each run's conditions as described in 6.3.

Chapter 6 lists the workloads. On LGA1851, test P-cores and E-core clusters separately after mapping logical processor numbers to the CPU topology. The final profile also goes through warm-up, cold startup, reboot, sleep and normal daily tasks.

Save the BIOS profile, text export, sensor log and results. Document the CPU, BIOS/ME/microcode, limits, DLVR mode, external settings, P/E/Ring offsets, frequencies, memory and cooling.

When tuning through TurboV Core, check that values survive a reboot: ASUS documents dependencies between voltage persistence, the selected profile and BIOS options.

Accept a working profile after repeatable checks show retained or improved performance. Updating BIOS or changing frequencies, limits, memory or the external supply requires revalidating the chosen offsets.

Sources: Falkentyne: Z890/DLVR measurements · HWiNFO: version history · ASUS TurboV Core FAQ

09 / Software and Links

9.1 Software: Websites and Guides

Record the program version and settings for each test. The official sites, guides and available versions below were checked on 29 October 2026; versions in archived screenshots belong to earlier runs.

HWINFO 8.54

Log sensor readings: VR VOUT / IOUT where available, VID, Effective Clock, temperature and limit flags. Save the log from each validation run.

Official download In the manual: 6.2

CPU-Z 3.01

Check the CPU model, clocks, ratios, core count and thread count. Save a configuration snapshot for the report, and validate stability with separate workloads.

Official site In the manual: 6.2

Y-CRUNCHER 0.8.7.9547b

Component Stress Tester: SVT/VT3 plus BKT, BBP and SFTv4. Record the version, executable, threads, memory and duration. Compare load intensity on the specific system; use separate diagnostics to establish the source of an error.

Official site and download FAQ and troubleshooting In the manual: 6.4

OCCT 17.1.10

CPU and CPU + RAM testing with recorded test settings. Variable changes data sets; use separate scenarios for core cycling and load/idle transitions.

Official download CPU guide In the manual: 6.3

CINEBENCH 2026.1.3

Compare rendering performance, temperature and sustained clocks using the same version and conditions. Supplement a successful run with stability checks under other workloads.

Official Maxon download In the manual: 6.3 Release notes

KARHU RAM TEST 1.1.0.0

Memory testing after CPU / Ring tuning. Record allocation, duration, coverage and errors. Version 1.1.0.0 is taken from the developer's public README; record the installed program version in your test log.

Official site In the manual: 7.2 Developer README

CORECYCLER 0.11.0.3

Additional sequential loading of individual cores; the official project supports Intel Active-Core Turbo. On a hybrid CPU, check P/E-core and HT affinity and test engine compatibility, and leave automatic voltage adjustment disabled.

Official repository Latest release In the manual: 6.3

10 / Alternative Tuning Methods

10.1 SVID OFFSET UNDERVOLT

On LGA1700 / ASUS Z790, tune a negative SVID offset after selecting LLC, AC/DC and SVID Behavior. If AC is already tuned, keep its validated value and change only the offset, comparing voltage and performance after each step.

> **ADAPTIVE OFFSET FOR DAILY USE**
>
> When choosing between SVID offset and FIXED for daily use, I try SVID offset first. It retains a dynamic voltage request; FIXED sets a manual VRM target. Compare the methods on the same workload using the energy protocol in 7.1.

BIOS setting	Starting setting	Purpose / limitation
Global Core SVID Voltage	Adaptive Mode	Adjusts the CPU request; a separate setting controls the manual VRM output.
Offset Mode Sign / Offset Voltage	"-" sign; magnitude set separately	Test the baseline before applying an offset; 0.010 V = 10 mV
Actual VRM Core Voltage / Cache SVID Voltage	Auto / Auto	Retain automatic VRM control and an automatic Ring request.
Additional Turbo Mode CPU Core Voltage	Auto	Keep Auto while tuning the offset.
CPU Load-line Calibration	Choose and hold constant	Use a validated level; choose LLC6 based on your own tuning results.
SVID Behavior	Chosen baseline	Auto or another previously validated Behavior
IA AC Load Line	Auto or manual AC	Select before tuning the offset and hold constant.
IA DC Load Line	Match to LLC: Table 4.2	Selected according to LLC independently of AC; used in the power-accounting model. Verification — 6.2
Limits / CEP / UVP	As in the main method	Finite PL/ICCMAX; protections enabled (5.2)

Tuning sequence: baseline first, then offset

- Save the profile and record the BIOS/microcode, clocks, memory and results. Before tuning offset, hold LLC, SVID Behavior and AC/DC constant. For independent manual AC/DC, set Synch ACDC to Disabled; verify the applied values after boot.
- Validate the baseline before applying a global offset, with finite limits and active protections. Use a manual AC from a previously validated profile with stability margin. Restore a working baseline first if errors or performance loss occur.
- Change only the offset in 5–10 mV steps, saving BIOS settings and rebooting. Compare VID, VOUT, Effective Clocks and performance under the same workload. If behavior worsens, revert the step and leave margin.

- Validate the final offset using 6.3–6.4. After changing LLC, AC/DC, Behavior, Synch or BIOS, repeat the baseline measurement first, then validate the offset.

> **SELECTING SVID BEHAVIOR**
>
> Select Behavior before tuning the offset: Auto or a previously validated Trained setting. After changing Behavior, read back AC/DC and compare voltage and performance again. Auto in the AC and Behavior fields controls different settings.

On the shared LGA1700 rail, P/E-core and Ring requests depend on their own V/F curves. Check the response in each workload mode and keep UVP Enabled. Section 8.1 covers individual domain tuning on LGA1851.

Compare energy for the same completed work and performance using 7.1. Then validate the selected offset using 6.3.

Sources: ASUS ROG Z790 BIOS Manual · Intel VCCCORE · Intel FSP: V/F and offset · Intel UVP · Intel: tuning and validation · ASUS: SVID Behavior Auto

10.2 FIXED: Manual Voltage

My FIXED starting configuration: LGA1700, 14900KS, ASUS ROG Maximus Z790 Apex Encore / BIOS 2202; LLC6, P/E/Ring 5800/4500/5000, 1.35 V, HT Off. The table below sets out how to test this configuration. For your own sample, first choose clocks, HT and limits to suit the workload.

FIXED sets a manual VRM target; clocks are controlled separately. At steady load: VOUT ≈ VOverride - IOUT × RLL, where RLL is the load-line slope. With a 1.350 V target, actual VOUT varies with current and LLC; test load/idle transitions separately.

F7: E = Extreme Tweaker; D = E > Digi+ VRM; I = E > Internal CPU Power Management; T = E > Tweaker's Paradise. C = Advanced > CPU Configuration; A = C > CPU - Power Management Control. Tau = Package Power Time Window.

BIOS setting / path	LLC6: main branch	LLC5: separate trial
D: CPU Load-line Calibration	Level 6	Level 5
I: IA AC Load Line / IA DC Load Line	0.49 / 0.49 mΩ	0.73 / 0.73 mΩ
D: Synch ACDC Loadline with VRM Loadline	Disabled	Disabled
E: Actual VRM Core Voltage > CPU Core Voltage Override	Manual Mode / 1.350 V	Manual Mode / 1.350 V
E: SVID Behavior / I: CPU SVID Support	Auto / Enabled	Auto / Enabled
E: Global Core SVID Voltage / Cache SVID Voltage	Auto / Auto	Auto / Auto
E: Performance / Efficient Core Ratio; ALL-Core Ratio Limit	Sync All Cores; 58 / 45	Sync All Cores; 58 / 45
E: Min./Max. CPU Cache Ratio; Ring Down Bin	Auto / 50; Enabled	Auto / 50; Enabled
E: ASUS MultiCore Enhancement	Disabled - Enforce All limits	Disabled - Enforce All limits
I: Long / Short Duration Package Power Limit; Tau	253 / 253 W; 56 s	253 / 253 W; 56 s
I: CPU Core/Cache Current Limit Max.; Unlimited ICCMAX	307 A; Disabled	307 A; Disabled

BIOS setting / path	LLC6: main branch	LLC5: separate trial
I: IA CEP / SA CEP; T: UnderVolt Protection	Enabled (all)	Enabled (all)
I: Maximum CPU Core Temperature; D: CPU Current Reporting	90 °C; 100%	90 °C; 100%
D: CPU Voltage Suspension; C: Hyper-Threading	Disabled (both)	Disabled (both)
A: CPU C-states / Thermal Monitor	Enabled / Enabled	Enabled / Enabled

This trial uses AC = DC, limits of 253 W / 307 A / 90 °C, and a Ring ceiling of 50. DC matches LLC according to Table 4.2; AC = DC is the reference configuration for this trial. When comparing with SVID offset, keep clocks, HT, memory, limits and cooling identical.

Sequence: LLC6 first, then a separate LLC5 branch

1. Save the profile; use BCLK 100 MHz and keep memory settings unchanged. ABT and Overclocking TVB = Disabled; V/F, per-core offsets, CPU Core/Cache Boot Voltage = Auto. Enter the LLC6 column settings, press F10 and reboot; verify AC/DC, ratios, HT and limits.
2. Use a short workload to check VOUT/IOUT and temperature. Then validate the stability of the profile with Override set to 1.350 V using 6.3–6.4. If errors or unexplained performance loss occur, pause the reduction and check the baseline configuration first.
3. Reduce Override in 0.005 V steps, comparing VOUT/IOUT, temperature, Effective Clocks and performance in the same test. If errors or performance loss occur, revert the last step and check active limits. Leave margin in the working setting.
4. For LLC5, restore Override to 1.350 V and set LLC/AC/DC using the table. At the same target and current, LLC5 produces more Vdroop than LLC6; compare measured VOUT. If it fails, return to LLC6 or lower clocks and repeat the trial.
5. Validate each branch using 6.3–6.4, including warm-up, load/idle and sleep/wake. Results apply to the clocks attained under load. To validate 58/45/50, track whether those clocks are maintained throughout the test.

> **CHECKING FIXED UNDER LOAD**
>
> Keep DC matched to LLC and check Package Power alongside limit behavior (6.2). With CEP Enabled, compare performance after each reduction in Override: the protection can limit internal core activity. Keep protections enabled and test steady loads and transitions using 6.3. The Z890 / DLVR procedure is covered separately in 8.1.

Sources: ASUS ROG Z790 BIOS Manual · Intel Datasheet · Intel VCCCORE · Intel CEP · HWiNFO: VID and DC Load-line · Intel: tuning and validation

10.2.1 FIXED: Benchmark Tuning

On LGA1700 / ASUS Z790, the profile in 10.2 can be tuned separately for a chosen benchmark. Save it as a separate profile and validate it at that test's clocks and workloads. Use the E/D/I/C/A menu paths defined in 10.2.

BIOS settings	What to change or check against the 10.2 baseline
E: Performance / Efficient Core Ratio; Min./Max. CPU Cache Ratio	Tune P/E and Ring for the test and cooling. Select Sync All Cores or By Core Usage to suit the workload; set ABT and Overclocking TVB to Disabled. Check actual Core / Effective Clocks and Ring, accounting for Ring Down Bin.
I: Long / Short Duration Package Power Limit; Package Power Time Window	When power-limited, raise PL1/PL2 while monitoring cooling. Keep Auto if the applied limits suit the test; MCE = Enabled - Remove All limits is a separate choice. Tau controls power averaging; with PL1 = PL2, both forms of control use the same limit.
I: CPU Core/Cache Current Limit Max.; Unlimited ICCMAX	When current-limited, tune ICCMAX while monitoring temperature and Limit Reasons. Unlimited ICCMAX = Enabled expands the available range; read back the applied limit after boot. CPU Current Capability separately controls the external VRM limit, while other protections retain their settings.
E: Actual VRM Core Voltage > CPU Core Voltage Override; D: CPU Load-line Calibration	Tune Override for benchmark performance while monitoring Vcore. This example uses LLC6 / DC 0.49 mΩ or LLC7 / DC 0.24 mΩ (4.2). LLC7 provides stronger droop compensation and increases overshoot risk; compare VOUT, heat and load transitions at each level.
C: Hyper-Threading / Active Efficient Cores; A: CPU C-states / SpeedStep / Speed Shift	HT = Enabled (ON) is the baseline: Cinebench Multi Core results are usually higher. Active Efficient Cores = All is the starting point for a multithreaded test; choose the active core configuration by results. CPU C-states = Enabled as in 10.2; change it in a separate trial. EIST / Speed Shift are covered below.
I: IA CEP / SA CEP; A: Thermal Monitor	Before a CEP trial, compare performance, Effective Clocks, VOUT and Limit Reasons using 6.2. The separate benchmark trial settings are listed below.

Related CPU features: benchmark FIXED only

BIOS setting	Value for benchmark FIXED
A: Intel SpeedStep (EIST)	Disabled *
A: Intel Speed Shift	Disabled
I: IA CEP Enable	Disabled
I: SA CEP Enable	Enabled; test Disabled separately
A: Thermal Monitor	Enabled
A: Turbo Mode	Enabled

In this trial, EIST / Speed Shift = Disabled limits dynamic P-state / HWP control. Monitor the clocks attained; restore Enabled for daily use. * If Turbo depends on EIST, keep EIST Enabled and check turbo-ratio.

With aggressive Vcore / load-line settings, IA CEP can reduce Effective Clocks while the application continues running. Disabled removes this protection’s limiting response.

I test SA CEP separately while keeping IA CEP and all other settings unchanged. Enabled is the starting choice; I retain Disabled only if it produces a repeatable gain in the selected benchmark. The effect depends on BIOS and workload. Disabling it removes System Agent protection; IA CEP protects its own domain and is assessed separately.

Keep Thermal Monitor Enabled: it limits power when the temperature threshold is reached. If it activates, reduce the load or improve cooling. THRMTRIP triggers an emergency shutdown at a critical temperature.

Brief procedure

1. Save the daily-use profile and a separate benchmark BIOS profile based on 10.2.
2. Choose the benchmark version and mode; hold memory, BCLK, OS/background activity, threads and cooling conditions constant.
3. Change one parameter at a time; when changing LLC, match DC to it while keeping the other conditions unchanged.
4. Compare 2–3 correctly completed runs by performance, Effective Clocks, temperature and Limit Reasons. Revert the last step if results deteriorate.
5. Save the best confirmed configuration separately; restore the daily-use profile after benchmarking.

> **BENCHMARK PROFILE LIMITS**
>
> Elevated voltage and current create risks of CPU degradation, crashes and data corruption even with good cooling. Back up important data before testing; revert the last step if errors, overheating or performance loss occur.

Sources: ASUS ROG Z790 BIOS Manual · Intel Datasheet · Intel CEP · Intel: tuning and validation · HWiNFO: Effective Clock

10.3 Auto SVID: Limiting Turbo Ratios

Auto SVID caps the upper P/E-core Turbo ratios while retaining automatic voltage control. Choose the frequency ceiling to suit the CPU and cooling, and leave Actual VRM Core Voltage and Global Core SVID Voltage on Auto. Turbo controls frequency within the selected range.

Reducing peak boost may lower the voltage request and heat together with performance in light and single-threaded tasks. To assess undervolting, compare measured voltage and performance at the original frequency.

My gaming profile: Core i9-14900KS + Z790 Apex Encore

This profile applies to the Apex Encore / BIOS 2202 with ASUS Advanced OC Profile. That mode sets motherboard policy; Intel Default Settings and AI Overclocking are selected separately.

Setting	Author's example
CPU profile	ASUS Advanced OC Profile
Performance Core Ratio / ALL-Core Ratio Limit	Sync All Cores / 58
Efficient Core Ratio / ALL-Core Ratio Limit	Sync All Cores / 45
Min./Max. CPU Cache Ratio / Ring Down Bin	Auto / 50 / Enabled
Hyper-Threading (HT)	Disabled - my gaming profile
Enhanced C-states (C1E)	Enabled - required state
CPU C-states	Disabled; Auto is a separate choice
Actual VRM Core Voltage / Global Core SVID Voltage	Auto / Auto
SVID Behavior	Auto
Manual offsets and V/F adjustments	Not set
CPU Load-line Calibration	Level 6
IA AC Load Line / IA DC Load Line	Auto / 0.49 mΩ
Synch ACDC Loadline with VRM Loadline	Disabled
PL1 / PL2 / CPU Core/Cache Current Limit Max.	320 W / 320 W / 400 A
Maximum CPU Core Temperature	100 °C is the limit; leave margin below it during operation.
Turbo Mode	Enabled

Choose HT for the workload with any method. In my experience, HT Enabled requires a lower Ring ratio and revalidation; the value is individual. Ring x50 is a ceiling: Ring Down Bin Enabled permits downclocking.

On the Apex Encore with BIOS 2202 and ASUS Advanced OC Profile, I observe C1E locked to Enabled. CPU C-states is selected separately: Auto or Disabled, as in this profile. Check actual idle-state use through residency readings; with Disabled, measure idle power. Compare gaming performance in a separate series.

The initial SVID Behavior is Auto. Trained uses ASUS predictions based on the CPU, clocks and LLC. For comparison, change only Behavior with the same P/E/Ring, HT and limits; read back AC/DC and repeat stability testing.

> **Preparation and validation**
>
> Load the saved baseline before changing methods; 10.3.1 covers restoration after benchmark FIXED. After boot, read back AC/DC, including AC Auto. This example uses LLC6 and DC 0.49 mΩ (4.2); 10.3.2 explains the screenshot readings.

Sources: ASUS Z790 E23196 · ASUS: CPU Profiles · Intel VCCCORE · SkatterBencher #53 · ASUS: SVID Behavior Auto · ASUS: Trained

10.3.1 Auto SVID: Validation Under Load

After benchmark FIXED, restore the baseline: CPU SVID Support, EIST/SpeedStep, HWP/Speed Shift, IA/SA CEP, UVP and Thermal Monitor = Enabled; Current Reporting = 100%, finite PL/ICCMAX, Unlimited ICCMAX = Disabled. Set Actual/Global/Cache and manual P/E voltages to Auto, clear manual offsets and V/F adjustments, and set Voltage Suspension to Disabled.

My procedure for comparing Vcore and VOUT

Record the settings

Remove previous ratio/OC TVB adjustments and set the limits from 10.3. Use the Turbo baseline in 5.1 for testing: ABT, TBM 3.0, TVB Voltage Optimizations and Enhanced TVB = Enabled; OC TVB = Auto. Record BIOS/microcode, AC/DC, LLC, Behavior, P/E/Ring, HT, limits and the test mode.

Wait for a steady load

Test Cinebench, the y-cruncher component and the OCCT mode separately. Save an HWiNFO log. After warm-up, compare a continuous interval with the same component running. Reset Min/Max after the load settles to record fresh minima.

Compare Vcore and VRM Vcore Voltage (VOUT)

On the Apex Encore / BIOS 2202, close Vcore and VOUT readings serve as a reference for comparison. Compare the same log interval, accounting for sensing locations, accuracy and polling. Each sensor's Minimum retains its own lowest sample.

Check results and repeatability

Validate the profile using 6.3–6.4: computation, WHEA, temperature, Effective Clocks, actual P/E/Ring, limits and performance. To test the selected ratios, track whether they are maintained under load. Compare small gains with baseline variation.

COMPARING CORE VIDS, VCORE AND VOUT

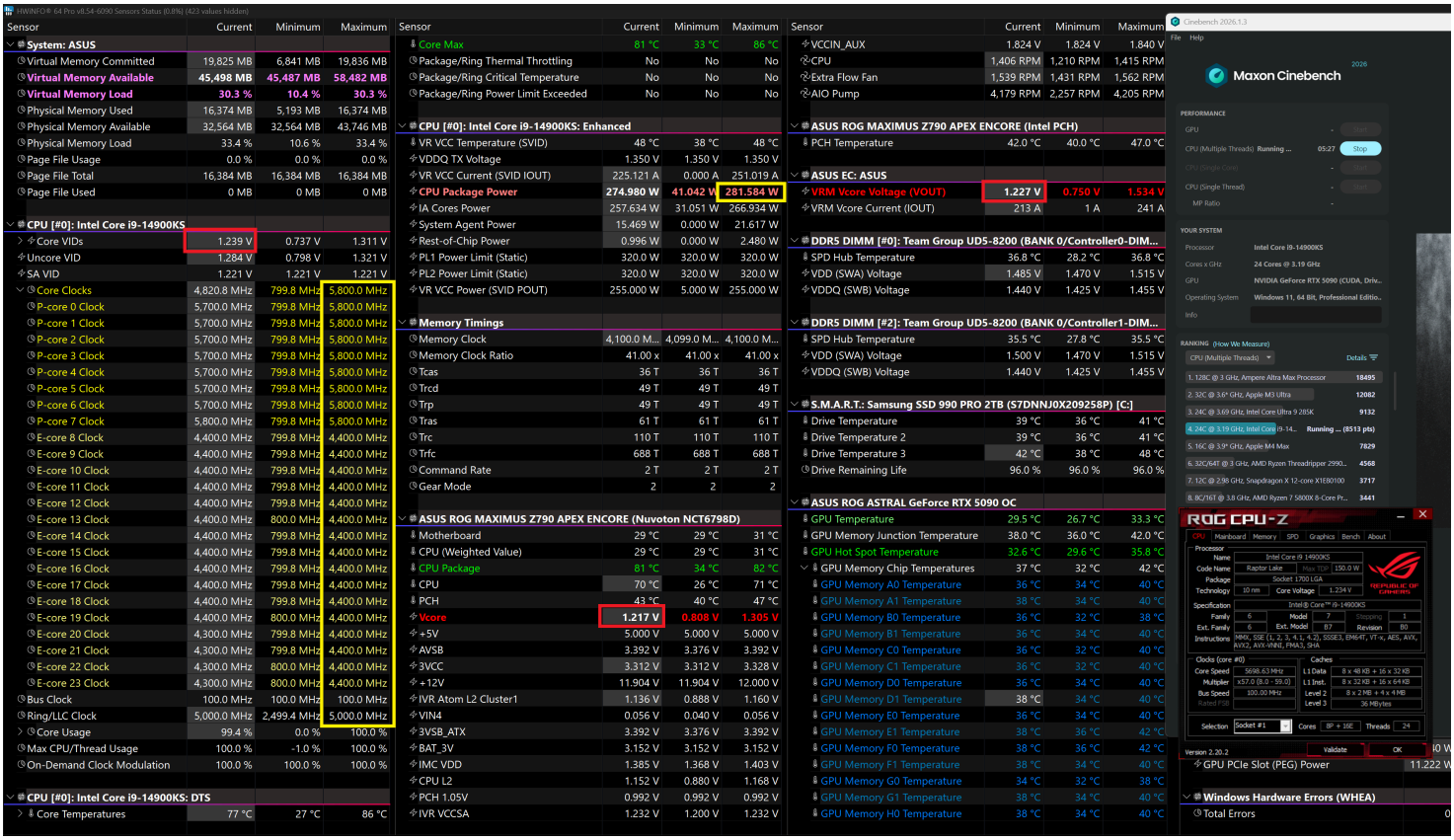
Expand Core VIDs and compare individual cores' current VIDs with Vcore/VOUT over the same workload interval. Section 6.2 explains the channels, mean Current and accumulated Minimum/Maximum.

Keep DC matched to LLC. Supplement the voltage comparison with power, clock and workload-performance checks using 6.2–6.3.

> **TUNING VOLTAGE WITH MARGIN ABOVE VMIN**
>
> Find the practical Vmin threshold by reducing voltage in steps and repeating tests at specified clocks, load and temperature. Leave margin for the working profile. Minimum in HWiNFO is the lowest sample recorded since statistics were reset; record it together with the workload mode.

Sources: HWiNFO: VID and DC Load-line · HWiNFO: VID / VOUT · Intel VCCCORE · Author screenshots

10.3.2 Auto SVID: Monitoring Example



Current in the screenshot: collapsed Core VIDs 1.239 V, Vcore 1.217 V and VOUT 1.227 V; the differences in this sample are 10 and 12 mV. Minimum includes idle. Maximum: VOUT 1.534 V, Vcore 1.305 V and Core VIDs 1.311 V. To investigate the VOUT maximum, save a log with workload phases marked and check the channel's accuracy; the rows accumulate their extrema independently. The E-core maximum in the frame is ×44, while the table in 10.3 specifies ×45. Cinebench is running when the frame is captured. Validation procedure. Open original.

11 / Documentation consulted

11.1 Documentation consulted

Intel and ASUS documentation describes platform parameters; software guides cover tests and measurements. Separate groups contain published community observations and the archive of my working example.

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12 / Glossary

12.1 Voltage and Power Delivery

The processor requests voltage, the VRM regulates power, and sensors provide monitoring readings. Click a term to open the detailed discussion.

Term	English name	Explanation
SVID	Serial Voltage Identification	The interface for commands and telemetry between the CPU and VRM. Section 3.1 explains its role in voltage control; 10.1 and 10.3 cover ASUS SVID Behavior policy.
VID / Core VID	Voltage Identification	A voltage value reported by the CPU. In the collapsed Core VIDs group, Current contains the mean of the cores' current VIDs. Sections 6.2 and 10.3.1 explain how to read it and compare it with Vcore/VOUT.
V/F	Voltage / Frequency	The voltage–frequency relationship used by adaptive control. The operating voltage request also depends on load, temperature and active adjustments.
AC LL	IA AC Load Line	A load-dependent adjustment to the voltage request. The main method reduces AC; when subsequently tuning a global offset, hold AC constant—see 10.1.
DC LL	IA DC Load Line	A droop-model parameter used for voltage and power accounting. In the LGA1700 example, match DC to LLC using 4.2; check the correspondence separately for the external LGA1851 rail (8.1.7).
LLC / Vdroop	Load-line Calibration / Voltage Droop	LLC changes the VRM load-line; Vdroop is the voltage drop as steady-state current rises. Test load transitions after changing LLC. In the main LGA1700 example, also retune AC.
VRM / VCCCORE	Voltage Regulator Module / Core Power Rail	The VRM converts power for the processor; on the LGA1700 platform considered here, VCCCORE is the shared P/E-core and Ring rail. Its voltage, current and power refer to that rail, while CPU Package covers the whole processor. On LGA1851 in Regulation Mode, the external rail supplies the DLVRs; its voltage differs from the internal domain voltages.
VOUT / Vcore	VRM Output Voltage / Core Voltage	VOUT is the voltage reported by VRM telemetry; Vcore is a separate motherboard sensing channel, Die Sense in this example. Compare the same workload interval, accounting for sensing locations and polling (10.3.1). On LGA1851, external VR VOUT describes the DLVR input supply; check domain voltages using their corresponding channels.

Term	English name	Explanation
IOUT / POUT	VRM Output Current / Power	The regulator output current and power reported by telemetry. Checking P ≈ U × I requires simultaneous readings from the same domain without sensor saturation.
Package / IA Power	CPU Package / IA Cores Power	Power estimates for the entire processor package and the IA domain. They cover different parts of the processor; power on an individual VRM rail can differ from Package Power.
Current Reporting	CPU Current Reporting	The scale applied to reported current; this guide uses 100%. Changing it affects current accounting and power control.
CPU Input Voltage LLC	CPU Input Voltage Load-line Calibration	In the LGA1700 profile used here, this adjusts the load-line characteristic of the separate auxiliary CPU Input rail. VCCCORE LLC is controlled separately. Do not equate this setting with Actual VRM Core Input Voltage on Z890, which controls the external DLVR supply.
Adaptive	Adaptive Voltage	A mode in which the voltage request changes with CPU operating conditions. The method in 10.1 retains adaptive control and applies a negative offset separately.
SVID offset	Global Core SVID Voltage Offset	In the LGA1700 example, an adjustment to the voltage request through Global Core SVID Voltage with a positive or negative sign; a negative value is used for undervolting. Evaluate the result using measured voltage and performance. AC LL and the VRM-side offset are adjusted separately. The LGA1851 procedure sets DLVR domain offsets and the external input-rail offset separately. See 10.1.
FIXED	Manual VRM Voltage / Voltage Override	In the method in 10.2, a mode for manually setting the Actual VRM Core Voltage target. Frequency and power saving depend on other settings, while the amount of Vdroop depends on the VRM load-line. Verify actual behavior through measurements.
DLVR	Digital Linear Voltage Regulator	Arrow Lake's internal digital linear voltage regulator. In Regulation Mode, the external supply passes through DLVR to the P/E/Ring domains; check input and domain voltages separately (8.1).
SVID Behavior	Auto / Trained	An ASUS policy for SVID settings: Auto selects parameters according to BIOS rules, while Trained uses predictions. After a change, read back AC/DC and compare operation under the same workload (10.3).
Regulation / Power Gate	DLVR Regulation / Power Gate Mode	Regulation uses internal DLVRs; Power Gate bypasses them. Bypass availability depends on the platform and firmware.

Term	English name	Explanation
Segment2 Loadline	Second Load-line Segment	A separate load-line characteristic above a configured current threshold.
Core Voltage Suspension	Voltage Floor / Ceiling Control	Control of voltage floors and ceilings, including temperature-dependent variants.
DLVR Offset / V/F Point Offset	Domain Offset / V/F Point Offset	DLVR Offset adjusts a selected domain; V/F Point Offset adjusts an individual curve point. Check the field's units.
VCCSA / VDD2	System Agent / Memory Controller Power Rails	VCCSA supplies the System Agent; VDD2 supplies the processor's memory controller. These are processor rails; DRAM VDD/VDDQ are memory-module voltages.

CHECKING THE TUNED POWER RAIL

In the main LGA1700 example, match LLC and DC first, then tune AC. Sections 3.1–3.2 cover the model, and 6.1 covers the tuning sequence. Use the separate procedure in 8.1 for LGA1851.

Sources: Intel VCCCORE · ASUS ROG Z790 BIOS Manual · HWiNFO: VID and DC Load-line

12.2 Clocks, Limits and Protection

Terms for frequency control, power and current limits, and protection. Compare BIOS settings with the actual reasons for limiting operation. Click a term to open the detailed discussion.

Term	English name	Explanation
P-core / E-core / HT	Performance Core / Efficient Core / Hyper-Threading	P-cores focus on high performance and E-cores on energy efficiency. On the LGA1700 platform covered here, HT lets a P-core run two threads. HT is disabled in the author's gaming profile; repeat CPU and Ring testing after changing it. The Core Ultra 7 270K Plus has 24 physical cores and 24 threads; the LGA1700 example's HT setting does not carry over.
Ratio / bin / Ring	Frequency Multiplier / Frequency Step / Ring Interconnect	Ratio is a frequency multiplier; bin is one frequency step. Ring denotes the ring interconnect and its associated cache. Max. Cache Ratio sets the upper Ring frequency limit, and Ring Down Bin permits reductions according to operating conditions. On LGA1851, Ring, NGU and D2D are separate clock domains.
ABT	Intel Adaptive Boost Technology	A mechanism that improves multithreaded performance when current, power and temperature limits allow headroom. The maximum frequency of preferred cores in lightly threaded workloads is considered separately.
TBM 3.0	Intel Turbo Boost Max Technology 3.0	A mechanism that uses preferred cores capable of higher frequencies. Validate their stability with lightly threaded workloads in addition to a heavy all-core test.

Term	English name	Explanation
TVB	Intel Thermal Velocity Boost	A boost mechanism that accounts for processor temperature. TVB Voltage Optimizations adjusts the voltage request with temperature; Enhanced TVB governs the temperature conditions for boosting frequency.
PL1 / PL2	Power Limit 1 / Power Limit 2	The processor's long- and short-duration power limits. With PL1 = PL2, both forms of control use the same value; actual consumption depends on the workload and other limits.
Tau / Dual Tau Boost	Power Averaging Time Constant / Dual Tau Boost	Tau is the time constant used to average power for PL1; time spent above PL1 also depends on the workload and prior power consumption. Dual Tau Boost is a separate Tau management policy under which the current limit remains in effect.
ICCMAX / Unlimited ICCMAX	Maximum Current Limit / Unlimited ICCMAX	ICCMAX sets the CPU current limit. On ASUS Z790, Unlimited ICCMAX permits values above 511.75 A; other protections retain their settings. CPU Current Capability controls the external VRM separately.
CEP	Current Excursion Protection	Protection against voltage falling below an internal threshold; it can reduce internal core activity and performance. Section 6.2 covers testing. Keep Enabled for daily use; 10.2.1 describes a separate benchmark trial with Disabled.
IA / SA	Intel Architecture / System Agent	Labels for different processor domains in settings and telemetry. IA CEP and SA CEP therefore control protection for their respective domains and are separate settings.
MCE	ASUS MultiCore Enhancement	An ASUS policy for multithreaded processor operation. Disabled - Enforce All Limits enforces the configured limits; manually entered values must be checked separately against Intel Defaults.
Thermal limit / Throttling	Temperature Limit / Performance Throttling	A temperature limit sets the threshold for thermal protection. Throttling is a reduction in performance caused by temperature, power, current or other limits.
C-states / Speed Shift	Processor Idle States / Intel Speed Shift Technology	C-states are processor idle states; Speed Shift / HWP controls active P-states in hardware. With HWP disabled, C-state control remains a separate setting and clock frequency can still vary.
UVP	Undervolt Protection	Protection that restricts software from lowering voltage below the level set at boot. BIOS voltage tuning can remain available with UVP enabled.

Term	English name	Explanation
EIST / HWP	Enhanced Intel SpeedStep / Hardware P-states	EIST lets the OS manage processor operating states; HWP selects them in hardware within OS policy. Before disabling them as described in 10.2.1, check whether Turbo depends on EIST.
Thermal Monitor / THRMTRIP	Thermal Monitor / Thermal Trip	Thermal Monitor controls temperature by reducing performance; it is enabled in 10.2.1. THRMTRIP provides an independent emergency shutdown alongside normal thermal protection.
C1E / Enhanced C-states	Enhanced C1 State	The enhanced C1 idle state. In the author's observation, Apex Encore with BIOS 2202 and ASUS Advanced OC Profile locks the field to Enabled. CPU C-states is a separate setting; actual idle-state entry must be checked from readings (10.3).
CPU Current Capability	External VRM Current Limit	The external VRM's current shut-off threshold, expressed as a percentage. It is separate from ICCMAX.
NGU / NoC	Next Generation Uncore / Network on Chip	NGU includes the SoC interconnects; the NoC connects its components. On Arrow Lake, NGU Ratio adjusts this interconnect separately from Ring and D2D.
D2D	Die-to-Die Interconnect	The interconnect between processor tiles. Check and tune its clock separately from Ring and NGU.
E-cluster	Efficient-core Cluster	A group of E-cores sharing domain-voltage control. In the 270K Plus used here, each cluster contains four cores; validate the entire group.
IccMAX.App / FVM	Application Current / Fast V-Mode	IccMAX.App is the expected maximum current of a real PL4 workload with Fast V-Mode enabled. It is distinct from IccMAX and does not automatically replace the BIOS limit.
Intel 200S Boost	Intel 200S Boost Overclocking Profile	An NGU, D2D and memory overclocking profile for compatible Core Ultra and Z890 systems. Check its limits and attainable clocks separately from core-voltage tuning.

> **Protection and daily operating margin**
>
> Daily operation requires margin below the temperature limit. Unlimited ICCMAX, Dual Tau Boost, VRM Current Capability and CPU Current Reporting serve different functions; assess each setting separately.

Sources: Intel Datasheet · Intel CEP · Intel UVP · Intel Turbo Technologies

12.3 Measurement and Validation

Terms for measurement and profile validation. Record the workload, actual clocks and conditions for every run. Click a term to open its detailed explanation.

Term	English name	Explanation
Baseline	Reference Configuration	A saved starting configuration with known settings and results. Compare AC, offset or manual-voltage changes against it, and return to it if unexplained deterioration occurs.
Vmin	Minimum Operating Voltage	The lowest stable operating voltage at specified clocks, workload and temperature. Find the threshold through repeated tests and leave margin in the working profile (10.3.1).
Steady state	Steady-state Load	A steady load condition suitable for comparing measurements. Applying and removing load, and leaving power-saving states, require separate checks.
Transient / Overshoot	Load Transient / Voltage Overshoot	A transient is the response to a load change; overshoot is a brief voltage spike. Use hardware measurements to investigate its amplitude and duration.
Effective Clocks	Core Effective Clocks	Effective clock speed over a measurement interval, accounting for core activity and sleep. Compare it with the regular clock speed, utilization and results from the same test.
Clock stretching	Clock Stretching	A lower rate of completed work while the displayed core frequency remains high. Diagnose it by comparing Core Clocks, Effective Clocks, utilization and workload performance using 6.2.
Limit Reasons	Performance Limit Reasons	Flags identifying a limiting condition: the Turbo ceiling, power, temperature or electrical limits. Compare Current with present clocks and workload; Maximum retains events since statistics were reset. Practical interpretation is given in 6.2.
WHEA	Windows Hardware Error Architecture	Windows infrastructure for recording hardware errors. Check WHEA-Logger events in the System log during the test; the source and event type guide further diagnosis (6.3).
y-cruncher	Component Stress Tester	A program for computing mathematical constants and stress testing. BKT, BBP, SFTv4 and SVT supplement CPU and cache validation; VT3 uses a large data set. Section 6.4 covers the components and run sequence.
AVX / AVX2	Advanced Vector Extensions / Advanced Vector Extensions 2	Vector instruction sets that change the nature of the computational workload. Validate stability at the highest clock speeds in light and lightly threaded workloads separately from a heavy AVX test.
Microcode	Processor Microcode	Low-level code that defines the processor's internal behavior. Microcode updates fix errors and can change CPU behavior; BIOS updates are one distribution channel. Record the microcode version with the profile and repeat key checks after an update.
Boot / Sleep-wake	Boot / Sleep and Wake	Boot means system startup; sleep/wake is the transition into sleep and back. Check repeatable application of settings and application behavior after each transition.
Daily envelope	Daily-use Operating Envelope	The range of clock speeds, voltages, power, current and temperatures selected for daily workloads. Assess it alongside cooling, noise and measured performance.

Term	English name	Explanation
DC verification	DC Load-line Verification	Checking DC against the selected load-line characteristic and assessing power accounting under several comparable loads. The LGA1700 example's LLC/DC values do not transfer to Z890; compare measurements from the same power-delivery level on LGA1851. See 4.2, 6.2.
Energy / task	Energy per Completed Task	Energy used to complete a task correctly. Keep the amount of work and measurement boundary the same when comparing: E ≈ Pavg × t, where Pavg is mean power over the entire interval and t is its duration (7.1).
Current / Minimum	Current / Minimum / Maximum	Columns for the current, minimum and maximum sensor readings; extrema are tracked from the statistics reset. Minima in different rows can refer to different times, including idle before the load began if statistics were not reset (10.3.1).
IMC / RAM / DRAM	Integrated Memory Controller / Random Access Memory / Dynamic RAM	IMC is the memory controller integrated into the CPU. RAM denotes system memory, and DRAM is its dynamic type. An error in a combined CPU and memory test requires further diagnosis to identify its source.
Safe Boot / ReTry	Safe Boot / ReTry Buttons	Safe Boot temporarily enters BIOS with safe parameters while retaining settings for editing. ReTry repeats startup with the existing parameters.
APO / Binary Optimization	Intel Application Optimization / Intel Binary Optimization Tool	APO optimizes resource allocation and threading for supported applications. Binary Optimization is a separate opt-in feature for compatible CPUs and software. Keep their states unchanged when comparing profiles.

REFERENCE RUN LOG

Record the test version and mode, duration, room temperature and completed result in the log. Save readings for the selected workload interval; Section 6.3 lists the full conditions and checks.

Sources: HWiNFO: Effective Clock · y-cruncher · Intel Core Ultra 200S / DLVR

BOOT AND REBOOT: AGREED TERMS

Boot — A normal system startup.

Boot after idle — A system startup after a period of inactivity.

Reboot — A normal system restart.

Power-cycled boot — A cold system startup after power has been completely removed.

Cold-system reboot — A reboot of a cold system that has not been warmed up by tests.

Warm-system reboot — A reboot of a hot system, after or during testing, with its components warmed up.