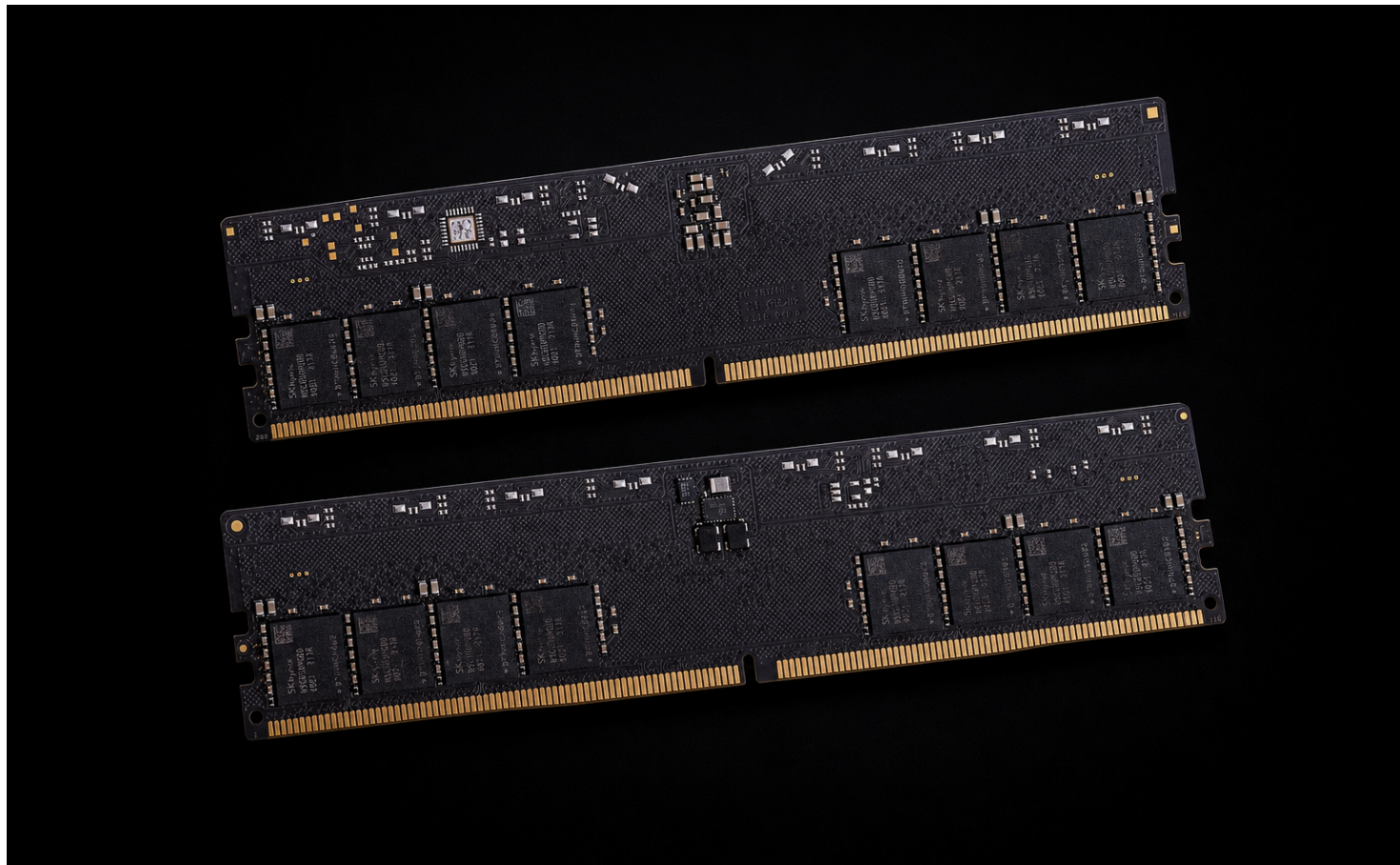




DDR5 MEMORY TUNING AND OPTIMIZATION ON INTEL LGA1700 / LGA1851 PLATFORMS

FUNDAMENTALS / TIMINGS / VOLTAGES / TRAINING / STABILITY

Reference platform: ASUS Z790 Apex Encore (BIOS 2202), with parallel coverage of Z890

REV 4.04 (October 16, 2026)

THE COMPLETE MANUAL FOR DDR5 TUNING AND OPTIMIZATION

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PROJECT REVISION HISTORY

3.01–4.00 (Archive)

- These changes have been archived. You can view them on the website at pakt.cc/ddr5/changelog.

4.01

October 11, 2026

- **P. 13.** Added a PMIC chapter covering DDR5 power, newer designs and overclocking capabilities. The table lists nine kits with verified chip markings, including 2 × 24, 2 × 48 and 2 × 64 GB.
- **P. 16–17.** Added a 2R + DS diagram showing two ranks and ICs on both sides. Clarified the organization of 32 and 48 GB modules.
- **P. 20.** Expanded the operating-point table with 2 × 24, 2 × 48 and 2 × 64 GB kits. Clarified IC revisions and the practical 7200 MT/s target for 2 × 32 and 2 × 48 GB.
- **P. 91–96.** Updated the glossary: SKU, PMIC5120, module power and High DRAM Voltage mode.
- Removed repetitive explanations and qualifications throughout the manual, while preserving calculation conditions, technical limits and warnings about real risks.

4.02

October 12, 2026

- **P. 73.** Clarified how to compare bandwidth, latency and in-game results.
- **P. 74.** Explained Hardware Prefetcher and added a note on its effect on Read/Write/Copy.
- **P. 79, 81–82, 103–104.** Checked software versions and links throughout the manual; updated details and download URLs.

4.03

October 14, 2026

- **PP. 54–64.** Added a new chapter with an advanced analysis of the Training Algorithms (memory training algorithms) settings in the memory section for ASUS motherboards.

4.04

October 16, 2026

- **PP. 21, 26.** Reworked the SPC/DPC explanation with new slot, module-population, and topology diagrams. Added a motherboard classification table in the new subsection 2.15.
- **P. 18.** Reworked the section on DRAM dies and packages: added new SDP/DDP diagrams and clarified their explanations.
- **P. 25.** Updated the MAXSUN board overview: confirmed the two DDR5 slots on Z890ITX WIFI and GKD5, and clarified the VERTEX PRO benchmark result.
- **PP. 22–23.** Expanded the motherboard table in section 2.12 and refined the descriptions of board design, features and practical selection.

INTRODUCTION: APPROACH AND LIMITS OF THE EVIDENCE

To understand a BIOS setting, I compare system behavior, parameter readouts and technical documentation. When those are insufficient, firmware analysis or signal measurements may be needed. Each method addresses a different part of the question.

AT WHAT LEVEL ARE WE INVESTIGATING?

There are four levels at which to investigate memory behavior. Choose the method to suit the question: repeatable tests, technical documentation, BIOS code or signal measurements.

1. Hands-on testing	Change BIOS settings, repeat POST and tests. Check stability, performance, and temperature.
2. Documentation and parameter readout	Compare specifications, other people's results, and parameters read from the system. Separate the meaning of a field from assumptions about how it works.
3. BIOS/MRC and registers	Examine the code, registers, and logs of a specific firmware version. Establish which memory-training stage ran and what it changed.
4. Physical measurements	Observe signals and timing intervals with an oscilloscope or analyzer. Interface measurements do not reveal every process inside the die.

Readouts show the current system state. Establishing the cause of a difference requires repeated checks under controlled conditions. For signal measurements, account for timing, measurement error and the effect of the connection itself.

WHERE I WORK AND WHAT I CAN CLAIM

I work at the first two levels: testing system behavior and examining technical data. I assess individual settings by comparing repeatable results. When no difference is visible, I leave the question open.

I distinguish verified results from explanations of their causes. When evidence is insufficient, I say so. As new measurements become available, I refine the conclusions and correct errors.

MY EXAMPLE: READ TIMING CENTERING 2D

In a recent discussion, I examined Read Timing Centering 2D under Training Algorithms. It is a switch for a training stage, not a numerical timing such as tCL. The ASUS BIOS Manual [1] lists Auto/Disabled/Enabled without explaining the algorithm. The RDTC2D field in Intel FSP for Raptor Lake-S [2] likewise offers only enable/disable. This explains the field's purpose, but does not establish how a particular BIOS applies it. I prefer to leave it Enabled, but this is not a firm recommendation. We will examine each setting in detail in a new chapter in subsequent revisions.

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01 1.1 WHO THIS MANUAL IS FOR AND HOW TO USE IT

You can read this manual from start to finish if you are just getting started, or use it as a reference if you already know the fundamentals. In both cases, the goal is the same: to understand why a setting is changed, how it relates to the other settings, and how to verify the result.

IF YOU ARE TUNING DDR5 FOR THE FIRST TIME

First, distinguish JEDEC from XMP and understand how capacity, rank, and topology affect frequency. Then establish a known-good baseline. Do not start with a full set of someone else's values: if something goes wrong, it will be difficult to find the cause. The links below provide a short tuning path.

[5.1 Preparation](#) [5.10 Recovery](#) [4.9 Voltages](#)
[7.8-7.9 Tests and Errors](#) [8.9 Measurements](#) [10.8-10.9 Profile Record](#)

IF YOU ALREADY HAVE EXPERIENCE

The manual can be used as a reference. Go directly to the relevant group of timings, voltages, or training parameters, but consult the fundamentals chapter whenever the platform, memory capacity, or module type changes. For LGA1851 and CUDIMM, use the relevant sections: the IMC, CKD and training differ from Z790.

HOW TO APPROACH TUNING

1. SAVE THE BASELINE

First test JEDEC/Auto, then test XMP separately. Record the BIOS version, actual frequency, voltages, and trained values.

2. CHANGE ONE THING AT A TIME

In each iteration, change one parameter or one predefined group of parameters. Even related voltages should initially be adjusted one at a time; change them together only once the role of each is understood.

3. REPEAT MEMORY TRAINING

After significant changes, check not only a warm restart but also a full cold boot. One successful boot does not yet prove repeatability.

4. USE MULTIPLE TESTS

No single test covers every type of error. Your test suite must check the modules themselves, the memory controller, and system behavior in real workloads.

5. LEAVE SOME MARGIN

The final daily profile should be slightly more conservative than the last borderline point and remain repeatable at a different temperature and after the system has been idle.

WHAT TO RECORD AFTER EACH STEP

For each journal entry, it is enough to record the changed parameter, frequency, main voltages, module temperature, test results, and cold-boot behavior. A short, clear entry is more useful than a large collection of unexplained screenshots: it lets you quickly identify the last successful point and determine which change introduced the error.

WHEN YOU CAN STOP

A profile can be considered ready when it is repeatable across several cold boots, passes a suite of different tests, and produces no errors in normal workloads at operating temperature. Running one test indefinitely provides less confidence than several workloads that exercise different parts of the system.

IMPORTANT BEFORE YOU BEGIN

XMP is also overclocking relative to the baseline JEDEC mode. Memory errors may be obvious or go unnoticed while causing data corruption. Keep a backup of important files on another storage device or in the cloud, and perform experiments on a system that can be safely recovered.

BEFORE ADVANCED TUNING

In my separate Russian-language guide “DDR5: Principles of Memory Operation”, I explain DRAM organization, commands, and timing relationships. I recommend reading it before advanced tuning to understand the constraints behind each setting.

02 2.1 WHAT EXACTLY ARE WE OVERCLOCKING?

DDR5 overclocking means tuning the entire chain from the memory controller in the processor to the DRAM cells. Increasing Memory Frequency places greater demands on the entire signal path: the CPU socket, motherboard traces and DIMM slot. The interface must then train correctly and reproduce the result at every boot.

THE ENTIRE CHAIN MUST WORK



DATA RATE AND CLOCK FREQUENCY

DDR5-8000 means 8000 million transfers per second on each data pin, or 8000 MT/s. Memory transfers data on both clock edges, so the actual interface clock frequency, fCK, is approximately 4000 MHz. Retailers and utilities often write "8000 MHz," but this manual expresses memory data rate in MT/s.

The theoretical bandwidth of one 64-bit channel, GB/s = $\text{MT/s} \times 8 / 1000$. DDR5-6000 provides 48 GB/s; DDR5-8000 provides 64 GB/s. Two channels provide 96 and 128 GB/s, respectively. Actual values are lower because of commands, refresh, bank switching, and controller idle time.

Mode	fCK	tCK	Bandwidth / 64 bits
DDR5-6000	3000 MHz	0.333 ns	48.0 GB/s
DDR5-8000	4000 MHz	0.250 ns	64.0 GB/s

WHY A HIGH CL CAN STILL BE FAST

Timings are expressed in clock cycles, not nanoseconds. Pure CAS latency is calculated as $\text{CL} \times 2000 / \text{MT/s}$. DDR5-6000 CL30 and DDR5-8000 CL40 therefore both yield 10 ns: the latter uses more cycles, but each cycle is shorter. This is only one part of total latency; tRCD, tRP, IMC queues, Gear mode, processor interconnects, and cache behavior add to it.

CHANNEL, SUBCHANNELS, AND CONTROLLER

A standard DDR5 UDIMM remains 64 bits wide, but is split into two independent 32-bit subchannels. They increase parallelism within a single memory channel; they do not turn one module into a dual-channel system. Two 64-bit CPU channels still require at least two correctly installed modules.

Gear indicates the ratio of the controller-domain frequency to the physical DRAM clock. Gear 1, or 1:1, exists in Intel terminology and remains practically relevant primarily for DDR4. Official Intel operating points for DDR5 on LGA1700 use Gear 2, while LGA1851 uses Gear 2 or Gear 4; Gear 1 is not relevant as a high-frequency DDR5 mode. A higher Gear makes high MT/s easier to achieve, but adds command-path latency.

WHICH GROUPS OF SETTINGS CHANGE IN BIOS

Group	Examples	What changes in practice
Frequency / Gear	Memory Frequency, Gear 2/4	Bandwidth ceiling and command-path latency.
Timings	tCL, tRCD, tRP, tRFC, tREFI	Delays between operations and access efficiency.
Voltages	VDD/VDDQ, SA, TX VDDQ	Signal margin, heat, and IMC behavior.
Training	Vref, ODT, line delays	The mode's ability to train and remain repeatable after boot.

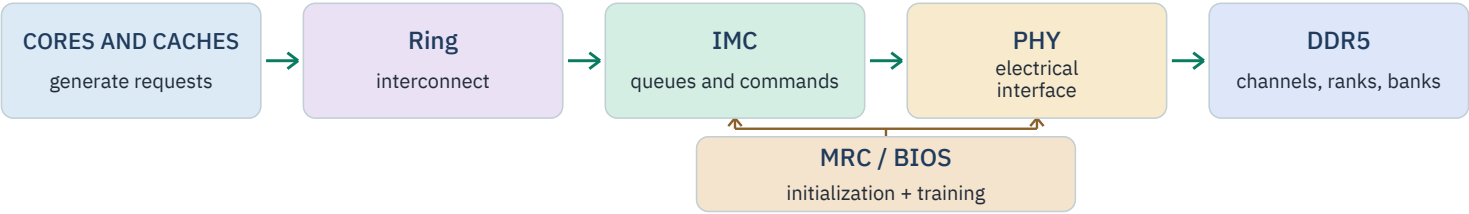
PRACTICAL TAKEAWAY

MT/s sets the bandwidth ceiling, timings determine the delays, and the IMC and physical signal path determine whether the system can reproduce the mode. Choose frequency and timings that suit the IMC and motherboard.

02 2.2 IMC: MEMORY CONTROLLER

The IMC, or integrated memory controller, is the memory controller built into the processor. It accepts requests, distributes them among channels, ranks, and banks, builds the DRAM command queue, and services refresh. The PHY handles the electrical interface with the memory lines. The MRC within the BIOS operates only during startup: it reads the SPD, configures the IMC/PHY, runs memory training, and leaves behind a working configuration. The MRC is not part of the memory request path during operation.

MEMORY REQUEST PATH



Main stages of a request to DRAM.

TWO CHANNELS, BUT FOUR DDR5 SUBCHANNELS

Raptor Lake-S remains a dual-channel desktop platform. In DDR5 mode, each of memory channels A and B comprises two independent 32-bit subchannels, totaling 64 data bits per channel. With both channels in use, four 32-bit subchannels are available. This is not equivalent to a quad-channel platform with four 64-bit channels.

Intel describes two independent MC blocks, one per memory slice. The practical takeaway for the user is that both channels should be populated symmetrically using the motherboard's recommended slots, while the subchannels allow the scheduler to interleave requests more flexibly.

Component	How it works	What this means for overclocking
Gear	Ratio of the MC frequency to the physical DRAM clock: G1= 1:1 , G2= 1:2 , G4= 1:4 .	Official Raptor Lake DDR5 operating points use Gear 2. It makes high MT/s easier to achieve, but adds command-path latency.
Training	The MRC reads the SPD, initializes the IMC/PHY, and trains delays, Vref, and ODT.	A successful POST confirms only that the system booted. Stability must be demonstrated with separate tests and repeated boots.
Load	Rank, DIMM count, the second slot, and routing change the electrical load.	The limit depends on the individual CPU, motherboard, modules, and BIOS. More voltage does not always produce a better result.

HOW LOAD LOWERS THE OFFICIAL RATING

DDR5 configuration on Raptor Lake-S	Intel, MT/s
1SPC / 1DPC, one single-rank DIMM per channel	5600
1SPC / 1DPC, one dual-rank DIMM per channel	5200
2SPC / 1DPC, one DIMM installed per channel	4400
2SPC / 2DPC, two single-rank DIMMs per channel	4000
2SPC / 2DPC, two dual-rank DIMMs per channel	3600

Official operating modes for higher-end 13th Gen Intel Core desktop processors. Some CPU models have lower limits; operation above specification is overclocking.

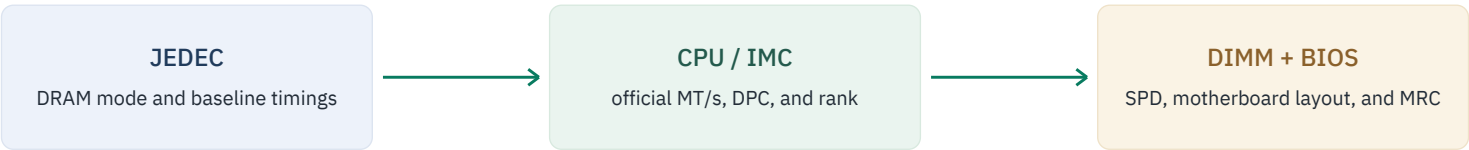
PRACTICAL TAKEAWAY

A memory test error does not prove a DRAM defect: the limitation may lie in the IMC, signal path, training, or voltages. First find the frequency and Gear using loose timings, then change one parameter at a time and test cold boots alongside stability after warm-up under load.

02 2.3 JEDEC, MT/s, AND VOLTAGES

The word "standard" has three different meanings here. JEDEC defines operating modes for the DRAM devices themselves, Intel specifies the official memory-controller limit for a particular processor, and the module manufacturer writes supported parameters to the SPD. A mode is standard for the entire system only when all three layers support it simultaneously.

THREE LAYERS OF COMPATIBILITY



JEDEC SPEED BINS USED IN THIS CHAPTER

This chapter uses JEDEC JESD79-5D v1.41, dated November 2025. It defines DDR5-3200, 3600, 4000, 4400, 4800, 5200, 5600, 6000, 6400, 6800, 7200, 7600, 8000, 8400, 8800, and 9200. The system's operating data rate also depends on CPU, motherboard and module support.

JEDEC bin	fCK	tCK	Bandwidth / 64 bits
DDR5-4800	2400 MHz	0.417 ns	38.4 GB/s
DDR5-6400	3200 MHz	0.313 ns	51.2 GB/s
DDR5-8000	4000 MHz	0.250 ns	64.0 GB/s
DDR5-9200	4600 MHz	0.217 ns	73.6 GB/s

WHAT IS CONSIDERED STANDARD ON OUR PLATFORMS

Platform	Official maximum	What matters
LGA1700 / 12th Gen	up to DDR5-4800	Depends on DPC and ranks; 2DPC lowers the supported mode.
LGA1700 / 13th-14th Gen	up to DDR5-5600	True 1SPC, 2R: 13th Gen - 5200; 14th Gen - 5600*. Modes are lower for 2SPC.
LGA1851 / Core Ultra 200S	1DPC: UDIMM 5600; CUDIMM 6400	CKD improves the clock signal; OC also depends on IMC capability.
LGA1851 / 200S Plus	1DPC CUDIMM up to 7200	The official POR applies to the Intel-specified configuration, not to all modules.

* In the 14th Gen datasheet, DDR5-5600 for 2R is marked as pending Intel enablement; the product brief still lists DDR5-5200. We therefore do not treat 5600 as an unconditionally available current POR.

NOMINAL DDR5 VOLTAGES

For standard DDR5, the nominal DRAM VDD and DRAM VDDQ values are 1.10 V, while VPP is 1.80 V. However, a manual mode at 1.10 V does not automatically become JEDEC-compliant: the IC speed bin, SPD data, CPU support, and motherboard configuration must all match. XMP often uses higher VDD/VDDQ and tighter timings.

The key notation rule is: DDR5-8000 or 8000 MT/s is correct; "8000 MHz" is common slang. The clock frequency of this interface is approximately 4000 MHz.

WHY JEDEC-8000 CAN STILL BE OVERCLOCKING

The DDR5-8000 speed bin in JESD79-5D means that the standard defines such a mode for compatible DRAM devices. But a DDR5-8000 XMP kit may use its own timings and higher voltages, while the official CPU limit remains 5600, 6400, or 7200 MT/s. For such a system, 8000 MT/s is overclocking regardless of the number 8000 appearing in the JEDEC standard.

POR, or Plan of Record, is the officially supported Intel mode for the specified module and rank configuration. Operation above POR is overclocking.

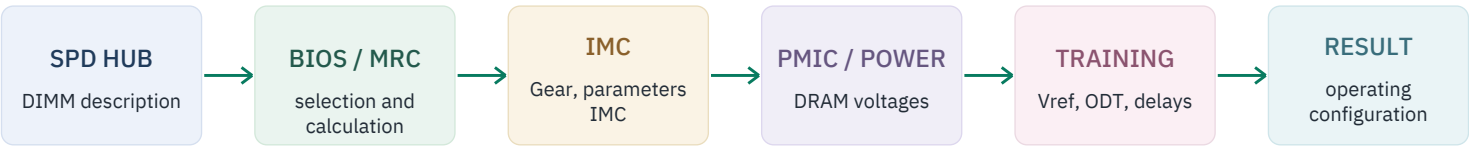
02 2.4 SPD AND INTEL XMP 3.0

SPD, or Serial Presence Detect, is a data set stored in the module's nonvolatile memory. In DDR5, the EEPROM is integrated into the SPD Hub. The BIOS reads this data before the operating system starts and uses it as the module's initial description, but the platform itself still builds and trains the final operating mode.

WHAT THE SPD CONTAINS

Group	What is stored	How the BIOS uses it
Organization	DIMM type, capacity, rank, x8/x16, bus width	Determine the physical channel configuration.
JEDEC timings	Permissible tCK, CL, and minimum intervals	Build a safe baseline mode.
Identification	Manufacturer, part number, serial number, date, CRC	Verify the module and SPD data integrity.
Extensions	XMP and manufacturer/user areas	Offer additional profiles and features.

HOW A PROFILE BECOMES AN OPERATING MODE



XMP 3.0 IS OVERCLOCKING

Intel explicitly calls XMP an overclocking technology. A profile contains a target data rate, a set of specified timings, and voltages validated by the kit manufacturer. XMP 3.0 was created for DDR5 and allows up to five profiles: three factory profiles and two user-rewritable profiles.

I do not recommend using XMP as a ready-made daily profile. Many motherboards apply excessive voltages, calculate Auto values differently, and sometimes train the same kit poorly. It is more reliable to start from a stable baseline, tune the memory manually, and then verify the result.

Before enabling XMP, always compare the kit's exact part number with the QVL for the specific motherboard, including module count, capacity, and rated data rate. A kit's presence on the QVL confirms testing only in the listed configuration and does not guarantee the same result with every CPU sample, another BIOS version, or mixed kits. At the same time, the absence of a particular kit from the QVL does not by itself indicate incompatibility: a motherboard manufacturer cannot physically test every memory kit available.

WHY XMP LOOKS DIFFERENT ON TWO MOTHERBOARDS

The SPD does not store absolutely every secondary and tertiary timing. The BIOS calculates some values itself and obtains others during memory training. The same XMP can therefore produce different Auto timings on different motherboards or after a BIOS update. XMP is a starting recipe, not a complete snapshot of every system register.

THREE LAYERS OF A SINGLE PROFILE

Layer	What it contains	Why it may differ
SPD / XMP	Baseline modes, profile MT/s, specified timings, and DIMM voltages.	Written by the module manufacturer and travels with the kit.
BIOS / MRC	Auto timings, motherboard rules, IMC parameters, and PMIC settings.	Depends on the motherboard model and firmware version.
Training	Trained delays, Vref/ODT, and other results from the current boot.	Depends on the CPU, modules, temperature, and startup conditions.

IN SHORT

SPD describes the module's capabilities. The BIOS selects the mode. The MRC calculates and trains it. Only testing can show whether a stable profile was achieved on a particular system.

02 2.5 PMIC — POWER CONTROL ON A DDR5 MODULE

The PMIC (Power Management Integrated Circuit) converts motherboard power into the DRAM supply rails: VDD, VDDQ and VPP. It sets their voltages, manages startup and monitors overloads and overheating. The PMIC is one chip; the complete power circuit also includes inductors, capacitors and other components on the module PCB.

Desktop DDR5 solutions include Richtek RTQ5132/RTQ5136, Renesas P8911 and ANPEC APW8502C. As of 11 October 2026, newer confirmed client designs include the second-generation Renesas RRG5332, a JEDEC PMIC5120-class device, and Think Future SY5889 with CUDIMM support. Model names and JEDEC classes describe the product and its capabilities; silicon revisions require separate identification. The table lists models or literal package markings checked against teardown photographs.

For overclocking, check the available voltage range, module configuration, BIOS support and power stability under load. Richtek RTQ5136 and Think Future SY5888 offer an extended VDD/VDDQ range up to 2.2 V; SY5888 also specifies Intel XMP 3.0 OC support. Access to higher voltages depends on the module and motherboard. A High DRAM Voltage switch in the BIOS cannot remove every restriction. Check physical markings when identifying the PMIC: SPD and BIOS identification can be wrong.

PMICS FOUND IN REVIEWED KITS

Kit, exact SKU	Rated profile	PMIC: model / marking	Source, year
Kingston Fury Beast KF560C40BBK2-64	2 × 32 GB 6000 CL40	Richtek OP=AC UG1	Tom’s HW 2024
G.Skill Trident Z5 NeoX RGB F5-6000A3038F16GX2-TZ5NXRK	2 × 16 GB 6000 CL30	ANPEC APW8502C / VBA50	Tom’s HW 2026
Patriot Viper Venom RGB PVVR532G640C32K	2 × 16 GB 6400 CL32	Richtek OP=AL	TweakTown 2026
Patriot Viper Venom PVV532G640C32K	2 × 16 GB 6400 CL32	Think Future SY5888	Igor’sLAB 2025
Patriot Viper Xtreme 5 Aurum VXA532G8038K	2 × 16 GB 8000 CL38	MPS MPSG 5431 CQ83	TweakTown 2025
Corsair Dominator Titanium First Edition CMP48GX5M2X7200C36FEW	2 × 24 GB 7200 CL36	Richtek OP=AD 7G1	Tom’s HW 2023
G.Skill Trident Z5 RGB F5-6400J3239F48GX2-TZ5RW	2 × 48 GB 6400 CL32	Richtek OP=AJ 7G1	Tom’s HW 2024
G.Skill Trident Z5 Neo RGB F5-6000J3444F64GX2-TZ5NR	2 × 64 GB 6000 CL34	Richtek OP=CF MY2	Tom’s HW 2026
V-Color Manta XFinity RGB TMXFAL6464832KWK	2 × 64 GB 6400 CL32	Richtek OP=BH 3YM	Tom’s HW 2026

These are the reviewed samples; PMICs may differ between production batches of the same SKU.

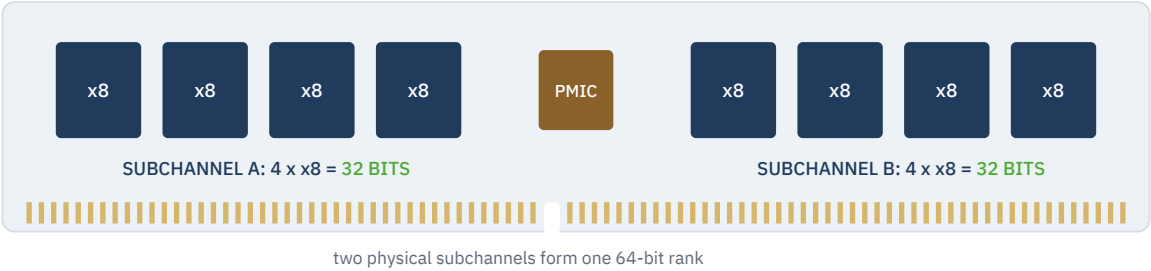
WHAT MATTERS WHEN CHOOSING A KIT

A newer PMIC alone does not improve overclocking. Check whether it supports your intended profile. A 2.2 V capability is a power-controller feature, not a safe DRAM voltage. Memory ICs and the IMC still set the final overclocking limits.

02 2.6 RANK, x8/x16, AND DENSITY

A "32 GB" label indicates only total capacity. It does not show the number of ranks, device width, or density of a single die. These characteristics are independent and are often more important for overclocking than capacity itself.

HOW A TYPICAL DDR5 1Rx8 UDIMM IS ORGANIZED



RANK IS NOT A PCB SIDE

A rank is a logical layer of memory accessible through Chip Select. Each 32-bit DDR5 subchannel selects its own group of DRAM devices; together, the two groups form a 64-bit module rank. 1Rx8 means one such layer built with x8 devices; 2Rx8 means two. The number of PCB sides is not a reliable indicator: check the SPD, markings, and datasheet.

x8 AND x16 ARE THE WIDTH OF ONE DRAM DEVICE

A 64-bit non-ECC rank requires eight x8 devices or four x16 devices. On one 32-bit subchannel, that means four x8 devices or two x16 devices. x16 reduces the number of packages, but usually provides fewer internal bank groups and less parallelism. High-performance desktop kits more often use x8.

A dual-rank DIMM still has two physical subchannels; each one simply has two ranks available. This is sometimes called "four subchannels," but it merely refers to four rank x subchannel combinations, not four separately wired channels.

DIE DENSITY DETERMINES RANK CAPACITY

x8 die density	One die	1Rx8	2Rx8
16 Gbit	2 GB	16 GB	32 GB
24 Gbit	3 GB	24 GB	48 GB
32 Gbit	4 GB	32 GB	64 GB

WHAT IS CALLED NON-BINARY DDR5

Non-binary DDR5 refers to memory built with 24-Gbit dies, typically in 24 GB and 48 GB capacities. In a standard non-ECC DIMM using x8 SDP devices, one package contains one die. Capacity in GB = density of one die in Gbit x number of dies per rank x number of ranks / 8.

HOW TO CHECK YOUR MODULE'S ORGANIZATION

Source	What to look for	Reliability
SPD	Module organization: ranks, x8/x16, and capacity	A quick way to check an installed module.
Label / datasheet	Exact part number and official specification	The best source for a production module.
PCB inspection	Package count and markings	Provides clues, but a PCB side alone does not prove rank count.

DO NOT CONFUSE THIS WITH SYSTEM-LEVEL ECC

On-die ECC corrects some errors within the DRAM die itself. A standard non-ECC UDIMM, an unbuffered module without system-level error correction, does not gain end-to-end data protection between the controller and the module from this feature.

02 2.7 KIT CAPACITY AND IMC LOAD

Memory-controller load depends on DIMMs and ranks per channel, x8/x16 organization, die density, motherboard routing, frequency and timings. The same total capacity can therefore impose a very different electrical load.

TYPICAL KITS FROM 2024-2026

Kit	Common organization	Ranks/channel	Practical significance
2 x 16 = 32 GB	16 GB 1Rx8, 16 Gbit	1	With H16A, second to non-binary H24M in OC potential. I consider this capacity outdated.
2 x 24 = 48 GB	24 GB 1Rx8, 24 Gbit	1	Best overclocking potential, but only with H24M (Hynix M-die).
2 x 32 = 64 GB	2Rx8/16 Gbit or 1Rx8/32 Gbit	1 or 2	Limited OC potential. Look for H16A (Hynix A-die) and newer revisions.
4 x 16 = 64 GB	four 1Rx8 modules	2 (2DPC)	Second branch: usually harder to drive than two 32 GB DIMMs.
2 x 48 = 96 GB	48 GB 2Rx8, 24 Gbit	2	Little OC headroom, which is not the priority here. For high frequency, 2 x 48 GB is usually preferable to 4 x 24 GB.
4 x 24 = 96 GB	four 1Rx8 modules	2 (2DPC)	High load and less signal margin.
2 x 64 = 128 GB	64 GB 2Rx8, 32 Gbit	2	Requires a validated BIOS, QVL support, and a conservative starting point.

SAME NUMBER OF RANKS, DIFFERENT ELECTRICAL TOPOLOGY

64 GB: 2 x 32 GB 2R 1 DIMM per channel two ranks on the channel fewer installed loads	64 GB: 4 x 16 GB 1R 2 DIMMs per channel two ranks + second branch second branch is active
---	---

WHAT REDUCES FREQUENCY HEADROOM THE MOST

A second DIMM on a channel is usually a heavier load than a second rank within one module: it engages the second routing branch and adds the electrical load of another module. Four DIMMs therefore tend to require a lower frequency than two, even with the same total number of ranks. A true 1SPC motherboard with one slot per channel also differs from a four-slot 2SPC motherboard, where the empty second branch still physically exists.

At the same MT/s, 2R may slightly improve performance through rank interleaving: while one rank is busy with an internal operation, the IMC accesses the other. In extreme overclocking, this benefit is often outweighed by the lower achievable frequency.

OFFICIAL INTEL MODES SHOW THE EFFECT OF LOAD

Configuration	POR (Intel mode)	How to interpret it
LGA1700 13th, true-1SPC / 1DPC	1R 5600; 2R 5200	For 13th Gen, the second rank lowers POR.
LGA1700 14th, true-1SPC / 1DPC	1R 5600; 2R 5600*	*2R 5600 is marked pending enablement; the product brief lists 5200.
LGA1700 13th-14th, 2SPC	1DPC 4400; 2DPC: 1R 4000, 2R 3600	Motherboard layout and actual population are listed separately.
LGA1851 Core Ultra 200S	1DPC: UDIMM 5600; CUDIMM 6400	With 2 DIMMs/channel: 1R 4800, 2R 4400.

HOW TO APPROACH HIGH-CAPACITY CONFIGURATIONS

Start at more conservative MT/s, rerun memory training, and verify rank organization through the SPD. A heavier load does not by itself mean that SA, TX VDDQ, or other voltages should be raised immediately: excessive voltage can also reduce stability.

02 2.8 FROM DDR3 TO DDR5: GENERATIONS AND DIMM DESIGN

A new memory generation changes more than speed. The electrical interface, operating voltage, pinout, key position, and internal DIMM organization change with it. Similar appearance does not imply compatibility, and with DDR5 the physical IC layout must be distinguished from logical rank organization.

THREE GENERATIONS - THREE INCOMPATIBLE SLOTS

DDR3

240 pins
VDD/VDDQ 1.50 V
1 x 64-bit interface

DDR4

288 pins
VDD/VDDQ 1.20 V
1 x 64-bit interface

DDR5

288 pins
VDD/VDDQ 1.10 V
2 x 32-bit interface

DDR3L uses 1.35 V. DDR4 and DDR5 both have 288 pins, but differ in pinout and key position.

WHAT IS FOUND ON A TYPICAL DDR5 1Rx8 UDIMM

1 DRAM IC

2 SPD HUB

3 PMIC

4 INDUCTORS

5 R/C COMPONENTS

6 PCB

SUBCHANNEL A: 4 x 8 = 32 BITS

DDR5 KEY

SUBCHANNEL B: 4 x 8 = 32 BITS

TeamGroup T-Force Xtrem DDR5-8200, 24 GB: 1Rx8, eight SK hynix 24-Gbit x8 DRAM ICs.

PCB SIDES AND RANK ARE UNRELATED

Rank organization and the placement of ICs on PCB sides are different characteristics. **Single Rank (1R)** means one logical rank selected by one group of Chip Select signals. **Double-sided (DS)** means only that ICs are physically soldered to both sides of the PCB. These characteristics coincided on many DDR3/DDR4 modules, which perpetuated the confusion.

1R + SS

One rank, one side

FRONT · 8 DRAM

BACK · 0 DRAM

CS0 / R0

A typical DDR5 1Rx8 UDIMM. Eight x8 packages form 2 x 32 bits. Both groups are R0.

1R + DS

One rank, two sides

FRONT · 10 DRAM

BACK · 10 DRAM

CS0 / R0

Kingston KSM48R40BS4TMI-32MDI [1].
DDR5, 32 GB, 1Rx4 ECC RDIMM.
20 x x4 = 2 x 40 bits.

2R + SS

Two ranks, one side

FRONT · 8 DDP

BACK · 0 DRAM

CS0 / R0 CS1 / R1

Example from RAMGuide: early Corsair DDR4 8 GB, Hynix MMR. The source does not identify the exact SKU.

2R + DS

Two ranks, two sides

FRONT · 8 DRAM · R0

BACK · 8 DRAM · R1

CS0 / R0 CS1 / R1

DDR5 2Rx8 UDIMM: one module, 16 x8 ICs. 16 Gbit → 32 GB; 24 Gbit → 48 GB. [1, 10]
Examples: 2 × 32 and 2 × 48 GB kits.

The colored bars indicate membership in R0 and R1. Verify rank through the SPD and datasheet.

02 2.8.1 PCB SIDES AND RANK ON DDR5: CLARIFICATIONS

In theory, rank is unrelated to PCB side: rank organization and IC placement are different characteristics. However, among standard DDR5 UDIMMs/SO-DIMMs actually in production, I found no confirmed 2R + SS module. Every verified 2Rx8 DDR5 module uses 16 DRAM packages and is DS.

On mainstream desktop DDR5 UDIMMs, 2R is usually built from 16 separate x8 SDPs (Single-Die Packages), resulting in 8 packages on the front and 8 on the back. For example, Kingston describes current 64 GB DDR5 UDIMMs built with 32-Gbit DRAM as exactly 16 x x8 = 64 GB, 2 ranks.

NON-ECC DDR5 UDIMM EXAMPLES

Module	Organization	DRAM packages and PCB sides
Kingston KVR56U46BD8-32	32 GB DDR5-5600 2Rx8	16 FBGAs; 8 + 8, DS. Datasheet: pp. 1-2. [1]
Samsung M323R4GA3BB0-CQKOL	32 GB DDR5-4800 2Rx8	DS according to the ASRock QVL. 2Rx8 organization according to the MSI AVL. [6, 7]
SK hynix HMC88AGB0A081N	32 GB DDR5-5600 2Rx8	16 SDPs - HMC88AGB0A family. DS for 081N according to the ASRock QVL. [5, 6]
Micron MTC16C2085S1UC56BA1	32 GB DDR5-5600 2Rx8	16 DRAM packages; 8 + 8, DS. Datasheet: pp. 1-2. [4]
Innodisk M5UZ-BGM2KC0Q-D	32 GB DDR5-5600 2Rx8	16 ICs; 2 ranks; 2 sides. Explicitly stated in the Approval Sheet. [8]

The SO-DIMM example is Kingston KVR56S46BD8-32: 16 FBGAs, 8 on each side. [9]

TYPICAL NON-ECC DDR5 x8 UDIMM USING SDPs

1Rx8 = 8 DRAM packages → SS

2Rx8 = 16 DRAM packages → DS

PRACTICAL LAYOUT

This diagram describes mainstream non-ECC DDR5 UDIMMs using x8 SDPs. PMIC, SPD Hub, and other support ICs are not included in the DRAM package count. I verify rank through the SPD and datasheet, and SS/DS through package placement.

02 2.8.2 DRAM IC: DIE AND PACKAGE

DRAM stands for Dynamic Random Access Memory. On a memory module, it takes the form of **ICs** (Integrated Circuits). A single package may contain one or more dies.

SILICON DIE

Silicon containing memory cells. Data is stored as charge in capacitors; **refresh** periodically restores that charge.

IC PACKAGE

Protects the die and connects it to the board. Inside are the die, interconnects, and a substrate with traces.

MODULE PCB

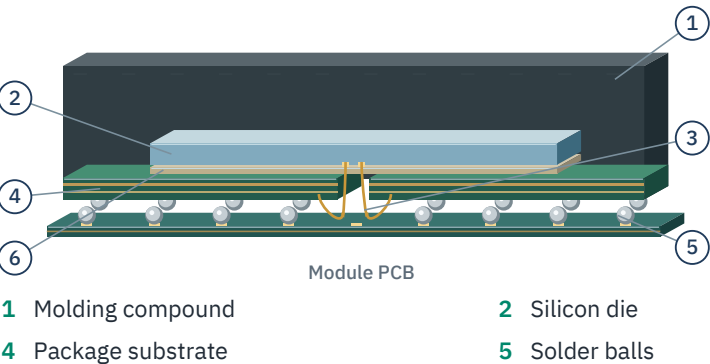
Holds the packaged ICs. Each package has its own small substrate.

ONE PACKAGE, DIFFERENT DIE COUNTS

Examples of wire-bonded packages

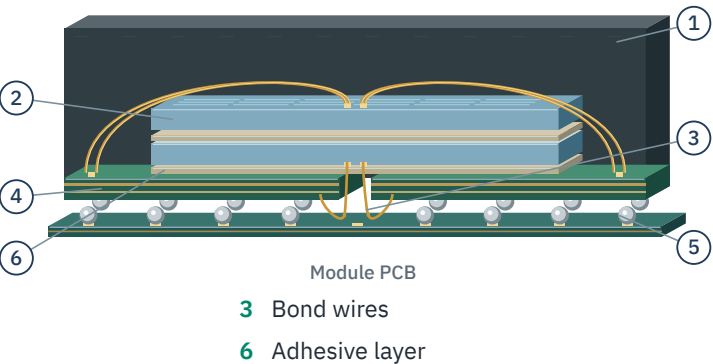
SDP · one die

Single-Die Package



DDP · two dies

Dual-Die Package

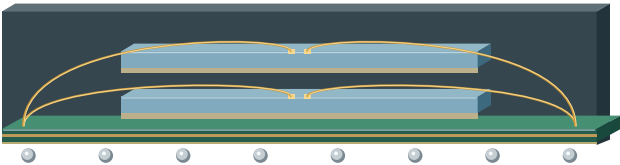


FBGA (Fine-Pitch Ball Grid Array) is a package with closely spaced solder balls. The balls on its underside are soldered to the module PCB.

HOW TWO DIES FIT INTO ONE PACKAGE

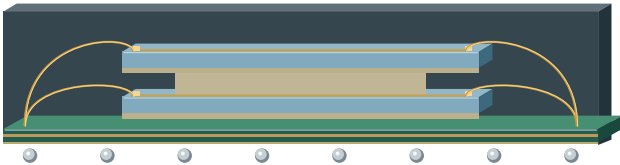
DDP assembly variants · Invensas

1. Center pads



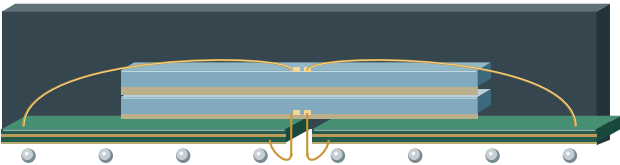
Both dies face up. Bond wires connect the center pads to the substrate.

2. Edge pads



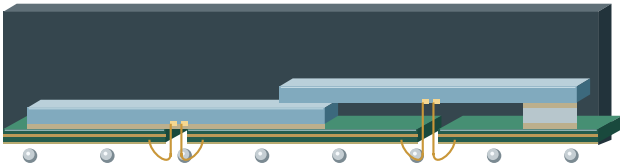
RDL routes the pads to the edges. A spacer separates the dies.

3. Back-to-back



The lower die connects through a window in the substrate; the upper die connects from above.

4. Both dies face down



The dies are offset. Bond wires pass through windows in the substrate.

RDL (Redistribution Layer) relocates the pads across the die surface.

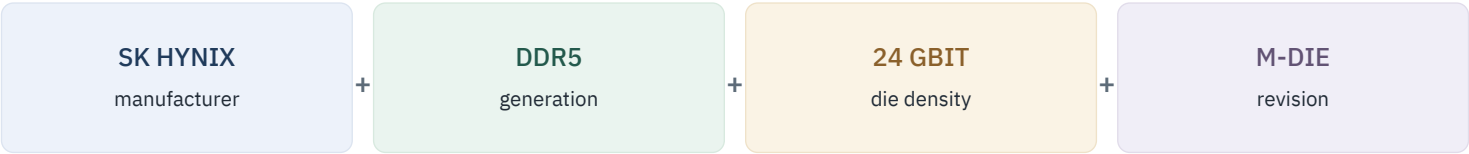
READING THE MODULE LAYOUT

8 DDP packages contain 16 dies. Rank organization depends on their connections and select signals. I check rank organization and device width against the **SPD data and the module datasheet.**

02 2.9 MANUFACTURER, DENSITY, AND REVISION

DRAM die density (also called DRAM IC density) is the amount of data stored by one die. It is specified in gigabits, such as 16, 24 or 32 Gbit. The brand on the heat spreader identifies the kit manufacturer, but the DRAM dies themselves may have been made by SK hynix, Samsung, or Micron, for example. An exact description requires four fields: manufacturer, DDR generation, density, and revision.

CORRECT NOTATION



OVERCLOCKING SHORTHAND

Abbreviation	Full notation	What matters
H16M	SK hynix DDR5 16Gbit M-die	An early 16-Gbit die; not the same as H24M.
H16A	SK hynix DDR5 16Gbit A-die	Another revision in the 16-Gbit family; commonly found in 2 x 16 kits.
H24M	SK hynix DDR5 24Gbit M-die	The basis of typical 24/48 GB modules and 48/96 GB kits.
S16B	Samsung DDR5 16Gbit B-die	Do not confuse it with the famous Samsung DDR4 B-die.
Micron Rev.B/D	Micron DDR5 + density + :revision	Micron uses the same letter for different densities.

HOW TO READ THE PART NUMBER INSTEAD OF GUESSING FROM XMP

A full SK hynix code such as H5CGD8M... can be read by field: H5C indicates DDR5, GD indicates 24-Gbit density, 8 indicates x8 organization, and M indicates the die generation; the remaining suffix encodes other product parameters. Micron places the revision after a colon: for example, 16-Gbit :D and 24-Gbit :B are different products. Samsung must be tied to the full K4R... part number because the letter B appears in both DDR4 and DDR5.

The most reliable sources are the module's official datasheet and the full number printed on the DRAM IC. The SPD and utilities help, but if the exact revision cannot be determined, label it accordingly as an assumption. XMP frequency, voltage, and capacity alone do not prove the die type: the kit manufacturer may change ICs without changing the marketing name.

DIE REVISION AND PROCESS NODE ARE NOT THE SAME THING

A-die, B-die, and M-die describe a revision or design generation within a manufacturer's naming scheme. 1nm, 1bnm, 1alpha, and 1beta name a process node. The letter is not an official quality grade and does not promise specific MT/s, tCL, or a permissible voltage.

HOW TO CONFIRM THE IC TYPE

Step	Source	What you can conclude
1	Module datasheet and part number	The organization and rated specification of the specific product.
2	Full DRAM IC marking + official decoder	Manufacturer, density, x8/x16 organization, and die revision.
3	SPD and diagnostic utilities	A useful clue; a clickable field in HWiNFO Memory Timings does not replace confirmation from the marking.
4	XMP bin and observed behavior	Only an indirect assumption, which must be labeled as such.

Manufacturers can use the same ICs in kits with different XMP profiles, PCBs, PMICs and voltages. The revision describes the die design; binning establishes the kit's validated operating point.

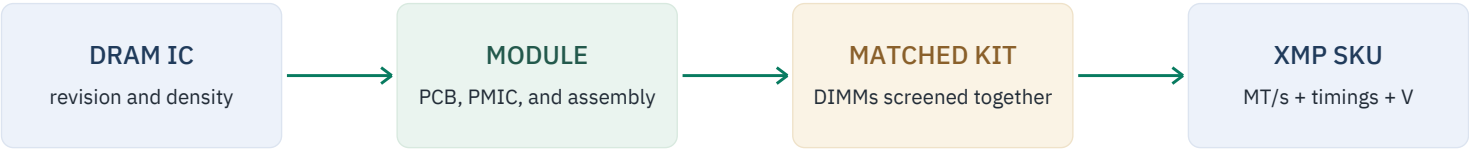
THE MAIN SAFEGUARD AGAINST CONFUSION

Always write manufacturer + DDR5 + density + revision. H16M is not H24M; Samsung DDR4 B-die is not Samsung DDR5 B-die; Micron Rev.B is not the 1beta process node.

02 2.10 XMP BINNING AND KIT SCREENING

Binning, or screening, is the sorting of ICs and assembled modules by their ability to operate at a specified point: particular MT/s, timings, and voltage. The manufacturer validates the result and sells it as a separate SKU with a specific XMP profile.

HOW AN XMP KIT IS CREATED



HOW TO COMPARE KIT BINNING

The same H16A or H24M ICs appear in kits with different profiles. One kit is selected for frequency, another for low tCL, lower voltage or capacity. Compare them for the same task and with matching module organization.

ONE DATA RATE – DIFFERENT OPERATING POINTS

Kit	Profile	VDD/VDDQ	CAS, ns	Interpretation
2 × 16 GB	XMP 6000 36-36-36	1.35 V	12.00	Looser CL at the same MT/s.
2 × 16 GB	XMP 6000 30-36-36	1.35 V	10.00	Tighter tCL without raising V.
2 × 16 GB	XMP 6000 28-36-36	1.40 V	9.33	Lower tCL, with higher voltage.
2 × 32 GB	XMP 6000 30-36-36	1.40 V	10.00	Capacity and rank change the conditions; capacity is the main OC constraint.*
2 × 24 GB [1]	EXPO 6000 28-36-36	1.35 V	9.33	H24M changes the conditions and raises OC potential.
2 × 48 GB [2]	XMP 6000 30-36-36	1.35 V	10.00	H24M changes the conditions and raises potential; capacity is the main OC constraint.*
2 × 64 GB [3]	EXPO 6000 32-44-44	1.40 V	10.67	S32M changes the conditions and raises potential; higher capacity constrains OC even further.

* 7200 MT/s is the established practical stable community target for 2 × 32 and 2 × 48 GB.

[1] G.SKILL F5-6000J2836F24GX2-TZ5NRW

[2] G.SKILL F5-6000J3036F48GX2-TR5S

[3] G.SKILL F5-6000J3244G64GX2-TZ5NR

WHAT A LOWER PROFILE VOLTAGE TELLS YOU

With matching ICs, density, capacity, rank, PCB, frequency and timings, lower VDD/VDDQ suggests the kit needs less voltage at that operating point. The manufacturer specifies a validated voltage; testing establishes the minimum working value and OC headroom. The IMC, motherboard and cooling also affect the result. Kits are validated as a set, so mixed kits require fresh testing.

02 2.11 DPC/SPC, MODULES, AND ROUTING TOPOLOGY

Desktop LGA1700 and LGA1851 platforms have two memory channels: **A and B**. First count the slots on the board, then the modules installed in each channel.

SPC — slots per channel

Slots Per Channel

1SPC: one slot in A and one in B. **2 slots** total.

2SPC: two slots each in A and B. **4 slots** total.

DPC — DIMMs per channel

DIMMs Per Channel

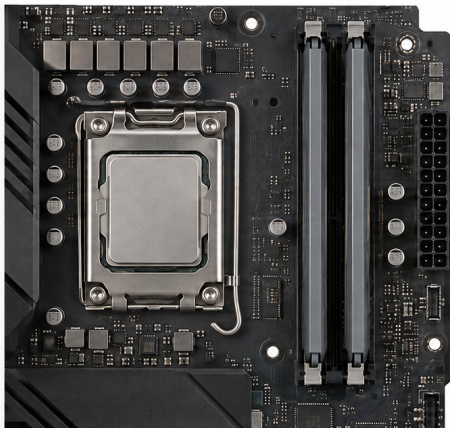
1DPC: one DIMM installed in each channel.

2DPC: two DIMMs installed in each channel.

2-DIMM / 4-DIMM board describes its slot count. **2 × 24 GB** means two 24 GB modules. **1R / 2R** means one or two ranks in a DIMM. **1DPC 2R** means one dual-rank DIMM per channel.

WHAT THIS LOOKS LIKE ON A BOARD

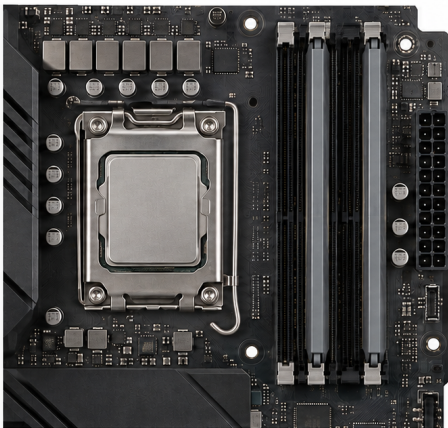
1SPC + 1DPC



A B

2 slots, 2 modules. One each in A and B. There is no room for four DIMMs.

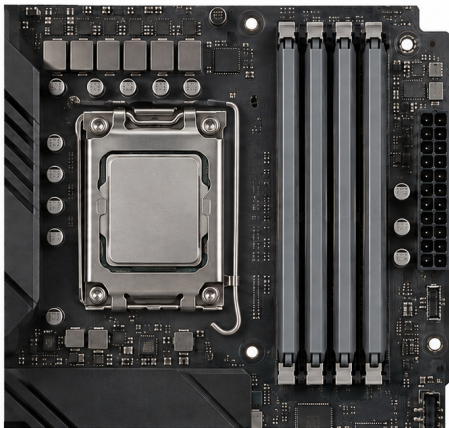
2SPC + 1DPC



A1 A2 B1 B2

4 slots, 2 modules. A2 and B2 are populated; A1 and B1 are empty. The board remains 2SPC.

2SPC + 2DPC



A1 A2 B1 B2

4 slots, 4 modules. A1, A2, B1, and B2 are populated. Two DIMMs per channel.

HOW SLOTS IN ONE CHANNEL ARE CONNECTED

Daisy Chain and T-topology allow 1DPC and 2DPC. Population does not change the board's routing.

1SPC · one slot



One connector on the path. No second slot or branches to it.

2SPC · Daisy Chain



The line passes through the A1 and A2 connection points in sequence.

2SPC · T-topology



Branches of similar electrical length run from a common point to the slots.

WHAT I CHOOSE FOR OVERCLOCKING

For high frequencies, only **1SPC + 1DPC**: this is the most effective layout. On 2SPC boards, only **2SPC + 1DPC** with two modules. Filling all four slots is bad form unless capacity takes priority.

With **2DPC**, electrical loading increases, and the data rate often has to be reduced. T-topology equalizes the paths to the slots, but retains the load of four DIMMs. The result also depends on the IMC, ranks, memory kit, and BIOS.

With three DIMMs, A and B have different populations. A/B are the platform's two channels; DDR5's 32-bit subchannels do not change this classification.

02

2.12 CHOOSING AN LGA1700 MOTHERBOARD: Z690 AND Z790

Z790 alone does not make a motherboard faster than Z690. For memory, physical 1SPC routing, PCB quality, BIOS/MRC, and recovery features matter more. The selections below include 2-DIMM models, standard 4-DIMM Z790 boards, and expensive E-ATX flagships. Overall, 2-DIMM motherboards provide better memory training than the rest.

2-DIMM / TRUE 1SPC: MOTHERBOARDS FOR MAXIMUM FREQUENCY

Motherboard	Format	DIMMs / max., GB	Official MT/s	Practical takeaway
ASUS Z690 Apex	ATX	2 / 96	6600	Post-launch lottery: some 2021 boards could not even hold XMP-6400; good later samples reached around 7000. Buy used only after testing both DIMM slots and the BIOS.
MSI Z690 Unify-X	ATX	2 / 96	6800+	A top Z690 board: full OC/recovery features and a convenient BIOS. My findings on it are coming in the next revision.
MSI Z690I Unify	Mini-ITX	2 / 96	6800+	A very short signal path and strong memory performance; fewer POST diagnostics and bench-overclocking tools.
Gigabyte Z690 Tachyon	E-ATX	2 / 128	7000	Bench-oriented routing and a hardware OC Kit; the BIOS is designed for an experienced enthusiast.
EVGA Z690 DARK K NGP N	E-ATX	2 / 64	6600+	Strong hardware, but the product line is no longer being developed; buy used only with full awareness of this.
ASUS Z790 Apex, white	ATX	2 / 96	8000+	The first white revision remains top-tier: mature BIOS and a complete OC Toolkit.
ASUS Z790 Apex Encore	ATX	2 / 96	8400+	The foundation for this manual: a clear BIOS, diagnostics, recovery, and strong daily-profile potential.
ASUS Z790-AYW OC WiFi	ATX	2 / 96	8200+	An Apex alternative: good 2-DIMM routing; notably simpler power delivery, I/O, and OC/recovery features.
MSI Z790MPOWER	mATX	2 / 128	8000+	An affordable specialized 2-DIMM board; simpler and less fully equipped than flagship models.
MSI Z790I Edge WiFi	Mini-ITX	2 / 128	8000+	A strong compact daily-use option; not a full bench replacement for Apex/Tachyon.
ASRock Z790I Lightning WiFi	Mini-ITX	2 / 128	8600+	Strong 8-layer board: XMP-8000/8200 in reviews. I have reservations about ASRock/BIOS; OC/recovery is more modest than on flagships. IMC and kit determine the limit.
Gigabyte Z790 Tachyon	E-ATX	2 / 128	8333	Excellent routing and hardware switches; the BIOS requires an understanding of the settings.
EVGA Z790 DARK K NGP N	E-ATX	2 / 64*	8000+	A 9400 profile is not a guarantee; in 2026 this is more of a collectible OC platform.

EVGA: STRONG MOTHERBOARDS, BUT A POOR BUY TODAY

EVGA has released no platforms since Z790; BIOS updates are rare and some remain beta. In 2026, DARK K|NGP|N is not worth buying for a main system: it is a collectible or dedicated bench platform tied to a specific firmware.

* 64 GB according to the original EVGA specification; 96 GB confirmed by later 2 x 48 GB kits.

DOCUMENTATION REVIEWED:
ASUS, MSI, Gigabyte, and EVGA specifications/QVL/BIOS; Igor'sLAB Z690 Apex batch comparison; ROG Forum; September 1, 2026.
ASRock: specification and manual; independent testing by Tom's Hardware / PC Gamer. Checked September 11, 2026.
[G.SKILL QVL: 2 x 48 GB](#) [ASRock: specification](#) [ASRock: manual](#) [Tom's Hardware: review](#) [PC Gamer: review](#)

02

2.12 CHOOSING AN LGA1700 MOTHERBOARD: Z690 AND Z790

4-DIMM / 2SPC: CURRENT Z790 MOTHERBOARDS FOR DAILY USE AND CAPACITY

Motherboard	DIMM / max., GB	Official MT/s	Practical significance
ASUS ROG Strix Z790-E Gaming WiFi II	4 / 256*	8000+	Useful for memory tuning: Q-Code, rear FlashBack and Clear CMOS buttons. An SSD in M.2_1 switches the GPU to x8.
ASUS TUF Gaming Z790-Pro WiFi	4 / 256*	7800+	For a daily build: four Gen4 M.2 slots without sharing GPU lanes. No FlashBack; CMOS reset uses onboard pins.
ASUS ProArt Z790-Creator WiFi	4 / 256*	7200	Choose for 10GbE and two Thunderbolt 4 ports. FlashBack is available; an SSD in M.2_4 disables SATA 5–8.
MSI PRO Z790-A MAX WiFi	4 / 256	7800+	For several SSDs: four Gen4 M.2 slots without sharing GPU lanes. Flash BIOS is available; CMOS reset uses JBAT1 pins.
MSI MAG Z790 Tomahawk MAX WiFi	4 / 256	7800+	For many SATA/USB devices and memory tuning: rear Flash BIOS and Clear CMOS buttons. An SSD in M2_1 switches the GPU to x8.
MSI MPG Z790 Edge Ti MAX WiFi	4 / 256	7800+	For five M.2 slots and rear Flash BIOS / Clear CMOS. Four Gen4 M.2 slots retain GPU x16; the fifth, M2_1, switches it to x8.
GIGABYTE Z790 AORUS PRO X	4 / 256	8266	Choose for 5GbE and five M.2 slots. An SSD in Gen5 M2C_CPU switches the GPU to x8. Q-Flash Plus; CMOS reset uses pins.
GIGABYTE Z790 AORUS ELITE X WIFI7	4 / 256	8266	For four Gen4 SSDs and Wi-Fi 7; Q-Flash Plus and a Clear CMOS button. An NVMe SSD in M2M_SB disables SATA 2/3.
GIGABYTE Z790 GAMING X AX rev. 2.1	4 / 256	7600	For a daily build with four Gen4 SSDs; Q-Flash Plus. CMOS reset uses pins; an NVMe SSD in M2M_SB disables SATA 2/3.

4-DIMM / 2SPC: E-ATX FLAGSHIPS FOR CAPACITY AND FEATURES

Motherboard	DIMMs / max., GB	Official rating	What matters for memory
ASUS Z690 Extreme	4 / 256*	6400+	Dual BIOS, Safe Boot/ReTry, ProbeIt and 10GbE for tuning. An M.2_1 SSD switches the GPU to x8.
MSI Z690 Godlike	4 / 192	6666+ 1DPC1R	10GbE, two Thunderbolt 4 ports, six M.2; dual BIOS and POST codes. An M2_3 SSD switches the GPU to x8.
ASUS Z790 Extreme	4 / 256*	7800+	Tuning and I/O: dual BIOS, Safe Boot/ReTry, ProbeIt, 10GbE. An M.2_1 SSD switches the GPU to x8.
MSI Z790 Godlike	4 / 256	7800+ 1DPC1R	Seven M.2, 10GbE, two Thunderbolt 4 ports; dual BIOS and POST codes. An M2_4 SSD switches the GPU to x8.
MSI Z790 Godlike MAX	4 / 256	7800+ 1DPC1R	Wi-Fi 7; rated 6000+ at 2DPC2R. Seven M.2, 10GbE, dual BIOS. An M2_4 SSD switches the GPU to x8.

I do not recommend the listed flagship 4-DIMM / 2SPC boards for overclocking: a 2-DIMM / 1SPC board or a more affordable 4-DIMM board is more rational.

OC speed and capacity maxima are separate; the operating point depends on the CPU, BIOS and kit. GAMING X AX lists 7600 for 13th/14th-gen Core i7/i9. All three MSI QVLs for 14 Gen K list Kingston KF556C40BWAK4-128: 4 × 32 GB at 5600. * The five ASUS boards above support 256 GB with updated BIOS; their specifications still list 192 GB.

DOCUMENTATION REVIEWED:

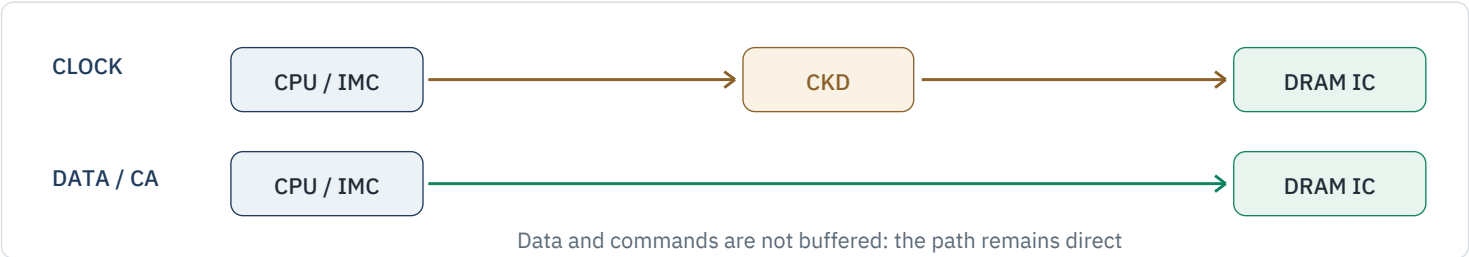
Z690/Z790 boards: exact-model specifications, manuals, QVLs and BIOS notes. ASUS Extreme: 256 GB from BIOS 3302 (Z690) / 1904 (Z790). Original reviews: 3DNews, Hardwareluxx, Igor'sLAB and Tom's Hardware; test conditions are retained in the research report.

[Strix E II: BIOS](#) [TUF Pro: BIOS](#) [ProArt: BIOS](#) [MSI: QVL](#) [Z690 Extreme: BIOS](#) [Z790 Extreme: BIOS](#)

02 2.13 LGA1851, Z890, AND CUDIMM

The main memory-related change in LGA1851 is official CUDIMM support. A Clocked Unbuffered DIMM remains a conventional unbuffered module for data and commands, but adds a separate Clock Driver, or CKD. It receives the clock signal, cleans it up, and reshapes it before sending it to the DRAM ICs.

WHAT EXACTLY THE CKD DOES



UDIMM AND CUDIMM ON CORE ULTRA 200S

Scenario	UDIMM POR	CUDIMM POR	What this means
true-1SPC / 1DPC, Core Ultra 200S	DDR5-5600	DDR5-6400	CKD enables a higher standard operating mode.
true-1SPC / 1DPC, 200S Plus	DDR5-5600	DDR5-7200	The updated IMC raises CUDIMM POR.
2SPC board, 1DPC: A2/B2 only	DDR5-5600	DDR5-5600	Even an empty second branch changes the official mode.

PRACTICAL Z890 SELECTION: OC, STANDARD 4-DIMM, AND FLAGSHIPS

Motherboard	DIMM / max., GB	Official MT/s	Practical significance
ASUS Z890 Apex	2 / 128	9600+	DIMM Fit Pro and bundled memory cooling aid tuning; Safe Boot/ReTry and Dual BIOS help recover from failed OC settings.
MSI Z890 Unify-X	2 / 128	9600+ / 7200+ 2R	An external Tuning Controller offers Safe Boot/Retry; Memory Force in BIOS and switchable Dual BIOS assist tuning.
Gigabyte Z890 Tachyon ICE	2 / 128	10400 OC	A bench/LN2 platform with a 10-layer PCB, hardware OC Kit, LIMP Mode, and DualBIOS for recovery after failed tuning.
ASUS TUF Z890-Plus WiFi	4 / 256	9066+	Daily-use ATX: DIMM Fit, BIOS FlashBack and Q-LED diagnostics; clearing CMOS requires the onboard header.
MSI MAG Z890 Tomahawk WiFi	4 / 256	9200+ 1DPC1R	ATX for tuning: POST codes, rear Clear CMOS and Flash BIOS buttons, 5GbE networking and two Thunderbolt 4 ports.
Gigabyte Z890 Aorus Elite WiFi7	4 / 256	9200 OC	ATX with POST codes, Multi-key Safe Mode and Q-Flash Plus; its four M.2 slots do not take lanes from the GPU.
ASUS Z890 Extreme	4 / 256	9200+	E-ATX with NitroPath, Safe Boot/ReTry and dual BIOS; 10GbE, TB5 and six M.2 slots, with GPU lane sharing.
MSI Z890 Godlike	4 / 256	9200+ 1DPC1R	E-ATX: dual BIOS, diagnostic LCD, 10GbE + 5GbE; six onboard M.2 plus two on a card that shares GPU lanes.

WHY YOU CANNOT COMPARE ONLY MAXIMUM MT/s

The 10400 Tachyon ICE, 9600+ Apex/Unify-X, and 9200+ 4-DIMM results used different CPUs, modules, BIOS versions, and slot populations. Maximum capacity does not promise maximum MT/s: these are separate specification targets.

CKD BYPASS AND INTEL 200S BOOST

Both UDIMM and CUDIMM work on Z890. On some LGA1700 motherboards, CUDIMM is possible only through a BIOS-supported CKD bypass mode: the clock driver is bypassed, the CUDIMM advantages disappear, and frequency is limited by the older platform. Buying CUDIMM to accelerate LGA1700 is pointless. Intel 200S Boost is a separate official OC profile, while 200S Plus refers to updated CPU models. Boost specifies memory up to DDR5-8000, NGU/D2D up to 3.2 GHz, VccSA/VDD2 up to 1.20/1.40 V, and DRAM VDD/VDDQ up to 1.40 V with one DIMM installed per channel.

MAIN TAKEAWAY FOR LGA1851

CKD expands the practical DDR5 range, but a record rated frequency still does not guarantee stable daily operation. If maximum frequency is the goal, look first at Apex, Unify-X, or Tachyon ICE; if high capacity matters, look at everything else. If your tastes are unusual and you have a couple of hundred bucks to spare, choose Extreme or Godlike.

02 2.14 MAXSUN Z690-Z890 1SPC BOARDS

Maxsun appeals to enthusiasts as a relatively budget-friendly overclocking option: two memory slots and decent features for the money. The BIOS still leaves room for improvement, especially with manual timings, as the reviews below show.

Maxsun model (MS-)	Socket / format	PCB layers	CPU VRM	Memory: claimed / tested
iCraft Z690ITX WIFI	1700 / Mini-ITX 2×DDR5	10	8+1; ISL99390, 90 A; controller*	7200 / 7400+ OC
Challenger Z690M	1700 / microATX 2×DDR4	n/a	8+1+1; SiC654, 50 A	DDR4: incompatible with DDR5
iCraft Z790ITX WIFI	1700 / Mini-ITX 2×DDR5	n/a	9 main ISL99390 stages, 90 A**	7400+ OC / 8200+ in blog; XMP-7200 tested
iCraft Z890 VERTEX	1851 / ATX 2×DDR5	8***	20+1+1; stage part numbers and ratings n/a	9200 OC; strong potential under extreme cooling
Challenger Z890M	1851 / microATX 2×DDR5	n/a	10+1+1; 60 A SPS	7200 OC; independent limit not established
Challenger Z890M WIFI	1851 / microATX 2×DDR5	n/a	10+1+1; 60 A SPS	7200 OC; independent limit not established
Challenger Z890M WIFI ICE	1851 / microATX 2×DDR5	n/a	10+1+1; 60 A SPS	7200 OC; independent limit not established

PCB: printed circuit board; n/a: unconfirmed; OC: overclocking; data rates in MT/s. VRM layouts follow manufacturer/teardown data. An SPS current rating does not specify the current capability of the whole board.
* Z690ITX: RAA229131 in the product listing, RAA229132 in the teardown. ** Not all nine stages supply Vcore. *** Low-loss PCB material and back-drilling (removal of unused plated via stubs).

Z790ITX WIFI: a budget option for LGA1700

Tom’s Hardware (2023): i9-13900K, BIOS H5.3G, TeamGroup XMP-7200 worked without issues. i2HARD (2023) reached 7200 with an i9-13900KF, H4.2G and 2×16 GB Patriot 5600, but CL rose to 58 because manual timings were applied incorrectly. H7.4G included timing optimizations. The early review does not tell us how newer firmware behaves. I would consider it for a sensible 7200 target, rather than buy it for the advertised 8200.

Z890 VERTEX: the main candidate for high data rates

Overclocking.com (2025) used an Ultra 7 265K and 2×24 GB G.Skill with Hynix M. Results: 8800 CL36 with ambient memory cooling and extreme CPU cooling; 9400 CL36 at roughly -70 °C on the memory in y-cruncher 2.5B; 9494 CL36 in 7-Zip. 11200 was a separate bench. There is potential, but the daily-use ceiling remains unproven; the reviewer missed Safe Boot/Retry for quick recovery after a failed boot.

NEWLY SHOWN BOARDS: KEEP THESE SEPARATE FOR NOW

iCraft Z890 VERTEX PRO	Computex 2026: 2×DDR5, 20+1+1; reported as microATX. A completed 3DMark benchmark records 2×24 GB at 9066 MT/s.
iCraft Z890ITX WIFI	MAXSUN's exhibition placard lists Mini-ITX, 2×DDR5, dual-channel operation (1SPC), and an 8+1+1 power design.
Terminator Z890M WIFI GKD5	MAXSUN's launch presentation showed a microATX board with two DDR5 slots. Retail-version specifications remain unconfirmed.

Choose by test results and BIOS behavior. Two slots and good routing help overclocking; the achieved frequency also depends on the IMC and kit and requires stability testing.

i2HARD: Z790ITX VERTEX: conditions and results	Tom’s Hardware: XMP-7200 VERTEX: limitations	Maxsun: BIOS Z790ITX PRO: 3DMark
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02 2.15 MOTHERBOARD CLASSIFICATION

SPC means slots per channel. Population lists supported DPC configurations, rather than an installed kit. Channels A/B follow the board manual; DDR5 subchannels are not counted separately here. Board names link to specifications; confirmed topology labels link to their sources.

T-Topology is used for motherboard memory routing and has confirmed implementations in previous DDR generations. No reliably confirmed T-Topology implementations have been established for the production DDR5 boards examined here.

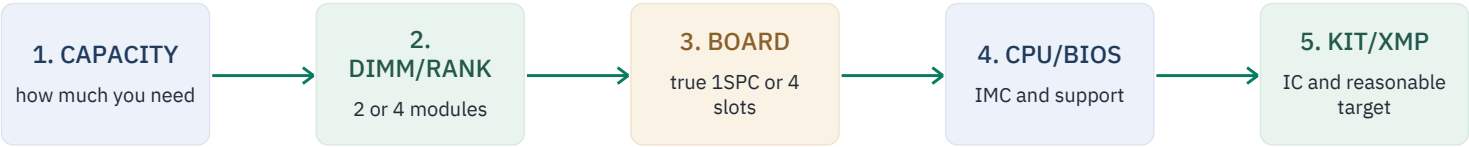
Model	Slots	SPC	Population	Topology
ASUS ProArt Z890-Creator WiFi	4	2SPC	1DPC / 2DPC	Unconfirmed
ASUS ROG Maximus Z690 Apex	2	1SPC	1DPC	Point-to-point
ASUS ROG Maximus Z690 Extreme	4	2SPC	1DPC / 2DPC	Unconfirmed
ASUS ROG Maximus Z790 Apex	2	1SPC	1DPC	Point-to-point
ASUS ROG Maximus Z790 Apex Encore	2	1SPC	1DPC	Point-to-point
ASUS ROG Maximus Z790 Extreme	4	2SPC	1DPC / 2DPC	Unconfirmed
ASUS ROG Maximus Z890 Apex	2	1SPC	1DPC	Point-to-point
ASUS ROG Maximus Z890 Extreme	4	2SPC	1DPC / 2DPC	Unconfirmed
ASUS ROG Strix Z790-E Gaming WiFi II	4	2SPC	1DPC / 2DPC	Unconfirmed
ASUS ROG Strix Z890-I Gaming WiFi	2	1SPC	1DPC	Point-to-point
ASUS TUF Gaming Z890-Plus WiFi	4	2SPC	1DPC / 2DPC	Unconfirmed
ASUS Z790-AYW OC WiFi	2	1SPC	1DPC	Point-to-point
MSI MAG B860 Tomahawk WiFi	4	2SPC	1DPC / 2DPC	Unconfirmed
MSI MAG Z790 Tomahawk MAX WiFi	4	2SPC	1DPC / 2DPC	Unconfirmed
MSI MAG Z890 Tomahawk WiFi	4	2SPC	1DPC / 2DPC	Unconfirmed
MSI MEG Z690 Godlike	4	2SPC	1DPC / 2DPC	Unconfirmed
MSI MEG Z690 Unify-X	2	1SPC	1DPC	Point-to-point
MSI MEG Z690I Unify	2	1SPC	1DPC	Point-to-point
MSI MEG Z790 Godlike	4	2SPC	1DPC / 2DPC	Unconfirmed
MSI MEG Z790 Godlike MAX	4	2SPC	1DPC / 2DPC	Unconfirmed
MSI MEG Z890 Godlike	4	2SPC	1DPC / 2DPC	Unconfirmed
MSI MEG Z890 Unify-X	2	1SPC	1DPC	Point-to-point
MSI MPG Z790I Edge WiFi	2	1SPC	1DPC	Point-to-point
MSI Z790MPOWER	2	1SPC	1DPC	Point-to-point
GIGABYTE Z690 AORUS TACHYON	2	1SPC	1DPC	Point-to-point*
GIGABYTE Z790 AORUS MASTER X	4	2SPC	1DPC / 2DPC	Daisy Chain
GIGABYTE Z790 AORUS PRO X	4	2SPC	1DPC / 2DPC	Daisy Chain
GIGABYTE Z790 AORUS TACHYON	2	1SPC	1DPC	Point-to-point*
GIGABYTE Z890 AORUS ELITE WIFI7	4	2SPC	1DPC / 2DPC	Daisy Chain
GIGABYTE Z890 AORUS MASTER	4	2SPC	1DPC / 2DPC	Daisy Chain
GIGABYTE Z890 AORUS TACHYON ICE	2	1SPC	1DPC	Point-to-point
ASRock Z790 Taichi Lite	4	2SPC	1DPC / 2DPC	Unconfirmed
ASRock Z790I Lightning WiFi	2	1SPC	1DPC	Point-to-point
ASRock Z890 Taichi OCF	2	1SPC	1DPC	Point-to-point
ASRock Z890I Nova WiFi	2	1SPC	1DPC	Point-to-point
EVGA Z690 DARK K NGP N	2	1SPC	1DPC	Point-to-point
EVGA Z790 DARK K NGP N	2	1SPC	1DPC	Point-to-point
Maxsun Challenger Z690M · DDR4	2	1SPC	1DPC	Point-to-point
Maxsun Challenger Z890M	2	1SPC	1DPC	Point-to-point
Maxsun Challenger Z890M WIFI	2	1SPC	1DPC	Point-to-point
Maxsun Challenger Z890M WIFI ICE	2	1SPC	1DPC	Point-to-point
Maxsun iCraft Z690ITX WIFI	2	1SPC	1DPC	Point-to-point
Maxsun iCraft Z790ITX WIFI	2	1SPC	1DPC	Point-to-point
Maxsun iCraft Z890 VERTEX	2	1SPC	1DPC	Point-to-point
Maxsun iCraft Z890 VERTEX PRO (announced)	2	n/a	n/a	Unconfirmed
Maxsun iCraft Z890ITX WIFI (announced)	2	1SPC	1DPC	Point-to-point
Maxsun Terminator Z890-A WIFI	4	2SPC	1DPC / 2DPC	Daisy Chain
Maxsun Terminator Z890M WIFI GKD5 (announced)	2	n/a	n/a	Unconfirmed

Point-to-point means the controller connects to the sole socket in a channel: a structural classification based on board documentation.
* GIGABYTE calls the Z690/Z790 Tachyon layout “2-DIMM daisy chain”; this table classifies them as Point-to-point by the number of sockets in each channel.

02 2.16 PRACTICAL PLATFORM AND KIT SELECTION

The right choice starts not with the highest XMP profile, but with the required capacity. Capacity determines module and rank count, which in turn determines the appropriate motherboard topology. Only then does it make sense to choose a CPU, specific IC, and realistic frequency target.

DECISION ORDER



TYPICAL SCENARIOS

Goal	Kit	Motherboard	Realistic approach
Maximum frequency	2×16 / 2×24	2-DIMM true-1SPC	Best chance of high MT/s; capacity is fixed in advance.
Balanced profile	2×16 / 2×24 / 2×32	High-quality 2- or 4-DIMM board	On a 4-DIMM board, use A2/B2 and do not chase records.
96-128 GB	2×48 / 2×64	QVL + current BIOS	Density, rank, and training matter more than an impressive XMP profile.
Four modules	one matched 4-DIMM kit	4-DIMM motherboard	Expect lower MT/s from the outset; two K2 kits are not equivalent to one K4 kit.
Future upgrade	final capacity now	according to task priority	Buying a second kit later does not guarantee that both kits will work together without additional tuning.

PROCESSOR

For full manual control, choose an unlocked K/KF processor and a Z-series motherboard. The individual IMC sample remains a lottery: a more expensive CPU model does not promise a stronger controller. On LGA1851, Intel 200S Boost also requires a suitable K/KF processor, motherboard, and BIOS.

MOTHERBOARD

For maximum frequency with two modules, choose a true 1SPC OC motherboard. For high capacity and flexibility, choose four slots while accepting a lower ceiling when fully populated. The Z790 Apex Encore is officially limited to 96 GB. Yet BIOS 0904, dated February 16, 2024, promises “Enhanced compatibility with 256GB memory.” I think the developers were high when they wrote that: this note does not override the specification limit. So 128-192 GB on LGA1700 requires another motherboard. Check the exact QVL, current BIOS, support for the required density and CUDIMM, recovery features, and DIMM airflow rather than a general marketing claim.

MEMORY KIT

Buy one matched kit with the final capacity you need. Check the part number, number of DIMMs, rank, die density, XMP voltage, and presence of a temperature sensor. Intel does not officially specify more than 192 GB for LGA1700 even if an individual motherboard lists 256 GB support; for LGA1851, the current Core Ultra 200S ARK already specifies up to 256 GB. In practice, the final limit is determined by the combination of CPU, motherboard, BIOS version, and specific memory kit.

FORMULA FOR A RATIONAL PURCHASE

Capacity -> number of DIMMs and ranks -> motherboard topology -> CPU and BIOS -> IC and XMP. Changing this order makes it easy to buy an impressive profile that does not match the actual load or platform capabilities.

03 3.1 HOW TO READ TIMINGS / 3.2 THE COMMAND PATH

A timing specifies a duration or an interval between memory events. Most are minimums; tREFI limits the average interval between refreshes. BIOS values usually use DDR5 clock cycles, so their duration depends on data rate. BIOS menus and the community group timings into primary, secondary and tertiary parameters.

FIRST CONVERT CLOCK CYCLES TO NANoseconds

Data rate	1 tCK	tCL 36	Formula and takeaway
DDR5-6000	0.333 ns	12.00 ns	tCK = 2000 / 6000; 36 × 0.333
DDR5-8000	0.250 ns	9.00 ns	time = timing × 2000 / MT/s
DDR5-8200	0.244 ns	8.78 ns	36 cycles is already faster than at 8000
DDR5-9000	0.222 ns	8.00 ns	profiles are more accurately compared in ns

3.2 COMMAND PATH: WHERE LATENCY APPEARS

Read:	ACT -> tRCDRD -> READ -> tCL -> first data
Closing after READ:	READ -> tRTP -> PRE; tRAS must also be met
Write:	WRITE -> tCWL -> data burst -> end of burst
From the end of the write:	tWR -> PRE or tWTR_S/L -> READ (details in 3.5)

Notation	Expansion	How to read it in this manual
ACT / PRE	Activate / Precharge	The bank first opens the required row, then prepares for the next one.
RD / WR	Read / Write	The order of the letters indicates the current and next commands.
S / L	Short / Long	Usually a different / the same bank group, respectively.
sg / dg	Same Bank Group / Different Bank Group	Intel scheduler notation for transitions between commands.
dr / dd	Different Rank / Different DIMM	The dr path is not used with 1R. On 1DPC motherboards, including ASUS Apex, dd timings are not used regardless of the installed modules. Neither path is used with 1R/1DPC.
Auto / Trained	Auto / Trained Value	After memory training, check the value that was actually applied.

FOUR TYPICAL ACCESS PATHS

Situation	Sequence	Minimum total	What matters
Row open	READ -> tCL -> data	tCL	The shortest path; ACT has already been completed.
Row closed	ACT -> tRCDRD -> READ -> tCL	tRCDRD + tCL	CAS cannot be evaluated without opening the row.
Another row open	PRE -> tRP -> ACT -> tRCDRD -> READ -> tCL	tRP + tRCDRD + tCL	Three primary timings are visible here at once.
Write	ACT -> tRCDWR -> WRITE -> tCWL	tRCDWR + tCWL	The write path has its own latency.

MAIN RULE

Consider the complete command path. After an early READ following ACT, the sum tRCDRD + tRTP may constrain row closure rather than tRAS alone. Gear 2 or Gear 4 does not require multiplying DRAM timings by 2 or 4.

Conversion when changing data rate: $N_{new} = N_{old} \times MT/s_{new} / MT/s_{old}$. Round up for minimum intervals; round down for the maximum interval tREFI.
Example: tRFC 688 at DDR5-8200 -> $688 \times 8400 / 8200 = 704.78 \rightarrow 705$ cycles at DDR5-8400. Nold is the original value; round a fractional tREFI result down.

03 3.3 PRIMARY TIMINGS

Primary timings describe opening a row, accessing data, and preparing a bank for the next row. They form one sequence, but are not calculated from one another by a simple rule: tCL, tRCD, and tRP are limited by different internal IC operations.

Timing	What it specifies	Relationship or formula	How to tune it
tCL	READ -> first data	$tCL(ns) = tCL \times 2000 / MT/s$	Reduce by 2 cycles: ASUS DDR5 rounds an odd value up.
tRCDRD	ACT -> READ	Closed row: $tRCDRD + tCL$	Find its limit separately after tCL; at high frequency, it often hits the limit sooner.
tRCDWR*	ACT -> WRITE	Write path: $tRCDWR + tCWL$	Start with tRCDRD; possible coupling between values depends on BIOS/MRC.
tRP	PRE -> new ACT	Row conflict: $tRP + tRCDRD + tCL$	Reduce separately; errors appear during frequent row changes.
tRAS	ACT -> permitted PRE	Practical guideline: $tRCDRD + tRTP$	Reducing it below the limiting sum provides no further speedup.
tRC	ACT -> ACT in the same bank	$tRC = tRAS + tRP$	Calculated for this platform: $61 + 49 = 110$; the actual interval may be longer.
CR	command bus rate	1N is theoretically faster; 2N provides operating margin	1N is practically irrelevant for DDR5, especially at the high frequencies used here. The working baseline is 2N.

WHY THE DDR5 PRIMARY TIMING STRING LOOKS DIFFERENT

Example	Primary timing string	Delta from tCL	What this means
DDR4 B-die	14-14-14-34	0 / 0	Famous for $tCL=tRCD=tRP$; tRAS remained separate.
DDR5-5600 JEDEC	46-45-45	-1 / -1	DDR5 has no mandatory $tRCD=tCL+X$ rule.
DDR5-8000 XMP	38-48-48	+10 / +10	A typical high-frequency profile on screened ICs.
DDR5-8400 XMP	40-52-52	+12 / +12	The gap grows because CAS and row opening have different limits.
Manual's 8200 baseline	36-49-49-61	+13 / +13	tCL scales down well, while tRCD/tRP are already close to their own limits.

HOW TO UNDERSTAND THE RELATIONSHIP WITHOUT INVENTING A FORMULA

Lowering tCL reduces latency after the READ command has already been issued, but does not open the row any faster. A good tCL therefore does not force tRCD or tRP to fall with it. On Hynix DDR5, tCL often continues to respond to VDD after tRCD/tRP have reached their own limits.

tRAS, by contrast, is validated through the actual row-closing sequence. For an early READ after ACT, the minimum cycle is described by the greater of tRAS and $tRCDRD+tRTP$, plus tRP. If the sum exceeds tRAS, reducing tRAS alone does not speed up the cycle.

RELATIONSHIP BETWEEN tCL AND THE OTHER PRIMARY TIMINGS

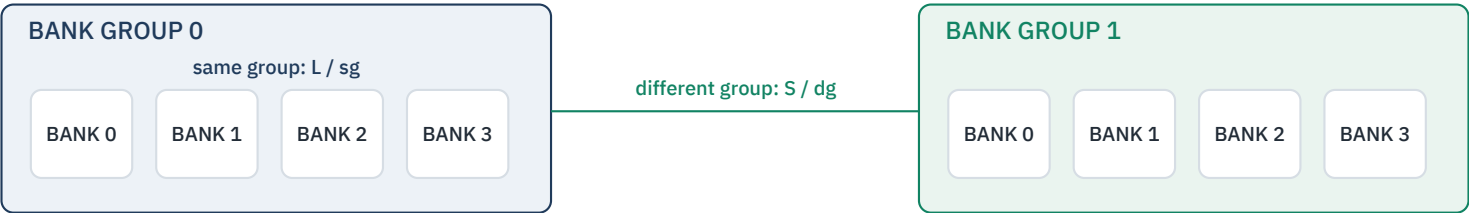
On high-frequency DDR5, the difference between tRCD/tRP and tCL is often approximately 8-13 cycles, but this is an observation from XMP and overclocking, not a formula. tRAS is selected according to the row-closing path, while tRC is the calculated sum $tRAS+tRP$ for this platform.

For the baseline profile with an early READ after ACT: read from a closed row = $49 + 36 = 85$ CK; row conflict = $49 + 49 + 36 = 134$ CK; tRAS = $49 + tRTP_{12} = 61$; tRC = $61 + 49 = 110$.

* A particular BIOS/MRC version may in fact couple or normalize tRCDRD and tRCDWR in a certain mode; however, public documentation does not confirm any universal requirement that they be equal.

03 3.4 SECONDARY TIMINGS: ACTIVATION AND BANK GROUPS

DDR5 divides banks into groups. Two commands to different groups can usually be issued closer together than within the same group because internal resources conflict less. S therefore means the short path and L the long path; in Intel tertiary timings, dg and sg follow the same logic.



Timing	What it specifies	Relationship or formula	How to tune it
tRRD_S	ACT -> ACT, different group	For x8 / 1 KB page: minimum 8 CK	Set 8 for every kit in this manual.
tRRD_L	ACT -> ACT, same group	At least 8 CK and the minimum in ns	Reduce after S; L is usually no lower than S.
tFAW*	Minimum interval from the first to the fifth ACT	For x8: the greater of 32 CK and the speed bin's limit in ns	My profile uses 32 as a convenient working OC setting.
tCCD_S	CAS -> CAS, different group	BL16 / 2 = 8 CK	Natural basis for tRDRD_dg and tWRWR_dg.
tCCD_L	CAS -> CAS, same group	At least 8 CK and 5 ns	Related to tRDRD_sg; shown separately on Z890.
tCCD_L_WR	WR -> WR, same group; second WRITE requires RMW	At least 32 CK and 20 ns	Shown as a separate field on Z890.
tCCD_L_WR2	WR -> WR, same group; second WRITE without RMW	At least 16 CK and 10 ns	A separate specification; the BIOS may not show it as a separate field.

* Details in 3.4.1

WHERE THE BENEFIT APPEARS

tRRD and tFAW have the greatest effect in workloads that open rows in different banks concurrently. Their effect is barely visible during a short sequential read from an already open row. tCCD, by contrast, determines the spacing of adjacent column commands and is more noticeable in a sustained data stream.

With tRRD_S=8, consecutive ACT commands can occur at 0, 8, 16, and 24 CK, with the fifth no earlier than 32 CK. This is how tRRD_S=8 and tFAW=32 work together. A value above 32 further restricts the activation stream.

For the x16 devices considered here, with a 2 KB page, the cycle-based portion of tFAW is 40 CK; the time limit also depends on the datasheet and speed bin. Server 3DS memory has additional constraints. tRRD_L needs both 8 CK and the minimum in ns.

03 3.4.1 tFAW: WHERE THE MINIMUM COMES FROM

tFAW specifies the minimum time from the first to the fifth ACT command within one rank. The check repeats for every new command: ACT5 is compared with ACT1, ACT6 with ACT2, and so on. tRRD must also be met between adjacent ACT commands.

WHY 8 NS IS NOT A UNIVERSAL LIMIT

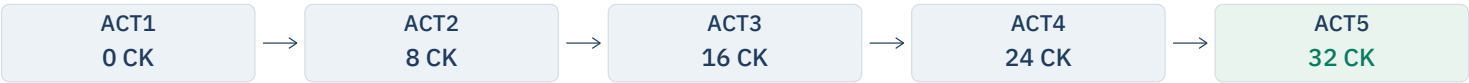
The tFAW minimum is specified simultaneously in CK cycles and nanoseconds. Both limits come from the table for the required DRAM organization and speed bin. One limit cannot be applied to all DDR5: the time component changes between bins, while the cycle component also depends on device organization.

The table contains selected speed bins for SK hynix 32 Gbit M-die, x8, with a 1 KB page. Minimums come from the datasheet. The green 8200 row is my OC profile: it lists the 32 CK setting and its time calculated from frequency.

Data rate, MT/s	tFAW, CK	Time, ns
5600	32 - minimum	11.428 - minimum
6000	32 - minimum	10.666 - minimum
6400	32 - minimum	10 - minimum
8000	32 - minimum	8 - minimum
8200 (my OC)	32 - setting	≈ 7.805 - calculated
8400	32 - minimum	7.619 - minimum
8800	32 - minimum	7.272 - minimum

WHY THE PRACTICAL MINIMUM FOR x8 IS 32 CK

tFAW (Four Activate Window) permits no more than four ACTIVATE commands within one rank in its window. tRRD_S specifies the interval between adjacent ACT commands to different bank groups. For standard DDR5 x8 with a 1 KB page, the minimum limit considered here is **tRRD_S = 8 CK**.



There are four intervals between ACT1 and ACT5: $4 \times \text{tRRD_S} = 4 \times 8 = 32 \text{ CK}$. tRRD_S prevents ACT5 from being issued earlier; the figure shows the densest possible ACT sequence while meeting the other constraints.

$$\text{tFAW_effective(min)} \approx 4 \times \text{tRRD_S}; \text{ with tRRD_S} = 8 \text{ CK:}$$
$$\text{tFAW_effective(min)} = 32 \text{ CK}$$

Estimated ACT-command density at the specified tRRD_S.

PAGE SIZE: WHY THE LIMIT FOR x16 IS 40 CK

DDR5 x4/x8 uses a 1 KB page; x16 uses 2 KB. For x16, the cycle-based tFAW minimum is 40 CK even though tRRD_S may also be 8 CK: $4 \times 8 = 32 \text{ CK}$. The value 40 is not derived from $4 \times \text{tRRD_S}$: the larger activated page requires a stricter window for a series of ACT commands and a tighter peak-load limit. tFAW is the constraint here: ACT5 can occur no earlier than 40 CK, not 32 CK.

JEDEC: BOTH CK AND NANOSECONDS COUNT

$$\text{tFAW: 1 KB - the greater of 32 CK and the ns minimum; 2 KB - 40 CK and the ns minimum.}$$

Here nCK is the duration of the stated number of cycles: times are compared. 32/40 CK are cycle limits; the minimum in ns comes from the specific IC and speed bin, so the final value is not always equal to 32/40 CK.

PRACTICAL TAKEAWAY

For standard DDR5 x8 with tRRD_S = 8 CK, tFAW = 32 CK is the effective lower limit. This follows from tFAW and tRRD_S working together: lowering tFAW alone below 32 CK does not increase ACT command density.

03 3.5 SECONDARY TIMINGS: READ, WRITE, AND RECOVERY

tRTP, tWR, and tWTR start from different events. To calculate the complete command-to-command path, add the preceding delays. This teaching example uses 8200 MT/s and CL36 with the SK hynix 32 Gbit 8000 speed bin. All sums are in clock cycles (CK).

READ AND WRITE: WHEN THE ROW CAN CLOSE

Read. tCL runs from READ to the first data; tRTP runs from the same READ to permitted row closure (PRE). Do not add CL and RTP for this interval. For 7.5 ns: $7.5 \times 8200 / 2000 = 30.75 \rightarrow 31$; select tRTP32 from the MR6 table. My overclocking profile uses tRTP12, or 14 at high data rates; I do not go below 12.

Write. tCWL runs to the first data, then the BL16 burst takes $16 / 2 = 8$ cycles, followed by tWR recovery after the data ends. DRAM tCWL = tCL - 2 = 34. For tWR = 30 ns, the calculation gives 123, then the permitted MR6 code 126. In our overclocking profile, tWR = 48, with no further reduction.

WRITE → PRE: tCWL + 8 + tWR = 34 + 8 + 126 = 168. For a WRITE followed by a READ with auto-precharge in the same bank, tCCD_WTRA ≥ 168 - tRTP32 = 136. Subtract RTP because PRE waits that interval after READ.

WTR: THE WAIT AFTER WRITE DATA ENDS

tWTR_S applies to another bank group: for this speed bin, compare 4 cycles and 2 ns → 8.2 → 9. tWTR_L covers the long path within the same group: 16 cycles or 10 ns → 41. These values come from the specific IC speed bin, not CL.

DRAM WRITE to READ: tCWL + 8 + tWTR. Across groups: 34 + 8 + 9 = 51; for the long path within one group: 34 + 8 + 41 = 83. The separate path to another bank in the same group (M) may be shorter in the datasheet; do not automatically substitute it for L.

In an overclocking profile, WTR, WR and RTP are tightened below datasheet intervals and tested under load.

WHY INTEL tWRRD IS NOT THE COMPLETE DRAM SUM

tWRRD = write → read; tRDWR = read → write. WTR uses the first group. S corresponds to dg, different bank groups; L corresponds to sg, the same group. Intel stores scheduler intervals; the utility derives WTR from them.

In pyhwinf0's main calculation for Raptor Lake DDR5 ≥ 5200: WTR_S = WRRD_dg - C - 10 - B; WTR_L = WRRD_sg - C - 10 - B. C is the controller's read-back CWL field. B is MR8[7]: 0 for the short, 1 for the long write-signal ending. Do not substitute its duration of 0.5 or 1.5 cycles for this bit.

Example: C34, B1, WRRD_dg54, WRRD_sg86. This gives S = 54 - 34 - 10 - 1 = 9, L = 86 - 34 - 10 - 1 = 41. The 10 = burst 8 + decoder correction 2. This is a specific utility's display calculation; read C and B rather than guessing them from CL.

HOW THE LINKED PAIR CHANGES

With C and B fixed, WRRD_dg54 → 55 gives WTR_S9 → 10; sg changes only the long pair. To keep WTR unchanged when C rises by 2, increase WRRD by 2 as well. Check the values actually applied after training.

The separate DEC/ADD branch and reverse calculation are explained in 3.7; compact formulas are in Chapter 11, p. 89.

03 3.6 SECONDARY TIMINGS: REFRESH

DRAM cells gradually lose charge, so memory must be refreshed regularly. tRFC specifies the duration of one refresh cycle, while tREFI specifies the average interval between cycles. The controller can shift individual refresh commands slightly. Lower tRFC and higher tREFI reduce idle time, but also reduce thermal margin.

Timing	What it specifies	Relationship or formula	How to tune it
tRFC1	REFab, Normal Refresh (refreshing all banks in normal mode)	$tRFC1\text{ ns} / tCK$; round up	The specification for the corresponding mode; not necessarily a separate BIOS field.
tRFC2	REFab, 2x Fine Granularity Refresh (twofold fine-granularity refresh of all banks)	A separate timing, not a fraction of tRFC1	The 2x FGR mode specification; the BIOS field name alone does not prove it is active.
tRFCsb	REFsb, Same-Bank Refresh (refreshing the same-numbered bank in each group)	$tRFCsb\text{ ns} / tCK$; round up	A separate same-bank refresh specification; display depends on the platform.
tREFI	Maximum Average Refresh Interval	$tREFI\text{ ns} / tCK$; round down Intel field limit: 262143	In this manual, values above approximately 30000 are tested only with airflow and monitoring.

REFERENCE REFRESH SPECIFICATIONS BY MODE AND DIE DENSITY

Die density	tRFC1, normal	tRFC2, 2x FGR	tRFCsb, REFsb	What this shows
8 Gbit	195 ns	130 ns	115 ns	Fewer cells mean a shorter baseline cycle.
16 Gbit	295 ns	160 ns	130 ns	The typical baseline for older 16 GB modules.
24 / 32 Gbit	410 ns	220 ns	190 ns	Higher density requires a longer refresh.

NORMAL REFRESH: TEMPERATURE AND INTERVAL

Mode / example	Time	@ DDR5-8200	Practical significance
REFab: TCASE ≤ 85 °C	3.9 μs	≈ 15990	Normal mode: 3.9 μs. FGR at the same temperature: 1.95 μs.
REFab: 85 < TCASE ≤ 95 °C	1.95 μs	≈ 7995	Normal mode: 1.95 μs; FGR: 0.975 μs. 85 °C is not an OC target.
Manual rule: >≈30000	> 7.32 μs	>≈30000	Directed airflow and HwINFO monitoring are mandatory during testing.
My TeamGroup Xtream	31.97 μs	131071	On the 2x24 GB kit, errors begin at approximately 47 °C according to the module sensor.
Intel platform limit	63.94 μs	262143	18-bit maximum; ASUS Z790 exposes the full range. This is not a stability target.

WHY tRFC AND tREFI ARE CHANGED SEPARATELY

Both parameters reduce refresh margin, but in different ways: tRFC shortens the cycle duration, while tREFI makes cycles less frequent. Changing them simultaneously obscures the cause of an error. tREFIX9 is the controller limit for the maximum interval between refreshes of one rank; Intel stores it in units of 1024 DCLK and defines it as $8 \times tREFI / 1024$. At high OC values of tREFI, direct calculation may exceed the tREFIX9 field range. The value actually programmed depends on the field limits and the controller/MRC implementation. Leave the field on Auto.

SPECIFIED AND ACTUAL TEMPERATURE ARE NOT ONE NUMBER

The 85 °C threshold refers to TCASE, the case temperature of the DRAM IC itself. On consumer DDR5, HwINFO usually shows a local SPD Hub/PCB sensor: this is a useful monitoring point, but not the temperature of the hottest IC and not the TCASE from the specification.

With tREFI above approximately 30000, directed airflow is a mandatory testing condition under this manual's methodology, but a fan does not replace monitoring. If the profile is stable only with directed airflow, the same airflow must be used in daily operation. The 47 °C / 131071 example above characterizes my specific kit, voltages, and test, not a limit for all DDR5.

Additional ranks and ICs usually increase cooling requirements.

DOCUMENTATION REVIEWED: SK hynix/Micron DDR5 temperature and refresh tables; Intel TC_RFTP; ASUS ROG Z790 BIOS Manual; SPD Hub temperature-sensor documentation.

03 3.6.1 SECONDARY TIMINGS: CALCULATING tREFI/tRFC

The tREFI and tRFC values in BIOS are expressed in memory clock cycles, so the same value at two data rates represents different amounts of time. tREFI limits the maximum average interval between refreshes, while tRFC specifies the minimum duration of a refresh cycle. This is why they are rounded in opposite directions.

ONE BASIC FORMULA - TWO DIRECTIONS

tCK, ns = $2000 / MT/s$; time, ns = $N \times 2000 / MT/s$. In reverse: $N = \text{time in ns} \times MT/s / 2000$. Round tREFI down to avoid exceeding the interval; round tRFC up to keep the cycle long enough. When changing data rate: $N_{\text{new}} = N_{\text{old}} \times MT/s_{\text{new}} / MT/s_{\text{old}}$, with the same rounding rule.

tREFI: A NOTIONAL LADDER FROM LOWER TO HIGHER

BIOS value	@ 8200	@ 8400	How to interpret it
15 990 / 16 380	3.900 μs	3.900 μs	≤85 °C: 3.9 μs normal / 1.95 μs FGR; above 85 °C: twice as often.
16 383	3.996 μs	3.901 μs	16K: the first binary reference point, nearly 3.9 μs @ 8400.
32 767	7.992 μs	7.802 μs	The first convenient notional step.
65 535	15.984 μs	15.604 μs	Approximately one quarter of the 18-bit range.
131 071	31.969 μs	31.207 μs	Half the range; a popular OC point.
262 143	63.937 μs	62.415 μs	Maximum of Intel's 18-bit field, not a stability target.

WHY SPECIFICALLY 16K, 32K, 65K, 131K, AND 262K

These are not JEDEC ratings or special electrical modes, but convenient binary boundaries of the form $2^n - 1$. On older Intel platforms, 65535 was the maximum of a 16-bit field; since at least Alder Lake, the field has 18 bits and ends at 262143. Intermediate integers are valid within the range. Example: $131071 \times 8400 / 8200 = 134267.85$; round down to 134267 at 8400.

PRACTICAL tRFC AND tRFCsb/tRFCpb TUNING

Parameter	What it means here	Starting point	Example @8200	Priority
tRFC*	The actually programmed duration of the overall refresh cycle	Auto/MRC runtime	688 = 167.80 ns	Tune first, reducing only this one parameter.
tRFCsb / tRFCpb**	Same-Bank / Per-Bank refresh; the name depends on the documentation level and platform	Auto/MRC runtime	565 = 137.80 ns	Secondary priority; reduce only after tRFC has been tested separately.

STEPS OF 16 OR 32: THE CURRENT TAKEAWAY

These are convenient search increments, not mandatory granularity. On Raptor Lake, TC_RFTP contains tRFC and tREFI; tREFIx9 is in a separate TC_RFP. On Core Ultra 200S, TC_RFTP additionally contains tRFCpb and tREFIx9. tRFC fields use 1 tCK units, and ASUS accepts any integer without a multiple requirement. Far from the limit, reduce by 32; closer to it, by 16. Transfer: $688 @ 8200 \rightarrow 688 \times 8400 / 8200 = 704.78 \rightarrow 705$ at 8400. For margin, use 720 with a step of 16 or 736 with a step of 32.

For Hynix in FGR, the guideline is tRFCpb ≈ tRFC2 – 30 ns; at 8200, tRFC2 – 123 cycles (688 → 565). The tRFC field must mean tRFC2; this is an empirical estimate, not a formula from tRFC1. Tune tRFC first, then test tRFCpb separately; raise tREFI only after restoring margin.

* JEDEC defines tRFC1/tRFC2 by refresh mode; separate tuning is not always available. Here, tRFC is the controller's runtime value. Equal BIOS numbers do not prove equal JEDEC specifications.

** JEDEC tRFCsb/REFsb and Intel tRFCpb/REFpb belong to different documentation layers. Their practical correspondence depends on the controller and BIOS; they are not universal synonyms and neither is tRFC2.

DOCUMENTATION REVIEWED: Micron DDR5 refresh operation and core timing tables; Intel 13th Gen TC_RFTP/TC_RFP and Core Ultra 200S TC_RFTP; ASUS ROG Z790 BIOS Manual (integer ranges).

MICRON: [DDR5 REFRESH](#), INTEL LGA1700: [TC_RFTP](#), INTEL 200S: [TC_RFTP](#)

03 3.7 TERTIARY TIMINGS: TRANSITIONS BETWEEN COMMANDS

Intel tertiary timings describe transitions between commands. All intervals below are in memory clock cycles. For each formula, first identify the direction, then the bank path and the utility's calculation method.

DIRECTION AND BANK PATH

RDRD - read → read; WRWR - write → write; RDWR - read → write; WRRD - write → read. WTR uses WRRD. S ↔ dg - different bank groups; L ↔ sg - the same group. The path to another bank within a group may be shorter than the overall long path L.

dr — another rank on the same DIMM: used with 2R. dd — another DIMM in the channel: used with 2DPC. With 1R/1DPC, neither path is used. Start with Auto; these timings cannot be derived from CL.

For BL16: RDRD_dg = WRWR_dg = 8. The physical references for sg differ: RDRD uses tCCD_L; WRWR uses tCCD_L_WR2 or tCCD_L_WR, depending on the write path.

WHY THE DDR4 FORMULA READS FOUR HIGHER

A DDR4 BL8 burst takes 4 cycles; a DDR5 BL16 burst takes 8. The base reverse calculation therefore changes: WTR_L = WRRD_sg - CWL - 10; WTR_S = WRRD_dg - CWL - 10; WR = WRPRE - CWL - 8. The 10 includes burst 8 and decoder correction 2.

If a program still subtracts 6 for WTR or 4 for WR, the same input fields produce a result 4 higher. Without additional corrections: CWL34, WRRD_sg64/dg52, WRPRE90 → L20/S8/WR48; the old formulas give 24/12/52.

In anta777's October 31, 2022 analysis, ASRock Timing Configurator is described as subtracting 6 for WTR, and ASUS MemTweakIt as subtracting 4 for WR; MSI Dragon Ball uses the base DDR5 relationships. ASRock calculates WR correctly there. This describes those versions, not a rule that 'all ASRock values are always +4.' Check the utility version and platform separately.

CORRECTIONS TO THE BASE CALCULATION

In pyhwinf's main calculation on Raptor Lake DDR5 from 5200: WTR = WRRD - C - 10 - B. C is the read-back controller CWL field, not automatically CL-2. B is MR8[7]: 0 for the short, 1 for the long write-signal ending. It is a setting bit, not its duration of 0.5/1.5 cycles.

With C34, B1: dg54 → S9; sg86 → L41. In reverse: WRRD = C + 10 + B + WTR. With C and B fixed, WRRD +1 gives WTR +1; if C rises by 2, the same WTR needs WRRD +2.

For WR, the code starts with WRPRE - C - 8, then adds 1 with 2N. Another calculation: WR = WRPDEN - C - 9. Thus, WRPDEN=WRPRE+1 is valid only without this correction; with it, the difference is 2.

A separate DEC/ADD branch: C' = C - DEC_tCWL + ADD_tCWL; WTR_alt = WRRD - C' - 10. It does not subtract B. With C34/DEC2/ADD0 and dg54, the result is 12. Do not combine these branches into one sum of corrections.

READ → WRITE AND PRACTICAL VALIDATION

DRAM READ→WRITE interval = CL - CWL + 8 + 2 - O + (P - 0.5) + W. O is the read-signal offset; P is the duration of its ending; W is the write-signal preparation time. CL36/CWL34 with O0/P1.5/W4 gives 17. BIOS tRDWR also accounts for the controller and training.

Compare the applied fields and the utility's calculation method, then validate under load and with cold boots. The main WTR explanation is in 3.5; compact formulas are in Chapter 11, p. 89.

03 3.8 MAINTENANCE AND POWER-SAVING TIMINGS

These parameters govern exit from idle, self-refresh, signal calibration, and maintenance commands. Tuning them alone rarely provides a measurable performance gain, but an excessively tight value can break cold boot, sleep, wake, or training repeatability.

Timing	What it specifies	Relationship or formula	How to tune it
tCKE	Power Down transition service interval; DDR5 has no separate CKE line	tPD/tXP: ≥8 CK and ≥7.5 ns tCPDED: ≥8 CK and ≥5 ns	Auto. Has no effect with Power Down disabled; 8 is neutral common practice, not a speedup.
tXP	Exit from Power Down	The greater of 8 CK and 7.5 ns	A lower value can break exit from idle.
tXS	Exit from Self Refresh	tXS(min) = tRFC1 (monolithic DDR5)	Auto; for commands requiring DLL: tXS_DLL = tDLLK.
tRDPDEN	READ -> Power Down	≈ tCL + 8 + 1	Scheduler field; related to CAS and burst length.
tWRPDEN	WRITE -> Power Down	≈ tCWL + 8 + tWR + 1	Increases with tCWL/tWR; do not lower independently.
tMRD / tMOD	Mode Register commands	IC service minimums	Not ordinary performance timings.
tZQSPeriod	ZQ calibration period	Resistance and temperature compensation	Leave on Auto; do not disable it for the sake of one test.
tOSCO / tMRR	Oscillator / mode register read	DDR5 service operations	May be visible on Z890; no manual overclocking is required.

monolithic DDR5 (DDR5 devices with a single DRAM die per package).

tCKE = 8, tXP AND PD = 0

tCKE=8 is neutral with PD=0 (Power Down Disabled). If this mode is actually disabled, tCKE/tXP and PD-entry delays do not affect this path; leave them on Auto. With PD=1, use Auto; tXP requires both 8 CK and 7.5 ns (at least 31 cycles at 8200). Sleep and self-refresh are independent of PD; leave tXS/tDLLK on Auto as well.

POWER POLICIES ARE NOT A SINGLE TIMING

Group	What it changes	Practical approach
Power Down	Entry into idle when inactive	With Disabled, tCKE does not participate. With Enabled, leave it on Auto and test idle operation and exit from idle.
Self Refresh	Memory refreshes itself without normal commands	A separate mechanism using tXS/tCKSRX; do not equate it with tCKE or tREFI.
ZQ calibration	Adjusts output resistance	Temperature-dependent; aggressive reduction lowers signal margin.
Training	Selects actual service intervals	Auto does not mean zero. Compare applied values after a cold boot.

OREF_RI: REFRESH WHEN THE RANK IS IDLE

OREF_RI sets the rank-idle duration after which an opportunistic refresh is possible. Auto is the default choice; 0 removes this threshold, but does not disable refresh and is not equivalent to PD=0. No universal benefit from 0 has been confirmed; compare it with Auto on your own system.

WHAT TO TEST BESIDES A MEMORY TEST

A daily profile must withstand not only sustained load but also transitions: a cold boot after complete power removal, several restarts, extended idle, sleep, and wake. This is where tXP, tXS, and power-state entry intervals are used.

If an error appears only after sleep, first return service intervals and power policies to Auto, then repeat the same scenario. This A/B test separates a power-state problem from cell instability more quickly.

03 3.9 CORRELATIONS: IC, RANK, DENSITY, AND CAPACITY

The same capacity does not mean the same behavior. Limits are affected by IC density and revision, rank count, modules per channel, and screening quality. Determine the kit's physical organization first; only then transfer timing logic.

Characteristic	What it changes	Which timings it affects	What to check
IC revision	Internal ranges and voltage response	tCL, tRCD, tRP, tRFC, tCWL	Marking/part number; XMP does not guarantee the revision.
Die density	Number of cells on the die	tRFC1/2/sb specifications and practical tRFC	Compare time in ns with data for the same density.
1R / 2R	Load and rank switching	Activates tertiary dr timings and changes ODT	With 2R, return dr and training settings to Auto.
1DPC / 2DPC	Number of modules and signal-path length	Activates dd, more often requires looser CR	Find frequency again, then timings.
XMP screening	Starting frequency, CL, and voltage	Does not define a universal minimum	Compare the entire profile, not just MT/s.

TYPICAL KITS AND TUNING PRIORITIES

Kit	Common organization	Typical characteristic	Tuning logic
2 x 16 GB	16-Gbit x8, 1R	Older Hynix A-die often scales down tCL well	Find frequency/tRCD first, then tCL and VDD response.
2 x 24 GB	24-Gbit x8, 1R	Non-binary Hynix M-die	At 8000+, lowering below CL36 often requires a lot of VDD for little gain.
2 x 32 GB	Depends on the specific SKU	May be 2R 16-Gbit or denser 1R	Do not draw conclusions from capacity: check SPD, rank, and density first.
2 x 48 GB	Often 24-Gbit x8, 2R	Rank-to-rank transitions are active	Find frequency, dr, and refresh settings again.

tCL AND VDD: CALCULATE THE ACTUAL GAIN

At DDR5-8200, reducing tCL from 38 to 36 cuts pure CAS latency by approximately 0.49 ns. If this requires 50-100 mV more VDD, makes the memory run hotter, and leaves tRCD/tRP unchanged, a CL38 daily profile may be the more rational choice.

CAPACITY MATTERS THROUGH ORGANIZATION

A 24 GB module built with 24-Gbit ICs remains single-rank, while a 48 GB module using the same ICs usually requires two ranks. In the latter case, the controller gains more parallelism but must also switch ranks and train additional dr paths.

When moving from 48 GB to 96 GB, retest frequency, tertiary transitions and refresh, even with the same IC revision.

CUDIMM improves the clock path through CKD, but does not change the meaning of tCL, tRCD, tRFC, or tertiary transitions. When transferring a profile, preserve relationships and time in ns, not absolute values.

03 3.10 ASUS Z790 APEX ENCORE BIOS 2202

In this chapter, I use the ASUS ROG Maximus Z790 Apex Encore with BIOS 2202 as the reference. The official manual confirms the overall structure, but the individual entries depend on firmware, processor, and modules. Setting names are given exactly as ASUS labels them.

AUTO ON APEX IS A VALID STARTING POINT

On the Apex BIOS versions I tested, secondary and tertiary timings train correctly on Auto. After a cold boot, save the values actually applied, including Runtime, and begin careful reduction from that baseline.

MAP OF THE DRAM TIMING CONTROL SECTION

ASUS group	What it contains	How to use it
Primary Timings	tCL, tRCD Read/Write, tRP, tRAS, Command Rate	Main timing string; Read and Write are shown as separate fields.
Secondary Timings	tRRD, tFAW, tRFC, tREFI, tWR, tRTP, tWTR, tCWL	Activation, recovery, and refresh.
Third Timings	tRDRD, tWRWR, tRDWR, tWRRD with sg/dg/dr/dd	Controller transitions; use trained values as the reference.
Misc. Timings	Power Down, Self Refresh, ZQ, and service intervals	Leave on Auto unless addressing a specific diagnostic problem.
Memory Training Algorithms	Interface training and matching algorithms	Covered in detail in Chapter 05; do not confuse with a timing.

EXACT FIELDS MOST OFTEN SET MANUALLY

ASUS name	In brief	Relationship	BIOS 2202 nuance
DRAM CAS# Latency	tCL	READ -> data	For DDR5, an odd value is rounded up.
RAS# to CAS# Delay Read / Write	tRCDRD/WR	ACT -> RD/WR	Two fields; equal values can be used as a starting point, but this is not a universal requirement.
DRAM RAS# PRE Time	tRP	PRE -> ACT	Tested during row changes.
DRAM RAS# ACT Time	tRAS	ACT -> PRE	Compare with tRCDRD+tRTP .
DRAM REF Cycle Time 2	tRFC	Refresh	This manual refers to the field neutrally as tRFC; the ASUS name alone does not prove active 2x FGR.
REF Cycle Time Same Bank	tRFCsb	One bank in each group	The other banks remain available during the cycle.
WRITE to READ Delay L / S	tWTR_L/S	End of WR data -> RD	Related to tWRRD_sg/dg.
DRAM Write Latency	tCWL	WRITE -> data	The CL36 baseline uses CWL34.
tRDRD_sg/dg Training / Runtime	RDRD	RD -> RD	Runtime is the actual operating interval; this is the value to record.

TRAINING AND RUNTIME

Training refers to finding an operating range during memory training; Runtime refers to the interval actually used by the scheduler after startup. Auto is not an empty value: before manual tuning, save the actual numbers after a cold boot.

WHAT TO RECORD BEFORE MANUAL ENTRY

After full training, save the frequency, Gear, Command Rate, all primary and secondary timings, the tRDRD/tWRWR/tRDWR/tWRRD groups, module temperature, and BIOS version. For fields with Training/Runtime, record Runtime specifically.

After startup, the MRC may round an entered value to a valid code or apply an internal constraint. Use the actual post-boot value as your reference.

03 3.11 ASUS Z890 APEX: WHAT CHANGED

The meaning of the main DDR5 timings has not changed on Z890, but ASUS reorganized the menu for Core Ultra 200S, CUDIMM, and the new MRC. Transfer the logic and relationships from Z790, not every number or field name. The table is based on the public ROG Z890 manual; the specific entries depend on BIOS, CPU, and DIMM.

Area	Z790 Apex Encore 2202	Z890 Apex	Practical takeaway
Profiles	Maximus Tweak	Memory Presets; DIMM Fit / Fit Store	DIMM Fit is a new training tool, not a renamed Tweak.
Command Rate	1N, 2N, 3N, N:1	1N / 2N in the public menu	2N remains the baseline for high-frequency DDR5.
tCCD	Separate fields are not shown	tCCD_L and tCCD_L_WR added	Long read and write paths are easier to see.
Refresh*	tRFC1, tRFC2, tRFCsb, tREFI, and extended fields	Publicly: tRFC, tRFCsb, tREFI; tRFM added	RFM is a refresh-management mechanism for frequent activations; tRFM is the duration of an RFM cycle. Neither replaces tRFC.
tRDRD	Training and Runtime separate	One final entry in the public menu	Training itself remains; manual separation of the fields is gone.
Power	Scattered Power Down fields	Explicit modes, thresholds, and counters by subchannel	Configuration is more detailed, but leave it on Auto for timing overclocking.
Divide DRAM timings	No separate entry in the public manual	Single Divide DRAM timings entry	This encodes field ranges; it is neither Gear 4 nor a way to reduce latency.
Training	Baseline algorithms and Round Trip	Training Consistency; Rank-to-Rank; more PHY settings	Test repeatability after a cold boot.

NEW AND HIDDEN FIELDS

Group	What is visible on Z890	How to interpret it
Added	tCKCKEH, tCA2CS, tOSCO, tMRR, tRPab, tccdByteCasDelta, tRFM, tSR, tZQCSPeriod, tMRD	Some service parameters and mechanisms became visible; this is not a mandatory manual-overclocking list.
Not shown	tRFC2, tREFIX9, Ref Interval, tXPDLL, tMOD, tZQOPER, and low-level refresh debt/PBR fields	The absence of an entry from the public menu does not prove that the mechanism disappeared from the MRC.
Not renamed	tRPab ext ≠ tRPab; tMOD ≠ tMRD; tZQOPER ≠ tZQCSPeriod	Similar names cannot be carried over as direct equivalents.

CUDIMM AND CKD

CKD restores the clock signal on the module, but does not change the meaning of tCL, tRCD, or tRFC. CUDIMM adds CKD settings: CKD Skew Control, PLL Bypass, and PLL modes. Dual PLL was added in BIOS 1203. PLL Bypass disables the primary advantage of CKD; it is used for compatibility and diagnostics.

WHAT TO TRANSFER FROM Z790 AND WHAT TO FIND AGAIN

You can transfer the meaning of settings, the $tRC=tRAS+tRP$ formula, the tRRD/tFAW and tWTR/tWRRD relationships, and the approach of converting cycles to nanoseconds from Z790. Frequency, voltages, training results, and PHY-dependent values must still be found again.

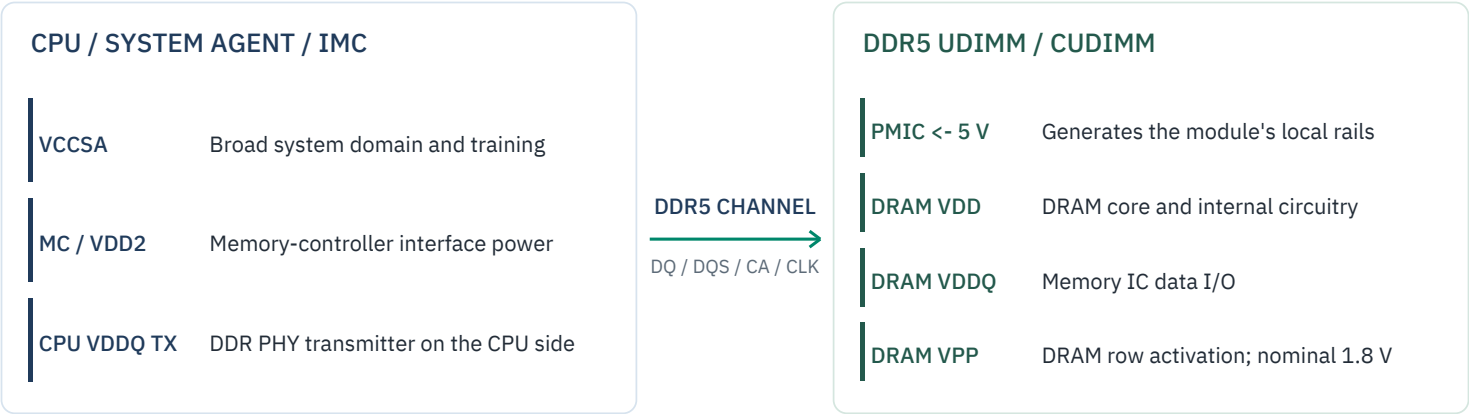
Do not search for Z890 entries absent from the public manual under similar names and fill them with Z790 numbers. Start with Auto and the actual value, then confirm the function for the specific BIOS version.

Leave Divide DRAM timings on Auto until a field-range limitation appears. It has no universal 9600 MT/s threshold: the BIOS/MRC decides according to frequency and the encoding of the specific timing.

* For Raptor Lake-S, public Intel documentation states that DDR5 RFM is not enabled. The presence of a similar BIOS entry alone does not prove that the mechanism is active on a specific platform.

04 4.1 POWER MAP / 4.2 CPU SYSTEM AGENT

DDR5 overclocking depends not on one voltage, but on a chain of several independent domains. Some are inside the processor, some belong to the channel's electrical interface, while VDD, VDDQ, and VPP are generated by the PMIC on the module itself. First separate these areas physically; only then look for a relationship with the error.



VDDQ APPEARS MORE THAN ONCE - IT IS NOT ONE RAIL

DRAM VDDQ powers data I/O on the DIMM's memory ICs. On Z790, IVR Transmitter VDDQ applies to the CPU transmitter. On Z890, Vddq Voltage Override is in the CPU-side Advanced Memory Voltages block. In both cases, VDDQ identifies an I/O-domain voltage in the DQ/DQS data path, but on opposite sides of the CPU-DIMM interface; they are functionally related but electrically independent power rails.

HOW TO READ THE NUMBER SHOWN BY THE BIOS

Value type	Example	What it means
Setpoint	SA, TX, MC, DRAM VDD/VDDQ	Requested value. It need not match the voltage at the measurement point.
Auto / training	MRC selects Vref, ODT, and delays	Auto is an algorithm result, not zero. Full retraining is required after changing one voltage.
Calculation base	MC/VDD Calculation Voltage Base	Firmware reference for calculations; not another physical rail.
Telemetry	IVR VCCSA, VDDQ TX, IMC VDD, PMIC	Compare readings from the same sensor under the same load.

4.2 CPU SYSTEM AGENT VOLTAGE: A BROAD SYSTEM DOMAIN

VCCSA powers the System Agent, a broader domain than the memory controller alone. SA therefore affects the overall memory and uncore operating point as well as MRC repeatability, but is neither a DRAM voltage nor a substitute for separate VDD2. On Z890, SA remains part of the overall uncore/NGU operating point, but does not directly power D2D: D2D has separate domains and ratios.

Insufficient SA may appear as POST loops, poor cold boot, or inconsistent training results. Too much can cause the same symptoms: noise, reference levels, and the PHY range found by training all change. Find a repeatable range in small steps, not the highest possible number.

THE BIOS INPUT LIMIT IS NOT A RECOMMENDATION FOR A PERMANENT PROFILE

ASUS permits a much wider input range than ordinary DDR5 overclocking requires. Even VCCSA <= 1.20 V from Intel 200S Boost applies to a specific Core Ultra 200S, Z890, 1DPC profile; it does not declare a universal safe limit for every platform.

04 4.3 CPU VDDQ TX / 4.4 MEMORY CONTROLLER VDD2

On ASUS Z790, the IVR Transmitter VDDQ Voltage entry literally sets the internal transmitter voltage of the memory controller. This is part of the CPU-side channel: it participates in shaping DQ/DQS edges, write training, Vref/ODT, and electrical margin at high speed.

TX state	What we usually observe	How to interpret it
Insufficient	Unstable write training, early data-path errors, dependence on MT/s	The first suspect, but not a complete diagnosis: MC, DRAM VDDQ, ODT, and PHY operate alongside it.
Operating range	Cold boots are repeatable; Vref and trained intervals do not vary	Record the center of the passing range, not one successful boot.
Excessive	Increasing it no longer helps or immediately worsens training	The stable operating range may narrow because of edge overshoot, crosstalk, and incorrect balance with the other side of the channel.

TX VDDQ AND DRAM VDDQ OPERATE ON OPPOSITE SIDES OF THE CHANNEL

They do not have to be equal, and there is no universal "correct" delta between them. Hold the other side at a known-stable value, then change only one voltage in small steps with full retraining.

On Z890, the separate IVR Transmitter VDDQ name is gone. Advanced Memory Voltages adds VccDdqControl Bypass and Vddq Voltage Override, alongside VccIog and VccClk fields. The public ASUS manual confirms these low-level CPU/PHY-side settings, but does not disclose their exact electrical mapping. Vddq Override is functionally similar to the former TX domain, but cannot be treated as a 1:1 rename or assigned a copied Z790 value.

4.4 MEMORY CONTROLLER VOLTAGE / VDD2: IMC INTERFACE POWER

ASUS calls this rail Memory Controller Voltage on both Z790 and Z890. Its hardware name in Intel documentation is VDD2: power for the memory-controller interface and processor DDR I/O. HWiNFO usually shows it as IMC VDD. It is neither the module's VDD nor TX VDDQ.

Factor	Why it changes the load	Practical takeaway
MT/s and Gear	The controller and PHY have less time to process data	MC often contributes to the frequency limit, but raising it does not replace a realistic frequency.
2R	More ranks, receivers, and switching within the DIMM/channel	First find frequency, ODT, and training again; do not raise MC automatically.
2DPC	A second DIMM adds electrical load and line branches	Account for motherboard topology and retest frequency, ODT, and training.
Die density	Changes DRAM internal organization and refresh	Affects MC indirectly; more strongly related to VDD, tRFC, tREFI, and temperature.
Excessive MC	Power consumption, heat, and noise within the CPU increase	If a higher value does not widen the range, it is extra load rather than margin.

WHAT TO LEAVE ON AUTO

MC/VDD Calculation Voltage Base entries are firmware calculation references. Memory Controller Boot Voltage is a temporary startup setpoint, while Eventual Memory Controller Voltage is the final operating setpoint. These are not additional physical rails. The Boot/Eventual names belong to specific Z790 BIOS versions and may be absent from the public Z890 menu; unless a problem specifically during the transition from boot to runtime has been confirmed, leave these fields on Auto.

04 4.5 DRAM VDD/VDDQ / 4.6 VPP, PMIC, AND SPD HUB

DRAM VDD and DRAM VDDQ reside on the module itself and are generated by its PMIC. VDD powers the DRAM core, while VDDQ powers the IC data I/O. The nominal DDR5 starting point is 1.10/1.10 V; XMP almost always raises both rails because it overclocks frequency and timings simultaneously.

Rail	Physical role	More commonly related to	What limits it
DRAM VDD	DRAM core, array, and internal peripheral circuitry	tCL, some internal timings, and the individual tRFC minimum	IC revision and screening, temperature, and the early tRCD/tRP plateau.
DRAM VDDQ	Data transmitters/receivers on the DIMM	Signal margin during data writes/transfers, VrefDQ, and turnarounds together with CPU TX and MC	Channel quality, ODT, and training; further increases may worsen the result.

HOW VOLTAGES RELATE TO FREQUENCY AND TIMINGS

Change	Typical response	Why you cannot increase it blindly
MT/s	Affects VDD/VDDQ, but also TX, MC, SA, and training	A frequency limit is rarely solved by one module voltage.
tCL	On Hynix, it often responds more noticeably to VDD	On 24-Gbit M-die, attempting to go below CL36 may require a lot of VDD for no useful gain.
tRCD / tRP	IC architecture often becomes the limit sooner	After the plateau, excess VDD only adds heat.
tRFC / tREFI	Depend on density, revision, and temperature	Higher VDD can heat the DIMM and worsen refresh stability after warm-up.

EQUAL VDD/VDDQ IS A CONVENIENT BASELINE, NOT A LAW

Starting with equal XMP values is convenient. Set different voltages for the two rails only after establishing a stable baseline: hold one constant and test the other in small steps. Using different values remains additional overclocking.

4.6 MODULE SERVICE RAILS AND PMIC CONTROL

ASUS entry	What it does	Practice used in this manual
High DRAM Voltage Mode	Unlocks the range above the usual 1.435 V when supported by the module	Does not raise anything by itself. The BIOS maximum of 2.070 V is not a safe recommendation.
DRAM VPP Voltage	Row-activation power; nominal 1.8 V	Do not change.
SPD HUB VLDO / VDDIO	SPD Hub logic power at 1.8 V and sideband at 1.0 V	Auto; problems here are more closely related to SPD, the sensor, and PMIC control.
Sync All / By per PMIC	Identical or separate module programming	Synchronized adjustment is convenient for modules in one kit; adjust separately only after confirming a difference. Even a matched kit does not guarantee equal temperature and telemetry.
Switching Frequency / Current	Converter mode and PMIC current limit	Leave on Auto until measurable droop or a PMIC error appears; this is not another power rail.

CUDIMM AND CKD DO NOT CHANGE THE MEANING OF THE MAIN POWER RAILS

CKD restores the clock signal and can operate in Single PLL, Dual PLL, or Bypass. There is no separate CKD Voltage in the public ASUS Z890 BIOS: VDD/VDDQ/VPP are DRAM/PMIC rails, while PLL and Gear 2/4 are different settings.

04 4.7 CORRELATION AND SWEET SPOT / 4.8 ASUS Z790 AND Z890

Every voltage has an operating range. Below it, electrical margin is insufficient; above it, edge rate, Vref, ODT, noise, and heat change, and after full retraining the operating range may narrow again. The dynamic component of power scales roughly as $P_{dyn} \sim C \times V^2 \times f$, so a small increase in V at high frequency noticeably affects heat.

Problem type	First suspects	What to check before increasing	Suitable test
No POST / training loop	MC/VDD2, CPU VDDQ, SA, frequency	Gear, 1DPC/2DPC, ODT, several cold boots	POST codes and retraining
Early write/data errors	DRAM VDDQ, CPU TX, MC	tWR/tWTR/turnaround and trained Vref	Karhu/TM5 with emphasis on writes
VT3 fails	MC, TX, SA, and interaction with CPU/ring	Separate a memory error from heavy CPU load	y-cruncher VT3
Errors only after warm-up	VDD, tREFI/tRFC, cooling	DIMM temperature and lowering tREFI	Karhu/TM5 after warm-up with monitoring
Cold boot / sleep only	Training, startup setpoints, power state	Fast Boot, saved data, and Auto service fields	Cold boots, sleep/wake

THE OPERATING POINT OF A PERMANENT PROFILE IS THE CENTER OF THE RANGE, NOT ITS EDGE

Fix frequency, Gear, timings, trained values, and temperature; change one voltage; perform full retraining and several cold boots. Find the lower boundary in small steps, and move upward only within a predefined reasonable range, stopping if there is no improvement or temperature rises. There is no need to deliberately raise voltage until errors appear. Leave the final value inside the repeatable range with a small margin; no error code identifies a specific rail unambiguously.

My Z790 Apex Encore / BIOS 2202 / 2 x 24 GB / DDR5-8200 profile uses SA 1.22; TX 1.35; MC 1.40; VDD 1.49; VDDQ 1.44 V. Telemetry shows similar but unequal numbers. This illustrates the difference between setpoints and sensor readings; it is not a ready-made profile or safe range.

4.8 EXACT ASUS NAMES: THE SAME MEANING DOES NOT ALWAYS USE THE SAME NAME

Function	Z790 Apex Encore 2202	Z890 Apex	How to transfer it
System Agent	CPU System Agent Voltage	CPU System agent Voltage	Name retained; do not copy the numbers because of the new NGU/D2D architecture.
CPU-side VDDQ	IVR Transmitter VDDQ Voltage	VccDdqControl Bypass + Vddq Voltage Override	Functionally similar, but not a confirmed 1:1 rename.
IMC / VDD2	Memory Controller Voltage	Memory Controller Voltage	Main CPU-side memory rail; HWiNFO often shows IMC VDD.
DRAM core/data	DRAM VDD Voltage / DRAM VDDQ Voltage	Same exact names	Module PMIC rails; do not confuse DRAM VDDQ with CPU Vddq Override.
PMIC / SPD / VPP	PMIC Voltages; SPD HUB; DRAM VPP	Same groups; PMIC0-1 on Apex	Leave service settings on Auto unless asymmetry has been demonstrated.
Z890 auxiliary fields	No separate public entries	VccIogControl Bypass; VccIog Voltage Override; VccClkControl Bypass; VccClk Voltage Override	Low-level CPU/PHY fields; exact electrical role is not publicly disclosed. Leave on Auto without specific diagnostics.
D2D / always-on	No	VNNAON 0.77v Voltage; NGU Ratio; CPU D2D Ratio	Not a DRAM voltage: leave on Auto/stock values for ordinary memory tuning.

INTEL 200S BOOST IS A REFERENCE FOR A SPECIFIC PROFILE, NOT A UNIVERSAL LIMIT

For compatible Core Ultra 200S K/KF/Plus processors, Z890, 1DPC, and a suitable XMP profile, Intel specifies up to DDR5-8000 with $VDD2 \leq 1.40\text{ V}$, $VCCSA \leq 1.20\text{ V}$, and module $VDD/VDDQ \leq 1.40\text{ V}$. This is an official conditional OC profile; manual 9200+ is outside its scope.

04 4.9 VOLTAGE RANGES AND THE EFFECT OF COOLING

The ranges below are very approximate guidelines based on my personal opinion. There is no single official safe range for manual overclocking: platform, IC type and density, rank count, number of modules, and other factors all matter.

VOLTAGE RANGES, V

Rail / platform	Working OC (V)	Not recommended (V)
DRAM VDD ¹	1.45-<1.52 ² ; 1.45-<1.55 ³	>1.55
Z690 · VCCSA	1.20-1.30 ⁴	>1.35
Z690 · IVR TX VDDQ	1.20-1.35	>1.35
Z690 · MC / VDD2	1.25-1.40	>1.40
Z790 · VCCSA	1.10-1.30	>1.40
Z790 · IVR TX VDDQ	1.20-1.40	>1.45 ⁵
Z790 · MC / VDD2	1.25-1.45	>1.50
Z890 · VCCSA	1.00-1.20	>1.35
Z890 · MC / VDD2	1.20-1.40	>1.50

Official Z890 reference: Intel 200S Boost - SA ≤1.20 V.

¹ A-die, non-binary M-die; ² air; ³ water; ⁴ reduce only while retaining stability, down to 1.10–1.15 V; ⁵ in my observations within the community, sustained TX VDDQ >1.45 V coincided with cases of failed 13900K and 14900K processors. These are observations, not a confirmed failure threshold.

DRAM VDD AND VDDQ: TUNED SEPARATELY

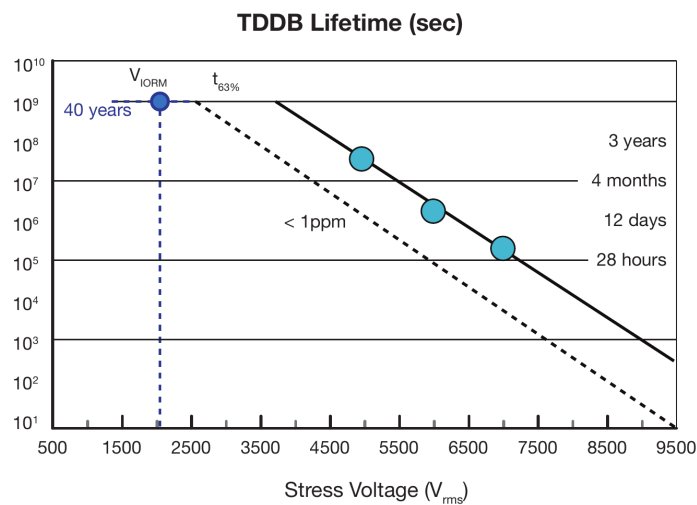
VDD powers DRAM circuitry; VDDQ powers I/O. The rail-to-rail voltage difference is limited by IC/PMIC specifications; maximum ratings are not operating conditions. No safe OC delta has been established. Fix VDD, frequency, and timings, then lower VDDQ in 10-20 mV steps. After warm-up and several complete training cycles, find the lower passing boundary, then select a value with a small margin inside the repeatable range. Passing tests does not prove that an overclock is safe.

A MEMORY WATER BLOCK: GOOD THERMAL HEADROOM

With good contact and cool liquid, a water block reduces DIMM temperature and provides headroom for timings, frequency, or lower voltage. If the limit is already the IMC or signal quality, there may be no gain.

Comparison of the same 2 x 24 GB M-die pair: for 8200 CL34, a 140 mm fan at 800 rpm required 1.56 V at 49.2/48.5 °C; the water block required 1.50 V at 31.2/31.0 °C. This was AM5, voltages were tuned separately, and validation was 1 hour of Karhu plus about 25 minutes of TM5. Temperature was read from the SPD Hub; I did not study service life. The example is provided for comparison.

LOW TEMPERATURE DOES NOT ELIMINATE ELECTRICAL STRESS



Higher voltage increases the electric field in the dielectric. Prolonged exposure gradually degrades its insulating properties and may end in breakdown: TDDB. Heat accelerates several aging mechanisms.

A water block reduces temperature, not the electric field from the configured VDD/VDDQ. A cold module can therefore pass tests while still losing service life. Lower temperature reduces the thermal component of risk; it does not make high voltage safe.

In the TI graph, the X-axis is voltage and the Y-axis is time to breakdown on a logarithmic scale. The higher the test voltage, the shorter the time. The points represent failure of 63% of samples; the dashed line predicts a 1 ppm failure rate.

TI, SSZY028 (2017), Fig. 5. High-voltage insulators. The voltages and service lives shown do not apply to DDR5. The figure illustrates the principle.

DOCUMENTATION REVIEWED: Intel 200S Boost; PhoenixMDA: voltage and cooling measurements; Texas Instruments SSZY028, Fig. 5.

[Intel 200S Boost, Comparison of one 2 x 24 GB M-die pair, TI, SSZY028 \(2017\), Fig. 5.](#)

05 5.1 PREPARATION / 5.2 WHERE TO START

Tuning starts not with someone else's timings, but with a repeatable baseline. First prove that the system works correctly on clean JEDEC/Auto, then establish a separate XMP baseline. Old manual voltages, trained values, or hidden profile settings must not be carried between these modes.

TWO BASELINES FOR TWO DIFFERENT TASKS

Mode	What to apply	What it is for
JEDEC / Auto	Load Optimized Defaults, XMP disabled; perform full training	Verify assembly, slots, SPD, boot, and baseline operation without overclocking.
XMP II	The complete set of parameters in the DIMM's XMP profile; BIOS/MRC determines parameters absent from the profile.	The original XMP baseline for comparison; loading XMP II does not exclude BIOS/MRC involvement.
XMP I	Main DIMM XMP fields with the remaining parameters optimized by ASUS	A separate comparison branch; do not mix its results with XMP II.
XMP Tweaked	XMP plus additional ASUS settings for compatible kits	Enhanced ASUS profile: test only after establishing a stable baseline.

RECORD FOR EACH SESSION

Record	Exact information	Record	Exact information
Platform	CPU, motherboard, BIOS version, and ME	Kit	Part number, total capacity, 1R/2R, die density
Installation	A2/B2 on a 4-DIMM board or both Apex slots; record DIMMs per channel separately	Module type	UDIMM/CUDIMM, XMP profile, CKD mode if present
Conditions	DIMM airflow, room temperature	Readings	BIOS setpoints and HWiNFO sensor readings
Result	Boot type, Q-Code (diagnostic POST code), training time	Validation	Test, duration, temperature, and exact symptom

5.2 ORDER FOR SELECTING THE INITIAL LOAD



WHAT INVALIDATES THE ESTABLISHED BASELINE

Changing the CPU, DIMM count or rank, occupied slots, UDIMM/CUDIMM type, BIOS version, or making a major change to frequency/Gear (the controller divider) requires retesting the corresponding earlier stage.

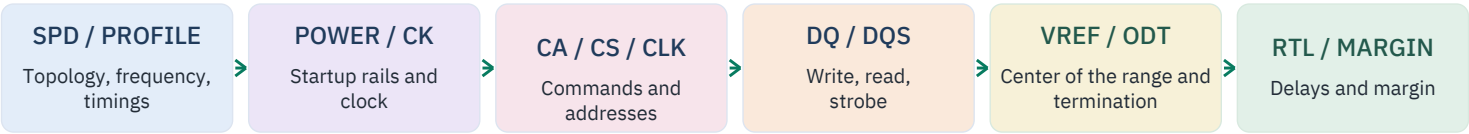
WHY THE ORDER STARTS WITH CAPACITY, NOT MT/s

Capacity determines the available module organization and electrical load before an impressive frequency is chosen. A 2 x 48 GB kit usually requires a different strategy from 2 x 24 GB, even with the same IC manufacturer: rank count, training, ODT, temperature, and the controller's realistic ceiling all change.

Gear (the controller divider) and Command Rate (the command interval) are selected after the target load. Only then does it make sense to find useful SA, TX, MC, VDD, and VDDQ ranges. This keeps every failure explainable and prevents excess voltage from masking an incorrectly chosen baseline.

05 5.3 WHAT THE MRC TRAINS / 5.4 BOOT TYPES

Memory Reference Code (MRC) is part of Intel firmware that selects working delays, reference-voltage levels, termination, and signal compensation during startup. The result is a set of parameters with which the system can continue booting. This is not a stability test under load and not an automatic search for the best timings.



5.4 THE SAME PROFILE MAY FOLLOW DIFFERENT BOOT PATHS

Scenario	What happens	What it proves
Full training	MRC reruns the required set of stages; POST takes noticeably longer	Repeatability of the range found during retraining, but not stability in Windows.
Warm restart	Warm restart without removing power; a fast path may be used	Only the profile's ability to restart through this path.
S5 / shutdown	The OS has shut down, but the motherboard may remain on standby power	Not equivalent to removing power and does not guarantee full retraining.
AC cold start	Cold boot after complete power removal	Does not promise a full MRC run if firmware uses saved data.
MRC Fast Boot / Fast Boot	BIOS applies a shortened MRC path	Saves time only after repeatability of full training has been demonstrated.
BIOS Fast Boot	Speeds up overall POST and device initialization	This is not the same as the MRC fast path.
Windows Fast Startup / sleep	The OS restores saved state or resumes from sleep	A separate scenario; does not replace cold/warm boot.

ASUS SERVICE SETTINGS

BIOS entry	Purpose	How to use it
MRC Fast Boot (Z790) / Fast Boot (Z890)	Shortened path through MRC	Disable while finding a profile; enable after a series of full training cycles.
MCH Full Check	Full MCH check; ASUS associates Enabled with stability	Auto/Enabled for a daily profile; Disabled only for a limit experiment.
Mem Over Clock Fail Count	Number of failed POST attempts before recovery	Do not set too high: a large number only prolongs a failed training loop.
Training Profile	Auto / Standard Profile / ASUS User Profile	Start with Auto; the internal difference is not publicly disclosed.
Mrc Training Loop Count	Exponential number of internal cycles	Not an OS stress test; leave on Auto without a specific diagnostic task.
Improve Training Limit (Z790 2202)	The entry exists in firmware, but its exact logic is not publicly described	Leave on Auto; do not assign it an invented frequency or voltage limit.
Memory Test on Warm Boot (Z790 2202)	Basic memory check on a warm restart; the entry may be hidden	For diagnostics only; does not replace OS testing.
Realtime Memory Timing	Allows timings to be changed after MRC_DONE	Disabled for the normal methodology; recheck the result after a full POST.

THE KEY DISTINCTION

A successful POST means only that the MRC found parameters with which the system can boot. An error may appear later after warm-up, under another load, or during the next full training cycle. Training and testing are therefore two consecutive but distinct stages.

05 5.5 TRAINING ALGORITHMS - ASUS Z790

The table combines the public ASUS Z790 BIOS manual with the actual Apex Encore BIOS 2202 menu. In Auto, MRC/ASUS selects the state of each function. The final column is my practical A/B scheme for Z790 Apex Encore / BIOS 2202 / 2 x 24 GB DDR5-8200. For another motherboard, CPU, kit, or BIOS, start with Auto.

Group	BIOS entries (similar items grouped)	What it trains	Mode
Commands / CA	Early Command Training; Command Voltage Centering; Early Command Voltage Centering; Late Command Training; CMD CTL CLK Slew Rate; CMD/CTL DS & E 2D; CMD/CTL Drive Strength Up/Dn 2D	Timing, Vref, drive strength, and edges of the command/address path.	Auto
Initial read	SenseAmp Offset Training; Early ReadMPR Timing Centering 2D; Read MPR Training; Receive Enable Training; Receive Enable Centering 1D	Receiver calibration, MPR, and read-gate timing; affects RTL.	Auto; do not disable Receive Enable
Write	Jedec Write Leveling; Early Write Time Centering 2D; Write Timing Centering 1D; Write Voltage Centering 1D; Write Timing Centering 2D; Write Voltage Centering 2D	DQS-to-CK alignment and write-eye centering.	Auto / stock; do not disable JEDEC WL
Read	Early Read Time Centering 2D; Read Timing Centering 1D; Read Timing Centering with JR; Read Voltage Centering 1D; Read Timing Centering 2D; Read Voltage Centering 2D	One- and two-dimensional search for the center of the read eye in time and Vref.	Auto; Early Read Time 2D - Enabled for 8000+*
ODT / RON / drive	Dimm ODT Training; Max RTT_WR; DIMM RON Training; Read ODT Training; DIMM CA ODT Training; Write Drive Strength/Equalization 2D; Write Slew Rate Training; Write Driver Strength Training; Write Drive Strength Up/Dn independently	DIMM/channel termination and drive strength. Manual Ω values are covered in 5.9.	Auto; Max RTT_WR - ODT OFF, 120 Ω for A/B only
Equalization	Read Equalization Training; Read Amplifier Training	Correction of receiver-path loss and distortion.	Auto
Compensation	Comp Optimization Training; TxDqTCO Comp Training; ClkTCO Comp Training; TxDqsTCO Comp Training; VccDLL Bypass Training; PanicVttDnLp Training; Read Vref Decap Training; Vddq Training	PVT, PHY delays, DLL, and reference levels; do not transfer between CPUs/BIOS versions.	Auto; Vddq: Auto → Disabled after voltages are fixed*
DCC	Duty Cycle Correction Training; Periodic DCC; Tx Dqs Dcc Training	Correction of CK/DQS duty cycle and its drift.	Auto
RTL / transitions	Round Trip Latency; Turn Around Timing Training	Round-trip delay and RD↔WR intervals; related to frequency, WTR, ranks, and topology.	RTL - Enabled; TAT: Auto → Disabled after manual turnaround settings*
DDR5 signal	DIMM DFE Training; EARLY DIMM DFE Training; DRAM EMPHASIS Training; DRAM DCA Training; DQS OFFSET ADJUST Training	DFE/DCA; DRAM EMPHASIS and DQS OFFSET ADJUST behavior is not disclosed.	Auto
Margin / test	Rank Margin Tool Per Bit; Rank Margin Tool; Memory Test; DIMM SPD Alias Test; Post Package Repair Training; Retrain Margin Check; Margin Check Limit; Margin Limit Check L2	Service margin checks; do not prove OS stability.	Auto; RMT/Test - temporarily Enabled for diagnostics
Not for this manual	LPDDR DqDqs Re-Training	Applies to LPDDR, not desktop DDR5 DIMMs.	Not applicable

* For my Z790 Apex Encore / BIOS 2202 / 2 x 24 GB DDR5-8200: I enable Early Read Time 2D at 8000+, disable TAT only after manually setting turnaround/WTR values, and disable Vddq Training after setting fixed CPU TX VDDQ and DRAM VDDQ values and completing several successful cold-training cycles. Start with Auto on another platform. BIOS 2202 uses the name Early Read Time Centering 2D; some manuals use Timing.

055.6 TRAINING ALGORITHMS - ASUS Z890

The Z890 menu exposes more PHY/MRC stages. The starting scheme below uses the ASUS manual and my recommendations. I leave most stages on Auto; choices for manual timing adjustments are shown in the table and Chapter 06.

Group	BIOS entries (similar items grouped)	What it trains	Mode
Commands / CA	Early Command Training; CA ODT Optimization; Command Voltage Centering; Late Command Training; CMD CTL CLK Slew Rate; CMD/CTL Drive Strength; CMD/CTL Tx Equalization; DIMM CA ODT Training	Command/address path, its termination, drive strength, and equalization.	Auto
Initial read	SenseAmp Offset Training; Early ReadMPR Timing Centering 2D; Read MPR Training; Receive Enable Training	Preparation of receivers and MPR data-capture boundaries.	Auto; do not disable Receive Enable
Write	Jedec Write Leveling; Early Write Time Centering 2D; Unmatched Write Time Centering 1D; Write Timing Centering 1D/2D; Write Voltage Centering 1D/2D	Write leveling/centering; Unmatched details are undisclosed.	Auto; do not disable JEDEC WL
Read	Early Read Time Centering 2D; Read Timing Centering 1D/2D; Read Voltage Centering 1D/2D; RxVref Per-Bit Training	Read-eye center in time/voltage and RxVref Per-Bit Training.	Auto; change Early Read Time 2D only as a separate A/B test
ODT / RON	DDR5 ODT Timing Config; Read DQS ODT Training; Read DQ ODT Training; Dimm ODT Training; DIMM RON Training	DQ and DQS are separate; enter manual resistances from the trained baseline.	Auto
EQ / DFE	Read Equalization Training; Read CTLE Training; DIMM DFE Training; Ddr5 Rx Cross-Talk Cancellation; Write Drive Strength; Write Equalization	Correction of frequency-dependent loss, reflections, and crosstalk.	Auto; do not disable DFE without an A/B test
Compensation	TxDqTCO Comp Training; ClkTCO Comp Training; Pre Training Comp Calibration; Comp Optimization; Ref PI Calibration; Rx SAL Calibration; VccClk FF Offset Correction; Data PI Linearity Calibration; Unmatched Rx Calibration; LVR Auto Trim	Phases, delays, PVT, and PHY power; do not transfer between CPUs/BIOS versions.	Auto
DCC	Duty Cycle Correction Training; Downstream; QCLK; Rise/Fall; Functional DCC for DDR5 DQS, CLK and Data DQ	Extended duty-cycle correction for different DDR5 paths.	Auto
Mapping / ranks	DQ/DQS Swizzle Training; Write Rank-to-Rank Training; Read Rank-to-Rank Training; Turn Around Timing Training; Write DQ/DQS Retrain	Line mapping, rank-to-rank transitions, and DQ/DQS retraining.	Auto; TAT Disabled with manual tertiary timings
Margin / protection	Rank Margin Tool; Rank Margin Tool Per Bit; Retrain Margin Check; Margin Check Limit; Margin Limit Check L2; Row Hammering Prevention; Post Package Repair	Signal margin, retraining decisions, and protection; does not replace OS tests.	Auto; margin checks for diagnostics only
Service	View Pin Calibration; Power Saving Meter Update; Read Vref Decap Training; Vddq Training; DIMM SPD Alias Test	Service calibrations and checks; internal logic is not fully disclosed.	Auto; disable Vddq Training only as a separate A/B test
Not for DDR5 DIMMs	Functional DCC for LP5 WCK; Duty Cycle Correction for LP5 DCA	LPDDR5 entries in the shared menu do not apply to UDIMM/CUDIMM.	Not applicable

WHAT CANNOT BE CARRIED OVER LITERALLY FROM Z790

E25061 has no separate Round Trip Latency entry. If one appears in the BIOS, record the version and test it separately. With manual tertiary timings, I leave TAT Disabled (§6.9). Start with Vddq Training on Auto on Z890; test the Z790 disabling scheme separately. Enabled is not a universal recommendation for Early Read Time 2D on Z890.

05 5.7 RTL/IOL TRAINING

WHAT RTL IS ON DDR5

RTL is Round-Trip Latency, the delay of the full read path. In Intel documentation for Alder Lake / Raptor Lake, it is the interval from the READ command until the first data returns to the memory controller, expressed in QCLK cycles. Training selects receiver parameters while accounting for the CPU, motherboard, modules, and settings. RTL is not CAS or AIDA64 latency.

IOL is I/O Latency. On DDR4, it is a separate I/O delay setting. On DDR5, receiver parameters and their availability depend on the platform and BIOS; the old RTL/IOL pairing cannot be carried over.

Conditional conversion of RTL to time

The conversion below applies when the displayed RTL value corresponds to a number of QCLK cycles and $tQCLK = Gear \times tCK$ has been confirmed for the selected mode. Check the output format and scaling for the specific platform and utility version. This correspondence has not been confirmed for ATC 4.1.7 on Apex Encore / Raptor Lake / BIOS 2202: the examples are conditional.

$$tCK = 2000 / S \text{ ns} \cdot tQCLK = G \times tCK \cdot tRTL = R \times tQCLK$$

S is the effective data rate in MT/s: for DDR5-8200, use 8200, not 4100 MHz.

G is the Gear ratio (2 or 4), and R is the RTL value in QCLK.

Conditional example: 8200, Gear 2, RTL 65: $tCK = 2000/8200 \approx 0.244 \text{ ns}$; $tQCLK = 2 \times tCK \approx 0.488 \text{ ns}$; $tRTL = 65 \times tQCLK \approx 31.71 \text{ ns}$.

WHAT TO USE AS YOUR REFERENCE

The main reference is **repeatability on your own stable profile**. Under identical conditions, a higher RTL, a new spread between corresponding entries, and boot-to-boot jumps are warning signs, especially when accompanied by repeated POST attempts, test errors, or performance loss.

- 1. Create comparable conditions.** Save frequency, Gear, CAS, voltages, BIOS, and ME in a profile. Compare several full training cycles using the same boot method: a restart with MRC Fast Boot may reuse a saved result.
- 2. Record the result of each boot.** Compare the same active controller, subchannel, and rank positions. Note boot time and Karhu / y-cruncher errors; measure performance the same way each time.
- 3. Change one parameter.** If the result varies, test a lower frequency or looser CAS, then voltages separately. Repeat training and tests to verify reproducibility.

WHY THE RESULT MAY CHANGE

Factor	What to check
Frequency and CAS	High frequency and tight timings reduce stability margin. Returning to a validated profile helps distinguish the overclocking limit from a random training result.
Voltages	An unsuitable memory or controller voltage, including too much voltage, can reduce stability. RTL cannot identify the required power rail or direction of adjustment.
BIOS and boot	BIOS / ME version, Auto rules, and reuse of training results can change the comparison conditions. After changing BIOS, first establish a new baseline series of boots.

MANUALLY LOWERING RTL IN BIOS

For **EVGA DARK**, the community reported RTL reductions of 1-2, supposedly by lowering CAS: the RTL block would then train according to the selected CAS. **ASUS Z790** documents RTL Init / Max, a signed Offset, and rank fields. I tested these blocks and concluded that they should remain on Auto. The motherboard should perform the training itself. If the result is unusable, diagnose it (see the glossary). For **Z690 Tachyon**, there are reports that manual entry does not work and recommendations to enable RTL training; no conclusion has been established for Z790.

BEHAVIORAL VALIDATION IS WHAT MATTERS

Passing POST does not prove OS stability, and errors in the OS alone do not prove an RTL training failure. There is no universal "correct" RTL or permissible spread for all DDR5.

05 5.7 RTL/IOL TRAINING (CONTINUED)

anta777 EMPIRICAL FORMULA

anta777 has an empirical formula for estimating RTL. Effective DDR5 data rate in MT/s and CAS in cycles are entered into it, and the result is used as an approximate reference.

$$X = S / 800 + tCL + 19$$

8200 @ tCL38: 67.25 • 8200 @ tCL36: 65.25 • 8400 @ tCL38: 67.5

A technically exact universal relationship has not been confirmed. Do not force every utility entry to 65 / 66. The rule that "RTLA rounds down and RTLB rounds up" cannot be considered universal: when the fractional part is below 0.50, the lower integer RTLB value also occurs. In this case, this is an observation from readings, not proof of the BIOS rounding algorithm.

XTREEM CASE STUDY: 8200 AND 8400 MT/s

ASUS ROG Maximus Z790 Apex Encore, TEAMGROUP T-Force XTREEM 2 x 24 GB, Gear 2. We compare ATC readings for three profiles: 8200 @ tCL38, 8200 @ tCL36, and 8400 @ tCL38.

ATC entry	Controller and DDR5 path	8200 @ tCL38	8200 @ tCL36	8400 @ tCL38
MC0 C0 A1/A2	MC0, group A, subchannel C0	72/25	70/25	72/25
MC0 C1 A1/A2	MC0, group A, subchannel C1	67/25	65/25	67/25
MC1 C0 B1/B2	MC1, group B, subchannel C0	73/25	71/25	73/25
MC1 C1 B1/B2	MC1, group B, subchannel C1	67/25	65/25	67/25

How to read an entry. MC0 / MC1 are controller blocks; C0 / C1 are the two 32-bit DDR5 paths within each block. A1/A2 and B1/B2 label groups of positions in ATC. Apex Encore physically has two slots.

What 70/25 means. The slash separates two RTL readings in one entry. 70 applies to the occupied position; 25 in the second position matches Intel's reset value of 0x19. For this 1R kit, 25 is consistent with an unused position.

Relationship to the formula. At 8200, C1 matches the lower integer from the anta777 estimate: 67.25 -> 67 at tCL38, 65.25 -> 65 at tCL36. At 8400 @ tCL38, the estimate is 67.5, but C1 stays at 67; the entire RTL block matches 8200 @ tCL38. C0 is 5 / 6 above C1. The formula does not directly describe the whole block; the screenshots do not explain the offset or rounding algorithm.

The basic validation remains the same: several full training cycles, comparison with a stable profile, tests, and identical performance measurements. My 8200 @ tCL36 profile also showed RTL 64/65. One screenshot proves neither normal behavior nor an error. Under the confirmed conversion conditions in Section 5.7 (p. 49), at 8200 MT/s and Gear 2 one QCLK is approximately 0.488 ns: a difference of 5-6 conditionally corresponds to 2.44-2.93 ns. The ATC 4.1.7 scaling on this system has not been confirmed. This is a calculated read interval, not a measurement of overall latency or stability margin.

I treat Apex and other prominent 2-DIMM motherboards as the benchmark for correct, fast RTL training when comparing them with other boards, especially 4-DIMM models.

WHAT TO ACCOUNT FOR ON Z890

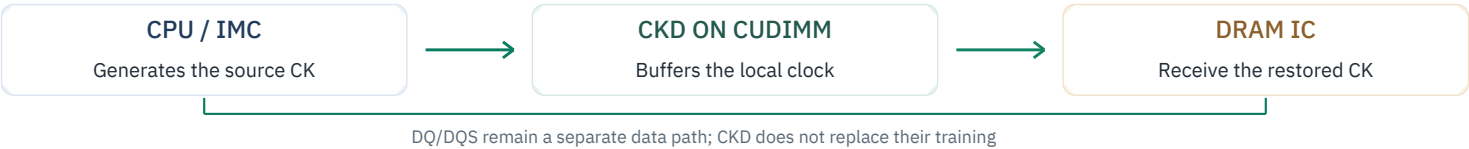
On Z890 / Core Ultra 200S, use documentation and a utility intended for that platform: field names, units, and training procedures may differ. ASUS BIOS includes **Training Consistency**, which may improve training repeatability but does not replace testing. Z790 numbers and offsets, including the anta777 estimate, cannot automatically be treated as targets for Z890.

05 5.8 Z890: CUDIMM, CKD, AND DIMM FIT

The public menu separates Read DQ/DQS ODT more precisely, exposes more PHY calibrations, and adds Training Consistency and the DIMM Fit family. The absence of an old name does not prove removal of the algorithm: it may have been merged, renamed, or hidden within the MRC.

Category	Examples	How to interpret the change
Retained	MCH Full Check; Training Profile; Mrc Training Loop Count; margin tools	The principle is unchanged; margin and the result depend on the new IMC/PHY and BIOS.
Renamed / split	MRC Fast Boot -> Fast Boot; Read ODT -> Read DQS ODT + Read DQ ODT	Compare by function, but do not treat every name as a direct 1:1 mapping.
Exposed for the first time	CA ODT Optimization; CTLE; RxVref Per-Bit; crosstalk; rank-to-rank; DCC	More observation points, not an obligation to switch each one manually.
Not visible as a separate entry	RTL, Max RTT_WR, Write Slew Rate, Read Amplifier, TxDqsTCO, Memory Test, and other Z790 entries	They are merely absent from the public Z890 manual; this does not prove removal from the MRC.

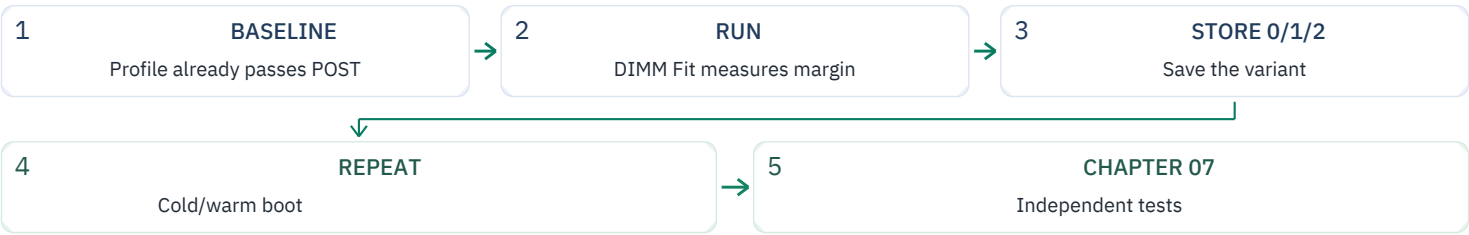
CUDIMM: CKD RESTORES THE CLOCK BUT DOES NOT TRAIN THE DATA PATH



CKD MODES AND AEMP III

The public ASUS Z890 BIOS manual lists no separate CKD Training entry. Single PLL, Dual PLL, and Bypass are modes of the CKD itself, not Gear 2/Gear 4 and not a replacement for the MRC. AEMP III is described as a two-stage process: first the clock driver, then memory frequency.

DIMM FIT: AUTOMATIC SEARCH FROM A GIVEN STARTING POINT



Function	What is available	Practical caveat
DIMM Fit	Store0 / Store1 / Store2 and deletion of the selected Store	Run it from a bootable baseline; the result is not yet a daily profile.
DIMM Fit Pro	Up to 20 parameters with ranges; Fail to Next advances to the next parameter early.	The transition criterion follows the BIOS User Guide. ASUS recommends 2 cycles; do not turn off power.
Training Consistency	Attempts to make training results more repeatable	Only when full retraining varies; start with Auto.

WHAT REMAINS VALID AFTER AUTOMATIC TUNING

DIMM Fit optimizes parameters only relative to the current starting point. After changing frequency, Gear, voltage, kit, or CKD mode, repeat training and tests for the saved Store. CKD improves clock-signal quality on CUDIMM, but does not prevent read/write data errors caused by unsuitable Vref/ODT settings or memory temperature. High Z890 frequencies cannot be explained by one CKD entry or attributed to Gear 4.

05 5.9 DDR5 RESISTANCES: ODT, RTT, AND RON

(FOR ADVANCED USERS. GENERALLY NEEDED FOR EXTREME OVERCLOCKING.
FOR ORDINARY TUNING, ALWAYS LEAVE THESE SETTINGS ON AUTO.)

ODT is line termination integrated into the die; RTT is its selected effective resistance; RON is the output resistance of the active transmitter. A lower number means stronger termination or output drive, but not automatically a better signal: excessive strength also creates ringing, overshoot, and crosstalk.

PRACTICAL TAKEAWAY

For ordinary DDR5 tuning, manual ODT/RON is not a mandatory step on either Apex platform considered here. Auto delegates the choice to the BIOS/MRC: firmware may account for factory tables and Power Training (DDR interface power-consumption training) results, but not every Auto value is a direct result of that stage. Auto can therefore be the correct final state. Even at 8400 MT/s, test Auto and readback values first. Manual resistances are needed mainly for extreme overclocking: extracting the last signal margin, raising maximum frequency, and locking in a repeatable benchmark result. 2R, 2DPC, a weak IMC, or unstable full training may require intervention sooner.

WHAT THE RESISTANCES ACTUALLY CONTROL

Parameter	When active	First A/B direction	What counts as improvement
RTT_WR	Target rank receives a write	DQ RTT WR: Auto/readback -> adjacent setting	A repeatable range of correct writes after several full training cycles
RTT_NOM_RD / WR	Non-target rank while reading/writing another rank	Change RD and WR one at a time; especially important for 2R/2DPC	Better rank-to-rank transitions without regression in the opposite direction
RTT_PARK / DQS	Rank is idle or parked	One PARK domain at a time	Repeatable cold/warm boot
DRAM RON	DRAM transmits data during a read	Pull-up/down: one adjacent setting after Auto	Improved read and training behavior, not a single successful POST
CA / CS / CK ODT	Commands, rank select, clock	GroupA/B only after a POST/training failure has been demonstrated	A series of cold-training cycles, not one successful boot

PRACTICAL POINTS FOR Z790 / Z890 APEX, STARTING AT 8400 MT/S

All resistances are in Ω. Historical examples do not replace Auto or validation on your own system.

Board / context	MT/s	Exact values / first step	What the source establishes
White Z790 Apex BIOS 1801 02/2024	8400–8600	Auto. Historical RON: PU/PD 40/34; 34/40. RTT and Groups: Auto.	Veii: a PCB-dependent comparison point [2]. Advice in a discussion, without a complete validated stable profile.
Z790 Apex Encore 02/2024 experiments	8533; 8600 target	RON: MC00 48/40; MC01 40/48 (PU/PD, source labels). No ready-made RTT preset.	Veii / tibcsi0407 [3, 4]: pairs and improvement after TX tuning are reported. This does not establish stable 8600–8800+.
Z890 Apex, UDIMM BIOS 3202; 285K; 2 × 16 GB A-die	8800 search → 8600 test	CHA RTT NOM RD 48 ; CHB RTT NOM RD 60 , NOM WR 40 , PARK DQS 120 .	UNIKO, DIMM Fit Pro [5]: four changed fields. Other actual resistances are not listed. ODT tuning alone did not pass the final validation stage.
Z890 Apex, CUDIMM	8800–9000+ target	Auto; supported DIMM Fit / Pro if needed. Record the result.	No transferable RTT/RON set was established in the reviewed sources. CKD does not replace DQ RTT; do not copy UDIMM CK ODT.

READING THE NUMBERS AND BIOS FIELDS

Auto is the basis for ordinary tuning, including Encore; 8400 MT/s does not require manual ODT. ASUS [1]: RTT 34/40/48/60/80/120/240 Ω; RON PU/PD 34/40/48 Ω. These are selectable values, not speed presets. Auto ≠ Disabled. Group A/B does not mean CHA/CHB; map RON pairs to the BIOS fields. Do not carry over old XOC sets without verified conditions. Max RTT_WR caps Power Training; it is not a direct DQ RTT WR input.

Z890: WHAT ODT TUNING ACHIEVED, AND WHAT CAME NEXT

In the UNIKO test [5] at 8600: new ODT alone → MT 100% and VT3 up to cycle 10 (~20 min); voltage fitting → error at cycle 16. Further tuning of MC Voltage Calculation Voltage Base to 1.16 V gave 30 cycles (~1 h). ODT alone did not produce that final result. Change one domain at a time and check full retraining and boots. DIMM Fit Completed Successfully also requires independent tests [6].

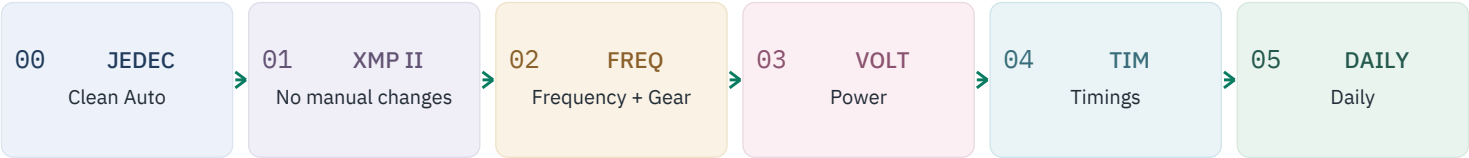
[1] ASUS Z890, 26–27 [2] HL #13403 [3] HL #13209 [4] HL #13315 [5] UNIKO, 30.06.2026 [6] ASUS DIMM Fit

05 5.10 PROFILES AND RECOVERY

Save a working step after each completed stage. Then a failed timing or voltage change will not force you to rebuild the profile: you can quickly return to the last repeatable point and test the next hypothesis separately.

Changing frequency or Gear requires retesting voltage ranges and training repeatability. When changing the CPU, kit, capacity, occupied slots, BIOS version, or UDIMM/CUDIMM type, it is safer to start from the baseline profile.

PROFILE LADDER: ROLLBACK SHOULD TAKE SECONDS



RECOVERY ORDER AFTER A FAILED POST

Step	Recovery	What to do	What is preserved
1	Wait	DDR5 training can take noticeable time; assess Q-Code and repeatability	Entire profile
2	ReTry	Retry POST with the same settings	Entire profile
3	Safe Boot	Safe boot: temporarily load conservative parameters and correct the OC	Manual fields
4	Working step	Load the previous profile	Validated baseline
5	Clear CMOS	Clear settings if BIOS is inaccessible; use FlashBack (BIOS recovery) only for a firmware problem	Previously exported copy

SAVE INTERMEDIATE PROFILES

Saved steps help isolate a change and roll back quickly. The criteria for a completed daily profile, cold/warm checks, and the test suite are covered in Chapter 7.9.

KEEP A COPY OUTSIDE CMOS

Export the profile to a USB drive and save screenshots of changed pages, the BIOS version, and a brief configuration description alongside it. A profile file may become incompatible after a firmware update, while the screenshots remain readable.

06 ADVANCED ANALYSIS OF TRAINING ALGORITHMS

6.1 COMMAND/ADDRESS PATH TUNING

This section covers Z790 Apex, Z790 Apex Encore, Z890 Apex, and other ASUS motherboards. Setting names were checked against the ASUS manuals, and the corresponding software values against Intel FSP.

The following settings provide a starting point and options to test when training causes problems. **AUTO does not always leave the setting ENABLED:** the BIOS decides, and an option appearing in the menu does not necessarily mean it is used for DDR5. **DISABLED does not lock in the previous training result:** other algorithms may change the same parameters.

These algorithms align the CMD/CTL command and control signals with the CLK clock signal, select command detection thresholds, and tune the electrical characteristics of the output drivers.

Early Command Training - ECT

What it does. Finds an initial working alignment of the command and control signals relative to CLK for the subsequent stages.

Practical choice. **AUTO.** Test ENABLED separately if full training fails with a new profile.

Key detail. The older implementation handles LPDDR. The specific CA/CS passes for DDR5 on Z790/Z890 have not been publicly confirmed.

Command Voltage Centering - CMDVC

What it does. Centers command Vref, the threshold for detecting commands.

Practical choice. **AUTO;** test ENABLED with automatic command Vref and inconsistent training results. DISABLED if centering repeatedly produces poor results or when manually tuning the same Vref.

Key detail. DDR5 has VrefCA and VrefCS; the exact scope of this BIOS stage has not been disclosed.

Early Command Voltage Centering

What it does. The name suggests early command Vref tuning; the exact implementation and how it differs from CMDVC have not been established.

Practical choice. **AUTO.**

Key detail. The option is listed for Z790; it is not listed in the Z890 manual reviewed.

Late Command Training - LCT

What it does. Performs late centering of CMD/CTL relative to CLK; the older code uses complex command patterns.

Practical choice. **AUTO;** ENABLED when selecting training stages manually while leaving command delays on automatic. Test DISABLED if this late adjustment reproducibly makes the result worse.

Key detail. Early and Late complement each other.

CMD CTL CLK Slew Rate - CMDSR

What it does. Tunes Slew Rate (the rate of voltage change at signal edges) for the command, control, and clock lines based on the operating window.

Practical choice. **AUTO** with automatic electrical settings. Test DISABLED when manually tuning the corresponding Slew Rate settings, or if the automatic stage reproducibly makes the result worse.

CMD/CTL DS & E 2D - CMDDSEQ

What it does. Jointly tunes command driver strength and transmitter equalization: Drive Strength × Tx Equalization.

Practical choice. **AUTO;** test DISABLED when manually tuning these parameters if the stage prevents the combination from being retained.

Key detail. Z890 lists separate CMD/CTL Drive Strength — CMDDS and CMD/CTL Tx Equalization — CMDTXEQ controls.

CMD/CTL Drive Strength Up/Dn 2D - CMDDRUD

What it does. Separately tunes the pull-up and pull-down strengths of the command drivers: pull-up × pull-down.

Practical choice. **AUTO;** test DISABLED when manually tuning the command Up/Dn settings specifically, or when automatic training repeatedly produces a poor result.

Key detail. The corresponding option/flag was not found in the Z890 manual reviewed or in the Arrow Lake-S interface.

6.2 INITIAL READ TRAINING

These stages calibrate the integrated memory controller (IMC) receivers, find an initial region of valid reads, and determine when to open the receive window. The BIOS retains the MPR name. In DDR5, training patterns are configured through dedicated MR registers: serial, clock, and LFSR (Linear Feedback Shift Register) patterns are provided.

SenseAmp Offset Training - SOT

What it does. Calibrates the inherent electrical offset of the CPU's DQ/DQS input receivers, compensating for variation in their detection thresholds.

Practical choice. **AUTO**. At the overclocking limit, if results differ between training runs, test DISABLED separately; keep it only if boot behavior and test results improve repeatably.

Early ReadMPR Timing Centering 2D - ERDMPRTC2D

What it does. Searches for an initial read region across DQ/DQS timing and RxVref. The older algorithm centers timing at different RxVref values using a known pattern, without requiring functional writes to normal memory.

Practical choice. **AUTO**. Test ENABLED separately if full training fails or produces inconsistent results.

Key detail. Early Read Time Centering 2D uses normal test traffic.

Read MPR Training - RDMPT

What it does. Aligns DQ reads relative to DQS using a known pattern: finds the timing boundaries of the operating window and selects a position within it.

Practical choice. **AUTO**; ENABLED when manually enabling the basic training stages.

Receive Enable Training - RCVET

What it does. Locates the arrival of the DQS preamble and sets when the receive window opens — DQS gating.

Practical choice. **AUTO**; ENABLED when manually enabling the basic training stages. Disable it only to diagnose a specific, reproducible failure.

Receive Enable Centering 1D - RCVENC1D

What it does. Further centers Receive Enable along the timing axis.

Practical choice. On Z790 Apex / Encore — **AUTO**.

Key detail. The older Coffee Lake description includes LPDDR Only. The option/flag was not found in the Z890 manual or the Arrow Lake-S IoT FSP reviewed.

HOW TO COMPARE THE SETTINGS

I start with AUTO wherever it is available. For the comparison, I disable MRC Fast Boot (Fast Boot within the memory settings on Z890). I change one switch at a time, perform several cold boots with full training, and check the frequency, full memory capacity, and stability after different training runs.

6.3 WRITE TRAINING

These algorithms align the write strobe DQS with the CK clock signal, then center the data relative to DQS and tune the VrefDQ threshold on the DRAM side.

Jedec Write Leveling - JWRL

What it does. Aligns DQS relative to CK on the memory side, compensating for the difference in their delays. The controller uses feedback from DRAM to position the write strobe.

Practical choice. **AUTO**; ENABLED when controlling the basic training stages manually.

Key detail. DDR5 also provides compensation for mismatched internal DQ/DQS paths.

Early Write Time Centering 2D - EWRTC2D

What it does. Performs a preliminary search for a working write region: centers DQ/DQS timing at several DRAM VrefDQ values and selects a suitable starting point.

Practical choice. **AUTO**. Test ENABLED or DISABLED separately when troubleshooting full training.

Key detail. In the older MRC code reviewed, this stage is allowed only for DDR4. The field in current FSP does not disclose the conditions under which it runs for DDR5. The Z790 manual uses Timing instead of Time in the name.

Write Timing Centering 1D - WRTC1D

What it does. Finds the write window and centers DQ timing relative to DQS at the current VrefDQ.

Practical choice. **AUTO** where available; in menus with only ENABLED / DISABLED, start with ENABLED. Keep the selected basic centering mode when enabling the late 2D pass.

Key detail. E21287 and E22758 for Z790 offer only ENABLED / DISABLED; E25061 for Z890 also offers AUTO.

Write Voltage Centering 1D - WRVC1D

What it does. Centers VrefDQ, the internal threshold for detecting write data in DRAM, at the current DQ/DQS timing position.

Practical choice. **AUTO**; ENABLED when manually enabling the basic training stages. Test DISABLED if centering repeatedly produces poor results or when manually tuning this same DRAM VrefDQ.

Key detail. Even with manual VDD/VDDQ settings, the DRAM VrefDQ threshold is tuned separately.

Write Timing Centering 2D - WRTC2D

What it does. Refines the DQ/DQS timing position, accounting for changes in the operating window at different VrefDQ values.

Practical choice. **AUTO**. At a borderline overclock, test ENABLED separately if stability varies after repeated training. Keep DISABLED only if it produces a repeatable improvement over the initial mode.

Key detail. The reference stage may include per-bit deskew: individual compensation for timing variation between bits.

Write Voltage Centering 2D - WRVC2D

What it does. Measures the voltage boundaries of the operating window at several DQ/DQS timing offsets and uses the combined results to refine VrefDQ.

Practical choice. **AUTO**. Test ENABLED separately if stability after training is borderline. DISABLED if centering is demonstrably poor or when manually tuning the same VrefDQ.

Z890: Unmatched Write Time Centering 1D is a separate option with the UNMATCHEDWRTC1D flag; see §6.12.

6.4 READ TRAINING

These algorithms tune the DQ sampling time relative to DQS and the RxVref threshold in the memory controller's receive path. Unlike write training, they tune the CPU side.

Early Read Time Centering 2D - ERDTC2D

What it does. Performs a preliminary search for a read operating point across DQ/DQS timing and RxVref; the reference code checks it using normal test traffic.

Practical choice. **AUTO**. Compare ENABLED / DISABLED separately when troubleshooting full training.

Key detail. In the older MRC code reviewed, ERDTC2D is restricted to DDR4; the conditions used by the current DDR5 implementation have not been disclosed. The Z790 manual spells the name Early Read Timing Centering 2D.

Read Timing Centering 1D - RDTC1D

What it does. Finds the timing boundaries for receiving data and centers the DQ sampling time relative to DQS on the controller side at the current RxVref.

Practical choice. **AUTO**; ENABLED when controlling the basic training stages manually. When enabling RDTC2D, keep the selected RDTC1D mode: basic and subsequent centering may run one after the other.

Read Timing Centering with JR

What it does. A separate read timing centering variant in the Z790 menu. How it differs from RDTC1D has not been established.

Practical choice. **AUTO**.

Key detail. The meaning of JR has not been confirmed. This option is not listed in the Z890 manual reviewed.

Read Voltage Centering 1D - RDVC1D

What it does. Centers RxVref, the memory controller's data detection threshold, at the current DQ/DQS timing position.

Practical choice. **AUTO**; ENABLED with automatic RxVref when controlling the basic training stages manually. Test DISABLED for poor results or manual RxVref tuning, provided a comparison confirms that this pass is interfering.

Key detail. Even with manual VDDQ or SA settings, the RxVref threshold is tuned separately.

Read Timing Centering 2D - RDTC2D

What it does. Refines the data sampling time based on the shape of the operating window at different RxVref values.

Practical choice. **AUTO**. At a borderline overclock, test ENABLED separately if stability varies after repeated training. Keep DISABLED only if it produces a repeatable improvement.

Key detail. The reference stage may perform per-bit deskew: individual compensation for timing variation between bits.

Read Voltage Centering 2D - RDVC2D

What it does. Refines RxVref using the voltage boundaries of the operating window, measured at several DQ/DQS timing offsets.

Practical choice. **AUTO**. Test ENABLED separately with inconsistent training results and automatic RxVref. DISABLED if centering is confirmed to be poor or when manually tuning the same threshold.

Z890: RxVref Per-Bit Training is a separate option with the RXVREFPERBIT flag; see §6.12.

6.5 ODT, RON, AND TRANSMITTER DRIVE STRENGTH

ODT provides termination for impedance matching; RON and Drive Strength set transmitter output resistance and drive strength. Slew Rate (the rate of voltage change at signal edges) and equalization change the signal shape.

Dimm ODT Training - DIMMODTT

What it does. Tunes DRAM termination based on read and write margins. The full set of DDR5 RTT settings searched by a particular BIOS has not been disclosed. DISABLED skips this tuning stage; termination itself continues to operate.

Practical choice. **AUTO** with automatic RTT settings. Test ENABLED if training results are inconsistent; DISABLED if the stage overrides manually tuned RTT settings or makes the result worse.

Max RTT_WR

What it does. Sets the upper limit for automatic RTT_WR tuning in power training. Options: ODT OFF and 120 Ohms. The final RTT_WR is selected during training within this limit.

Practical choice. **BIOS DEFAULT VALUE**. Test 120 Ω separately. ODT OFF sets the RTT_WR search limit here; DIMM termination as a whole remains active.

DIMM RON Training - DIMMRONT

What it does. Tunes the DRAM driver's output resistance during reads: memory → CPU. RON applies to the transmitter, RTT to termination.

Practical choice. **AUTO**. Test DISABLED with manual DRAM Output Driver Impedance if training interferes with it. If only RTT or CPU Write Drive Strength is being changed, the DIMM RON Training mode can remain as it was.

Read ODT Training - RDODTT

What it does. Tunes the CPU receiver's termination during reads. DIMM RTT_NOM_RD sets termination on the memory side and is tuned separately. On Z890, CPU receiver termination training is split into Read DQ ODT Training and Read DQS ODT Training.

Practical choice. **AUTO**. Test DISABLED for manually tuned CPU Read ODT if the stage changes the result, or if automatic tuning repeatedly produces poor results. On Z890, compare DQ and DQS separately.

DIMM CA ODT Training - DIMMODTCA

What it does. Tunes command/address line termination on the DRAM side. The older code handles LPDDR4; the scope for DDR5 CA/CS/CK has not been disclosed. CA ODT Optimization is listed separately on Z890.

Practical choice. **AUTO**. Test DISABLED with manual CA ODT if this stage interferes with it.

Write Drive Strength/Equalization 2D - WRDSEQT

What it does. Jointly tunes CPU driver strength and write equalization: CPU → DRAM. The two dimensions are Drive Strength × Tx Equalization.

Practical choice. **AUTO**; test ENABLED if training results are inconsistent. DISABLED when manually tuning these parameters if the stage interferes with them. Write Drive Strength and Write Equalization are listed separately on Z890.

Write Slew Rate Training - WRSRT

What it does. Tunes the slew rate of CPU write signals.

Practical choice. **AUTO**. Test DISABLED with manual Write Slew Rate or if the pass makes the result worse.

Write Driver Strength Training - WRDS

What it does. Trains CPU write driver strength separately. The order and interaction of WRDS and WRDSEQT in the BIOS have not been disclosed.

Practical choice. **AUTO.** Test DISABLED if training overrides manual CPU Write Drive Strength. On Z890, the field with the corresponding name is Write Drive Strength.

Write Drive Strength Up/Dn independently - WRDSUDT

What it does. Separately tunes the pull-up and pull-down sides of the CPU write driver. DIMM Pull-up / Pull-down Output Driver Impedance applies to the driver on the memory module.

Practical choice. **AUTO.** Test DISABLED with manual CPU Drive Up/Dn settings or if training produces a poor result.

Max RTT_WR, Write Slew Rate Training, and Write Drive Strength Up/Dn independently are not listed in the Z890 manual reviewed.

6.6 RECEIVER EQUALIZATION

These algorithms tune the CPU receiver when reading from DRAM. The equalizer compensates for distortion in the incoming signal; amplifier training selects the operating mode of the analog circuitry.

Read Equalization Training - RDEQT

What it does. Tunes the CPU receiver's equalizer based on read timing and voltage margins. In the older MRC, the available settings depend on the receiver mode; the code includes CTLE and DFE.

Practical choice. **AUTO.** At a borderline overclock, test ENABLED separately if results differ between training runs. DISABLED if automatic tuning produces a poor result or when manually tuning the corresponding equalization.

Key detail. On Z890, Read CTLE Training is listed separately from Read Equalization Training.

Read Amplifier Training - RDAPT

What it does. In the older code, tunes the bias current or load of the CPU receiver's analog circuitry, depending on the mode. It considers read margin and, in the relevant mode, power consumption.

Practical choice. **AUTO.** At the overclocking limit, test DISABLED separately if there are repeatable signs of poor receiver-mode tuning. ENABLED allows tuning of the already active amplifier's operating mode. The amplifier's operating parameters are determined by the tuning result.

Key detail. This option is not listed in the Z890 manual reviewed.

6.7 PHY COMPENSATION AND CALIBRATION

These algorithms tune compensation codes, internal transmitter delays, power supplies, and reference circuits in the CPU memory PHY.

Comp Optimization Training

What it does. In the older MRC, moves the shared portion of byte-group corrections into global compensation, reducing local offsets while aiming to preserve the overall result. Handles Write Drive Strength, Read ODT, and, in some branches, Slew Rate.

Practical choice. **AUTO.** Test DISABLED if this stage causes problems or when investigating manual compensation offsets. This stage can remain enabled with manual RTT or Drive Strength settings. Hardware compensation also works when training is disabled.

Key detail. Z890 lists Comp Optimization and Pre Training Comp Calibration separately.

TxDqTCO Comp Training - TXTCO

What it does. Tunes delay compensation for the DQ output path during writes: CPU → DRAM. The older MRC evaluates the write window.

Practical choice. **AUTO;** test ENABLED separately when training results are inconsistent, and DISABLED when this stage reproducibly makes them worse.

ClkTCO Comp Training - CLKTCO

What it does. Tunes delay compensation for the CLK output path. The older code evaluates the command window and also updates the CMD/CTL TCO codes; the exact scope of the current stage has not been disclosed.

Practical choice. **AUTO.** ENABLED can be tested when training is marginal.

TxDqsTCO Comp Training - TXTCODQS

What it does. Tunes delay compensation for the CPU-side write DQS output strobe.

Practical choice. **AUTO**, if available. Test DISABLED only when this stage causes a specific deterioration. No separate entry is listed in the Z890 manual reviewed.

VccDLL Bypass Training - VCCDLLBP

What it does. ENABLED allows testing the VccDLL power-supply bypass mode from VccIOG. Whether Bypass is entered depends on the test result; the DLL continues to operate.

Practical choice. **AUTO**. DISABLED is a diagnostic option if this stage causes problems. The setting is not listed in the Z890 manual reviewed.

PanicVttDnLp Training - PVTTDNLP

What it does. In the older MRC, tunes VttPanicCompDnLPMult for the pull-down branch of fast VTT correction, only for LPDDR with VTT termination.

Practical choice. **AUTO**. The setting is not listed in the Z890 manual reviewed.

Read Vref Decap Training - RDVREFDC

What it does. Tunes the programmable RxVref decoupling capacitances in the CPU receiver. The older code then provides for RxVref recentring.

Practical choice. **AUTO**; test ENABLED when read training results are inconsistent, and DISABLED when this pass makes them worse.

Vddq Training - VDDQT

What it does. The older, partly unfinished MRC describes tuning CPU TX VDDQ through FIVR based on command and write margins, only for LPDDR4/5. The role of this stage in controlling DRAM VDDQ through the PMIC remains unknown.

Practical choice. **AUTO**. With manual CPU TX VDDQ, test DISABLED separately if you suspect interference from this pass. If only DRAM VDDQ is set manually, you can retain the initial mode for this stage. My example in §5.5 applies only to the specified configuration.

6.8 DUTY CYCLE CORRECTION — DCC

Duty cycle is the fraction of a period for which a signal is high. DCC equalizes the high and low durations, usually toward 50/50.

Duty Cycle Correction Training - DCC

What it does. Calibrates the correction of high and low durations in the CPU memory interface.

Practical choice. **AUTO**. When explicitly controlling training stages, start with ENABLED; test DISABLED if a training problem is reproducible.

Key detail. The exact scope of the general Apex switch has not been disclosed. Z890 separately lists Downstream, QCLK Calibration, Rise/Fall, and Functional DCC for DDR5 DQS, DDR5 CLK, and Data DQ.

Periodic DCC

What it does. Allows periodic updates to duty cycle correction after the initial calibration. The interval and conditions for running it on DDR5 Apex have not been published.

Practical choice. **AUTO**. When selecting a mode explicitly, use DISABLED as the baseline for comparison; test ENABLED separately, including extended operation and transitions between idle and load.

Key detail. The setting appears in the Z790 E22758 manual; it is not listed in the earlier E21287 or in the Z890 E25061 manual.

Tx Dqs Dcc Training - TXDQSDCC

What it does. Tunes duty cycle correction for the CPU-side write DQS output strobe, for transfers from CPU → DRAM.

Practical choice. **AUTO**; when selecting a mode explicitly, start with ENABLED. Test DISABLED if this stage reproducibly makes the result worse.

Key detail. No separate entry is listed in E25061; a connection to Functional DCC for DDR5 DQS has not been confirmed.

6.9 RTL AND TRANSITIONS BETWEEN OPERATIONS

RTL determines when read data returns to the controller; TAT sets the intervals between bus operations.

Round Trip Latency - RTL

What it does. Optimizes the latency of data returning after a read command. In the older Ice Lake MRC, RTL is tuned together with receive FIFO delays, with read-window checks and a margin.

Practical choice. **ENABLED.** I always leave this stage enabled when tuning memory manually.

Key detail. Initial RTL values are already calculated during Receive Enable Training; a separate pass optimizes them. RTL is not listed in E25061. It is unknown whether the Read/Write Rank-to-Rank Training settings replace RTL.

Turn Around Timing Training - TAT

What it does. Tunes the intervals for read → read, read → write, write → read, and write → write, including rank changes. The older MRC optimizes the corresponding variants of tRDRD, tRDWR, tWRRD, and tWRWR, as well as CPU receiver ODT turn-on timing and duration.

Practical choice. **DISABLED.** I tune memory and tertiary timings manually, so I disable automatic tuning.

Key detail. The older MRC also tunes ODT with a single rank. TAT is retained on Z890.

6.10 DDR5 SIGNALING

DFE tunes data reception inside DRAM during writes; DCA adjusts the output waveforms during reads.

DIMM DFE Training - DIMMDFE

What it does. Trains Decision Feedback Equalization in the DRAM receiver during writes: CPU → memory. DFE accounts for previous bits and compensates for their effect on detecting the current bit.

Practical choice. **AUTO.** When explicitly controlling training stages, start with ENABLED; test DISABLED if training reproducibly produces poor results or when tuning DIMM DFE manually.

Key detail. Hardware DFE may also operate when training is disabled.

EARLY DIMM DFE Training - EARLYDIMMDFE

What it does. A separate early pass for tuning DRAM DFE. The exact search sequence and interaction with the main DIMM DFE stage in Apex BIOS have not been disclosed. It is unknown whether one pass can replace the other.

Practical choice. **AUTO.** Compare ENABLED and DISABLED separately for a specific training problem.

DRAM EMPHASIS Training - DRAMEMPHASIS

What it does. The purpose of this switch for DDR5 in Apex BIOS has not been disclosed.

Practical choice. **AUTO.**

DRAM DCA Training - DRAMDCA

What it does. Trains the Duty Cycle Adjuster inside DRAM: adjusts the high and low durations of the DQ/DQS outputs during reads, memory → CPU. The goal is to reduce duty cycle distortion, bringing the durations closer to 50/50.

Practical choice. **AUTO.** When explicitly controlling training stages, start with ENABLED; test DISABLED if training reproducibly gets worse.

DQS OFFSET ADJUST Training - DQSOFFSETADJUST

What it does. The implementation of this pass in Apex BIOS has not been disclosed. DDR5 provides Read DQS Offset Timing through MR40: the DQS strobe starts transmitting earlier relative to DQ. A connection between this switch and MR40 has not been confirmed.

Practical choice. **AUTO.** Compare ENABLED/DISABLED separately for a specific training problem.

Key detail. According to the DRAM documentation, changing MR40 leaves data transmission timing and Read Latency unchanged.

Z890: E25061 lists DIMM DFE Training separately; the other four settings in this block are not listed. Duty Cycle Correction for LP5 DCA is intended for LPDDR5. There is no confirmation that it can replace DRAM DCA when tuning DDR5.

6.11 SIGNAL MARGINS, CHECKS, AND REPAIR

Margin is the distance from the operating point to the error boundary in timing or Vref. These settings control measurements, training and addressing checks, retraining, and DRAM repair. Validate the profile under load separately.

Rank Margin Tool Per Bit - RMTBIT

What it does. Measures timing and receiver-threshold margins for individual DQ bits. In the older MRC, a separate flag starts it without checking the RMT flag; the dependency in current ASUS BIOS implementations has not been disclosed.

Practical choice. **AUTO** or DISABLED if the results are not used; ENABLED for diagnostics when the data is accessible.

Rank Margin Tool - RMT

What it does. Evaluates timing and Vref margins for reads, writes, and commands. Allows comparison of trained states.

Practical choice. **AUTO** or DISABLED for normal operation; ENABLED if you have a way to read the results. BDAT export is enabled separately. The report may still be unavailable in the BIOS interface.

Memory Test - MEMTST

What it does. Tests memory during initialization; ASUS has not disclosed the coverage or patterns.

Practical choice. **AUTO**; ENABLED for boot diagnostics. No separate entry is listed in E25061 for Z890.

DIMM SPD Alias Test - ALIASCHK

What it does. Intended to detect DRAM address aliasing when the module organization is described incorrectly. The older code checks geometry and capacity against SPD; the physical address test is unfinished.

Practical choice. **AUTO** or ENABLED. DISABLED makes sense only for a confirmed false positive.

Post Package Repair Training - PPR

What it does. Allows defective DRAM rows to be replaced with spare rows: Soft PPR is a temporary repair; Hard PPR is permanent and survives power loss.

Practical choice. Do not force it on for normal overclocking; when controlling it manually, start with **DISABLED**. Do not move to Hard PPR because of errors that occur only when overclocked.

Key detail. The repair type and trigger conditions may be set separately. The repair type used by ASUS has not been established; the Z890 menu name omits Training.

Retrain Margin Check - RMC

What it does. In the older MRC, checks read, write, and command margins; if margin is insufficient, raises the optimization thresholds and requests retraining during the current initialization. Execution also depends on the power training mode.

Practical choice. **AUTO**. ENABLED for investigating inconsistent training results; DISABLED if the check itself causes a problem.

Margin Check Limit

What it does. Selects the margin check used to decide whether to retrain on the next boot: DISABLED, L1, L2, BOTH.

Practical choice. **DEFAULT VALUE**. For diagnostics, start with L1; test L2 and BOTH with the L2 scaling in mind.

Margin Limit Check L2

What it does. Sets the threshold: $L2 = L1 \times \text{value} / 100$. Available when L2 or BOTH is selected.

Practical choice. **DEFAULT VALUE**; use 100 for comparison.

Key detail. A higher value sets a stricter check threshold. A range of 1–300 is specified for Z790; the Z890 manual does not give the limits.

6.12 ADDITIONAL Z890 APEX ALGORITHMS

The Z890 menu adds training stages and separate controls for some existing functions. This section covers the differences from Z790 documented in the ASUS Apex manuals. Start with AUTO; the procedure for comparing settings is in §6.2.

CA ODT Optimization

What it does. Separate optimization of command/address line termination. DIMM CA ODT Training is also retained in the menu; ASUS does not describe how the tasks are divided between these two stages.

Practical choice. **AUTO**. When tuning manually, change these two settings separately.

Unmatched Write Time Centering 1D - UNMATCHEDWRTC1D

What it does. A separate one-dimensional write alignment stage for the Unmatched path. The public Intel interface does not disclose how it differs from regular Write Timing Centering 1D.

Practical choice. **AUTO.**

RxVref Per-Bit Training - RXVREFPERBIT

What it does. Tunes the input detection threshold separately for each data bit on the CPU receiver side.

Practical choice. **AUTO.**

DDR5 ODT Timing Config - DDR5ODTTIMING

What it does. A separate stage for tuning DDR5 ODT timing: when termination turns on and off relative to data transfers.

Practical choice. **AUTO.** Compare ENABLED and DISABLED separately for a reproducible problem during full training.

Read CTLE Training - RDCTLET

What it does. Tunes the CPU receiver linear equalizer. CTLE adjusts the frequency response of the input path, reducing signal distortion during reads.

Practical choice. **AUTO.**

Ddr5 Rx Cross-Talk Cancellation - DDR5XTALK

What it does. Controls crosstalk compensation in the DDR5 receive path: adjacent lines can induce interference in the received signal.

Practical choice. **AUTO.**

Unmatched Rx Calibration - RXUNMATCHEDCAL

What it does. Calibrates the Unmatched receive path. Its architecture and adjustable quantities have not been disclosed in the ASUS manuals or the public FSP interface.

Practical choice. **AUTO.**

DQ/DQS Swizzle Training - DQDQSSWZ

What it does. Configures the mapping of logical DQ/DQS lines to their physical routing, accounting for line swaps.

Practical choice. **AUTO.**

Write DQ/DQS Retrain - WRTRETRAIN

What it does. Controls a separate stage that retunes the relative alignment of DQ and DQS during writes. The older MRC describes such a mechanism for LPDDR; its DDR5 implementation on Z890 has not been disclosed.

Practical choice. **AUTO.**

These stages calibrate internal memory-PHY circuitry: compensation, phase interpolators, receivers, and linear voltage regulators.

Pre Training Comp Calibration - DDRPRECOMP

What it does. Performs preliminary compensation calibration before the main training stages. Z890 separates it from the subsequent Comp Optimization stage.

Practical choice. **AUTO.**

Ref PI Calibration - REFPI

What it does. Calibrates the phase interpolator reference circuitry. PI positions the edge where required between the available clock phases.

Practical choice. **AUTO.**

Data PI Linearity Calibration - DATAPILIN

What it does. Calibrates the linearity of the data-path phase interpolators: equal control-code steps should produce uniform phase shifts.

Practical choice. **AUTO.**

Rx SAL Calibration - RXSALCAL

What it does. A separate receiver calibration. The purpose of the SAL circuitry and the adjustable quantities are not described in the ASUS manuals or public FSP.

Practical choice. **AUTO.**

VccClk FF Offset Correction - VCCCLKFF

What it does. Corrects the offset of the internal VccClk FF circuitry. What FF stands for and its relationship to a specific BIOS voltage field have not been established from the sources reviewed.

Practical choice. **AUTO.**

LVR Auto Trim - LVRAUTOTRIM

What it does. Automatically trims the internal PHY linear voltage regulators. In the Meteor Lake/Arrow Lake architecture, LVRs supply internal CPU memory-interface circuitry.

Practical choice. **AUTO.**

View Pin Calibration - VIEWPINCAL

What it does. An internal calibration for View Pin. Public manuals do not explain the purpose of this circuitry or its relationship to DDR5 tuning.

Practical choice. **AUTO.**

Power Saving Meter Update - PWRMETER

What it does. Updates an internal estimate of energy savings. In the older MRC, the calculation compares the states before and after optimization and passes the result to the power controller.

Practical choice. **AUTO.**

On Z890, DCC is split by circuit and signal. Separate settings handle read and write training across different ranks and protection against Rowhammer.

Duty Cycle Correction Downstream Training - DCCDOWNSTREAM

What it does. Corrects duty cycle in downstream clock-path circuitry. Intel specifies the PI Serializer/LUT area—the phase interpolator serializer and its settings table.

Practical choice. **AUTO.**

Duty Cycle Correction QCLK Calibration - DCCQCLK

What it does. Calibrates the duty cycle of the internal QCLK signal.

Practical choice. **AUTO.**

Duty Cycle Correction Rise/Fall Training - DCCRISEFALL

What it does. Performs separate rising- and falling-edge correction, equalizing the signal high and low durations.

Practical choice. **AUTO.**

Functional Duty Cycle Correction for DDR5 DQS - FUNCDCCDQS

What it does. Performs functional duty cycle correction for the DDR5 DQS strobe. A connection to the earlier Tx Dqs Dcc Training has not been confirmed.

Practical choice. **AUTO.**

Functional Duty Cycle Correction for DDR5 CLK - FUNCDCCLK

What it does. Performs functional duty cycle correction for the DDR5 CLK signal.

Practical choice. **AUTO.**

Functional Duty Cycle Correction for Data DQ - FUNCDCDQ

What it does. Performs functional duty cycle correction for the DQ data lines.

Practical choice. **AUTO.**

Write Rank-to-Rank Training - TXRK2RK

What it does. Separate write training for operation across different ranks. The delays it tunes are not listed in public FSP; Turn Around Timing Training is retained as a separate setting.

Practical choice. **AUTO.**

Read Rank-to-Rank Training - RXRK2RK

What it does. Separate read training for operation across different ranks. The delays it tunes are not listed in public FSP.

Practical choice. **AUTO**. Do not carry over the Z790 RTL recommendations to this setting; a connection between the stages has not been confirmed.

Row Hammering Prevention - ROWHAMMER

What it does. Controls protection against errors in adjacent DRAM rows caused by repeatedly activating the same rows. This is a separate entry in the Z890 training menu; the protection itself also existed on earlier platforms.

Practical choice. **AUTO**. I do not recommend disabling it for overclocking; it affects data protection. The specific mechanism selected by ASUS has not been disclosed.

FOR EVERYDAY MEMORY TUNING

The purpose of this chapter is to explain how the TRAINING ALGORITHMS controls work. For the average user, the practical rule is simple: leave 98% of these settings on **AUTO**. Changing them makes sense when you have a specific training problem and understand what you are testing.

07 7.1 WHAT EXACTLY NEEDS TO BE PROVEN

Use different workloads to check a DDR5 profile. Data storage and transfer, the memory controller, heavy computational workloads, training repeatability, and margin at real operating temperatures must be tested separately.

FIVE DIFFERENT TEST TARGETS

Target	What may be unstable	How we test it	What a single test does not prove
DRAM and data	Cells, rows, refresh, writes, and reads	Karhu, TM5, MemTest86, OCCT Memory	IMC stability under AVX load
IMC / PHY	CPU-to-DIMM link, VDD2/MC, TX, SA, Vref, and signal integrity	y-cruncher VT3/FFTv4, OCCT CPU + RAM	Absence of a rare retention error
CPU and cache	Cores, ring/cache, voltage, and CPU temperature	y-cruncher SVT and small in-cache tests	Stability of the modules alone
Training	Variation in trained values, cold/warm boot, and the saved fast path	Several complete training cycles and boots	Stability of an already-booted system
Temperature	tREFI, tRFC, DRAM voltage, and different thermal behavior of 1R/2R	Karhu/TM5 with HWiNFO and real airflow	Behavior of a cold memory kit

ANY CONFIRMED ERROR MEANS INSTABILITY

There is no acceptable number of errors. However, where an error appears does not by itself identify the culprit: Karhu can catch a CPU/cache issue, y-cruncher can catch memory or IMC instability, and MemTest86 can catch a firmware-dependent error. First reproduce the symptom, then change one parameter.

PROFILE TESTING SEQUENCE

Step	Stage	Practical action	Proceed when
1	Quick screening	10–30 minutes of a targeted workload after one change	No errors or hangs
2	Isolate the cause	Compare SVT with VT3/FFTv4 and an independent RAM test	The conditions that reproduce the failure are understood
3	Pre-boot	MemTest86: four passes after cold training	No address or bit errors
4	Thermal conditions	Bring the DIMMs to their daily-use temperature plateau	The profile holds its operating tREFI
5	Repeatability	Cold boot, warm restart, sleep, and normal workloads	The result does not depend on one lucky POST

THE CORE PRINCIPLE OF THIS CHAPTER

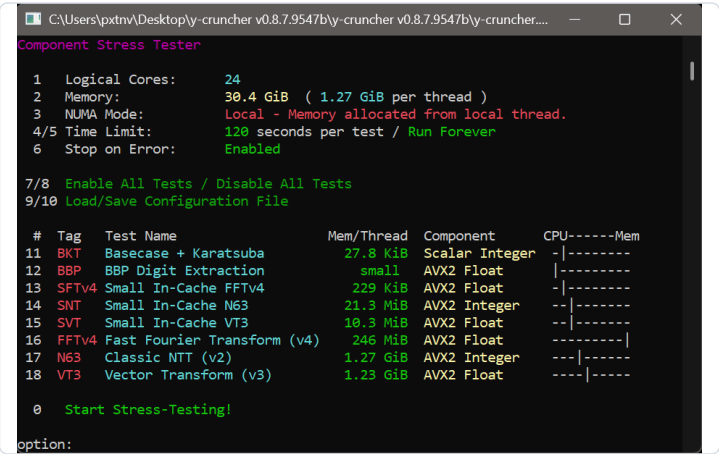
A combination of two or three different algorithms provides more information than running one test all day. For a final profile, we use y-cruncher, Karhu, MemTest86, and RAM Test Pro by Svetlana; for testing quality, I would even rank it first. Boot checks remain mandatory; I treat TM5 as an alternative targeted tool.

Test duration

Running one test on the principle that “longer is better” is a foolish waste of time. A profile needs a mix of checks: memory, the controller, heat, retraining, and boots. Even relatively short checks in combination can reveal more than blindly looping one algorithm. Every test needs a purpose. Without one, you are just wasting your time running hours of tests for the sake of testing. Ignore that advice — the people giving it have a very superficial understanding of the hardware.

07 7.2 y-cruncher: COMPONENT WORKLOADS

Use only Component Stress Tester. The official Windows build is v0.8.7.9547b; Linux is v0.8.7.9547. My screenshot shows the Windows binary 0.8.7.9547b.



PRACTICAL STARTING POINT

Memory: for large tests, 80–90% of free RAM with room for the OS, without paging. NUMA: Local on a typical LGA1700/LGA1851 system. Time Limit: 60–120 s per component, not per session. Stop on Error: Enabled.

The instruction set depends on the binary. AVX2 in the screenshot describes that run. Record the version, binary, threads, and memory allocation when comparing results. Mem/Thread shows memory use per thread, which varies by component.

WHAT EACH COMPONENT DOES

Tag	Algorithm	Primary workload	Role in DDR5 diagnostics
BKT	Basecase + Karatsuba*	Scalar integer multiplication; small working set	CPU arithmetic; little dependence on RAM
BBP	BBP Digit Extraction	Vector floating-point arithmetic; small working set	CPU compute workload; does not test the full RAM allocation
SFTv4	Small In-Cache FFTv4	Small FFTv4: floating-point Fourier transform in cache	CPU/cache; complements large FFTv4
SNT	Small In-Cache N63	Small N63: integer NTT in cache	CPU/cache with a different type of arithmetic
SVT	Small In-Cache VT3	Small VT3: vector computation with an in-cache working set	CPU/cache; I compare it with large VT3
FFTv4	Fast Fourier Transform v4	Floating-point FFT; large working set, strongly dependent on RAM bandwidth	CPU/cache/IMC/RAM with heavy memory traffic
N63	Classic 64-bit NTT v2	64-bit integer NTT; large working set	Another algorithm for combined CPU and RAM testing
VT3	Vector-Scalable Transform v3	Vector transform; large working set, CPU + IMC + RAM	Mixed workload across the DDR5 path; successor to VST

* Command Lines.txt expands BKT to include Toom-Cook; the developer’s internals guide says Toom-3 was removed.

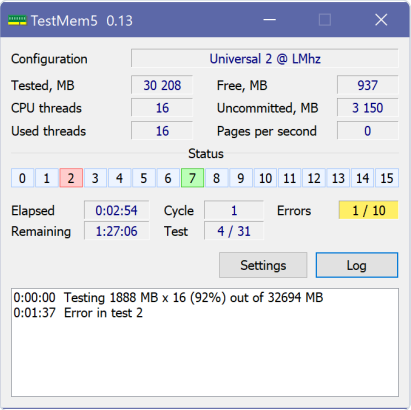
HOW I COMPARE THE RESULTS

SVT is the small, in-cache variant of VT3; VT3 succeeds the old VST. If SVT passes but VT3 fails, I check the profile with a large working set: CPU/cache, IMC, and RAM. If both fail, I start with the same components. I revert the last change, repeat the check, and add an independent RAM test. FFTv4 exercises the CPU and memory together.

TYPICAL PRACTICAL DURATION

Quick SVT + VT3 screening: 20–30 minutes. Final candidate: 45–60 minutes; up to 60–90 minutes when needed to reach the temperature plateau. These are guidelines from my methodology. After reaching the temperature plateau, I check the profile with other algorithms and repeat startup tests.

077.4 TestMem5 / TM5



MY POSITION

I do not use TM5 myself: in my methodology, it did not provide any additional diagnostic information beyond what I already got from Karhu and y-cruncher. TM5 remains a popular free tool. In the screenshot, Universal 2 has already detected an error.

The original TestMem5 0.12 was written by Serj; CoolCmd continued its development. The current version, 0.13.1, fixes premature completion, an incorrect tested-memory size, and silent allocation errors. Run it as administrator and verify the TM5.exe/TM5.dll version.

THE CONFIG DETERMINES THE NATURE OF THE TEST

Config	Creator	Purpose	Role for Intel DDR5
DDR5 Intel / OptimalforIntelDDR5	anta777	Profile specifically for Intel DDR5	The most logical starting point
Universal 2	LMHz	Modern general-purpose profile; default in 0.13.1	Quick general check
Absolut	anta777	Profile focused on testing the memory array	Final independent check
Extreme	anta777	Older, long-running general-purpose profile	Usable, but not DDR5-specific
1usmus v3	1usmus	Short diagnostic profile	Historical; do not treat it as the DDR5 standard
Default	Serj	Original baseline sequence	Not the best choice for modern overclocking

KARHU AND TM5 APPROACH A SIMILAR TASK DIFFERENTLY

Characteristic	Karhu RAM Test	TestMem5 0.13.1
Model	Single closed algorithm	Engine with user-defined configs
Progress	Time and coverage	Specified duration, sequences, and tests
Configuration	Cache, RNG, FPU, memory size, and threads	Patterns, blocks, duration, and order
Repeatability	Easier to compare identical runs	The result depends more heavily on the config
License	Paid	Free

AN ERROR NUMBER IS NOT A READY-MADE DIAGNOSIS

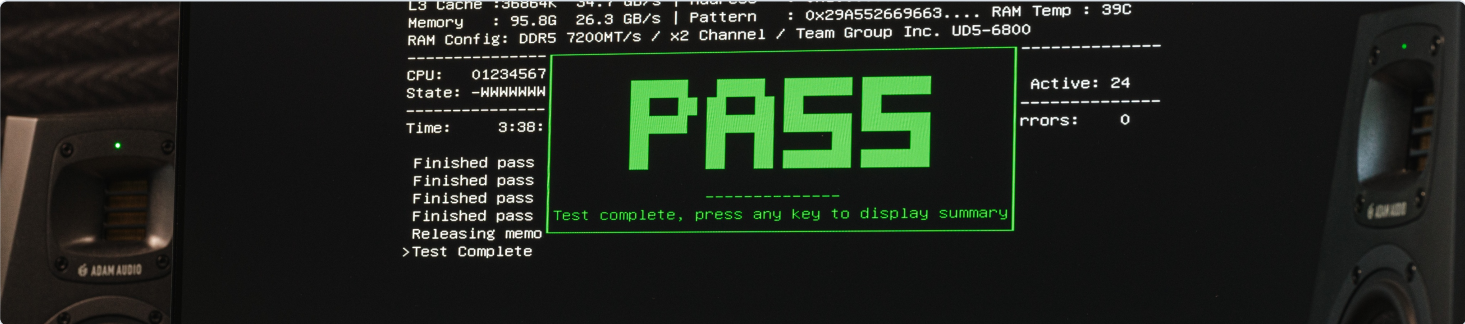
Tables that map ‘error N’ to a specific timing are based on community observations and depend on the config. Use them only as weak hints. For A/B comparisons, 10–30 minutes is enough; you can test a candidate profile for 1–2 hours with DDR5 Intel or Universal 2, then confirm it with another algorithm.

DO NOT USE RANDOM REPACKS

The official 0.13.1 binaries are unsigned and may trigger antivirus heuristics. That does not justify using archives with unknown TM5.dll, MT0.dll, or EXE files: the required popular configs are already included in CoolCmd’s release.

07 7.5 MemTest86 FREE / PRO

PassMark MemTest86 v11.7 Build 1000 is a standalone UEFI application. Write the image to a USB drive, select the drive in the Boot Menu, and MemTest86 then runs without Windows or Linux. It is used for basic and service diagnostics of memory kits in UEFI mode.



CONFIGURATION FOR DDR5

Setting	Practical choice	Meaning
CPU Mode	Parallel	Fastest standard mode; Single/Round Robin/Sequential are only for diagnosing UEFI or CPU cores
Passes	4 passes	Free: maximum of 4; the first is shortened, the next 3 are full. Four full passes are available only in Pro/Site through PASS1FULL=1
Tests	Free: 0–10, 13; Pro/Site: 0–13	Tests 11/12 are 64/128-bit tests available only in Pro/Site; Test 13 Row Hammer is available in Free
Test 14 DMA	Disabled by default	Additional DMA/USB diagnostics, not a standard memory-overclocking test

FOUR PASSES BEFORE BOOTING THE OS

PassMark’s official example is about 15 minutes for one pass and 120 minutes for four, but this is not a universal average: RAM capacity, CPU, selected tests, and cache mode can radically change the time. In Free, four passes consist of one shortened pass and three full passes. PASS1FULL=1 makes the first pass full, but it is available through mt86.cfg only in Pro/Site. Even four error-free passes do not replace Karhu/y-cruncher under an operating system.

FREE, PRO, AND ECC

Feature	Free	Pro
Core tests	Up to 4 passes; up to 16 logical CPUs; without Tests 11/12	Up to 999 passes; more CPUs; Tests 11/12 available
Automation	Manual launch and standard report	mt86.cfg, profiles, advanced reports, and cache policy
ECC	Detection and reporting of supported system ECC	ECC injection on compatible CPU/IMC combinations as well

HOW ON-DIE ECC AND SYSTEM ECC WORK

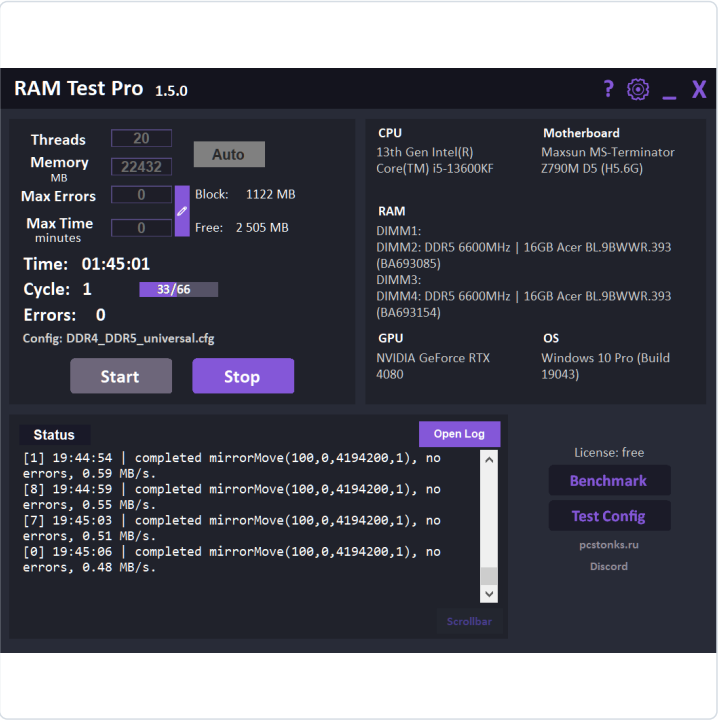
DDR5 on-die ECC corrects errors inside the DRAM device but does not protect data transfer over the channel. ECS (Error Check and Scrub) counters are accessible through registers when supported by the platform; this is not a system ECC report. Side-band ECC, meaning correction using additional ECC bits, requires a compatible CPU/IMC, motherboard, and ECC DIMM. Corrected ECC errors—errors corrected and logged by ECC—must not be ignored either; ECC injection in Pro verifies the mechanism by deliberately introducing an error, rather than testing an ordinary UDIMM.

TEST 13 HAMMER AND TEST 14 DMA

Leave Hammer enabled: it searches for row-disturbance bit flips in adjacent rows caused by frequent activations and tests a distinct class of risks associated with refresh (periodic restoration of cell charge). DMA—direct device access to memory without normal CPU handling—is experimental and disabled: its error may involve the USB drive or UEFI driver, so repeat the test with another flash drive.

077.6 RAM TEST PRO

RAM Test Pro 1.5.0 is a free 64-bit memory-testing utility for Windows 10/11 by **Svetlana (PCSTONKS)**. It combines configurable test sequences, error logging, WHEA monitoring, NUMA/Large Pages support, and a separate DDR2–DDR5 benchmark.



PCSTONKS RECOMMENDATIONS

FROM THE CURRENT RAM TEST PRO GUIDE

- Close unnecessary programs, free as much RAM as possible, and do not use the system during the run.
- Manual mode: at least 800 MB per block; more is better. Leave 300–500 MB of available free memory for the system.
- Test DDR5 for at least 6 hours; DDR4 for 3–4 hours.
- Monitor memory and CPU cooling; use only safe voltages.

MY INTERMEDIATE A/B STAGE

20–30 minutes is a short intermediate run. The final PCSTONKS check is at least 6 hours for DDR5.

WHAT SETS RAM TEST PRO APART

Component	What is implemented	Practical meaning
Engine	Its own x64 core and cfg format, according to Svetlana's description	Flexible configuration of test sequences and parameters
Algorithms	Inverse, mirror move, refresh, pseudorandom, and I/O/AVX	The sequence and parameters can be changed through a config
Diagnostics	Error location, log, WHEA, and stopping at a limit	More context than a single Errors counter
Platforms	Multicore CPUs, NUMA, and experimental Large Pages	Useful beyond a typical gaming system
Benchmark	Read/Write/Copy, latency, and random access	An additional comparison point, but not a replacement for AIDA64/MLC

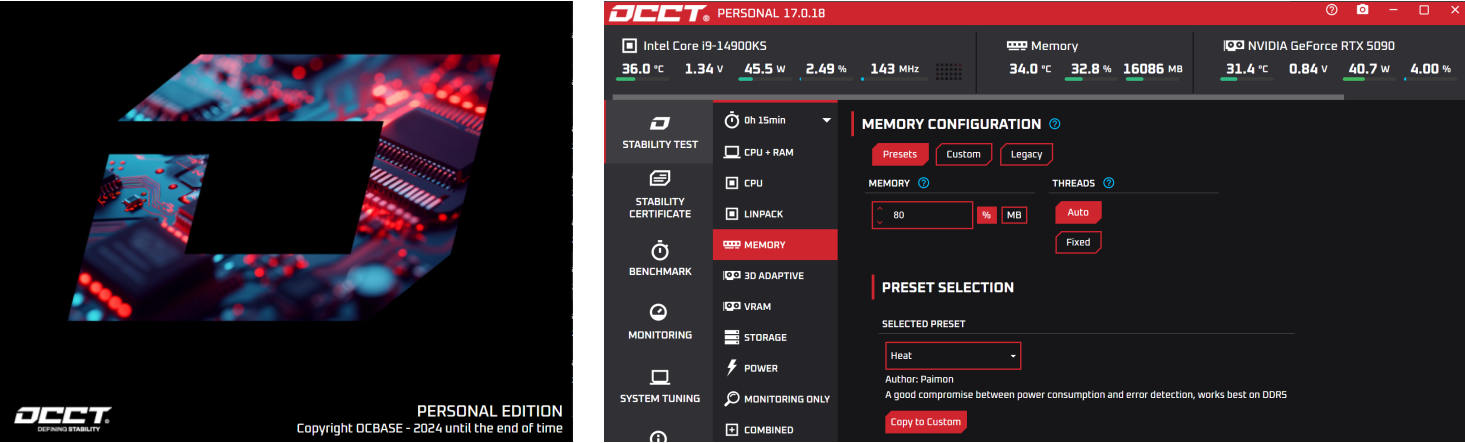
ADDITIONALLY:

Confirm RAM Test Pro results with y-cruncher, MemTest86 or another independent workload. Repeat the checks after cold starts and warm restarts.

07 7.7 ADDITIONAL TOOLS

These programs are optional, but they help quickly confirm a specific hypothesis and provide a second opinion. Karhu + y-cruncher remain the foundation of my methodology; Svetlana’s (PCSTONKS) RAM Test Pro is covered in 7.6 as a free alternative for an additional check. Always save the version, settings, duration, temperature, and first error together with the screenshot.

OCCT MEMORY CONFIGURATION EXAMPLE



Tool	When useful	Limitation	Practical duration
OCCT Memory	Quickly catches transfer, frequency, and timing errors under Windows	Cannot see memory occupied by the operating system	15–30 minutes
OCCT CPU + RAM	Tests the overall CPU and memory path; monitors WHEA	More difficult to isolate the cause	20–45 minutes
HCI MemTest 7.0	Simple alternative Windows RAM test	More manual setup; slower than Karhu. Pro makes thread allocation easier	400%+ as a basic reference point
Real-world workload	Game, archiver, compilation, rendering, and system sleep	Does not provide controlled coverage	Normal work cycle

7.8 RECOMMENDED TEST COMBINATIONS AND DURATIONS

Stage	Primary combination	What it covers	Guideline
One timing	Karhu	Quick feedback on the latest change	10–30 minutes
Frequency / power	y-cruncher SVT + VT3, then FFTv4	CPU/cache versus IMC/RAM and a large working set	20–30 minutes
Candidate profile	y-cruncher + Karhu; TM5/RTP are only additional cross-checks	Different algorithms under Windows	45–60 minutes + 1–3 hours of Karhu
Pre-boot	MemTest86 4 passes	Gross address, bit, and Hammer errors	Until completion
Final daily profile	MemTest86 + y-cruncher + Karhu + cold/warm boot	Data, IMC, temperature, and repeatability	4 passes + 45–60 min + 3–6 hr of Karhu

THERE IS NO UNIVERSAL ‘N HOURS IS ENOUGH’

The smaller the change, the shorter the intermediate test. A long final run begins only after the profile has survived several short A/B checks. If an error appears within a minute, there is no reason to wait out the remaining hours; if it appears only after warm-up, first establish the temperature threshold.

RECOMMENDED FOUNDATION OF THIS MANUAL

The foundation of my methodology is Karhu + y-cruncher; MemTest86 adds an independent UEFI check. The 1–3 and 3–6 hour ranges apply specifically to Karhu and were not borrowed from PCSTONKS. TM5 or RTP are acceptable only as additional independent cross-checks: an error-free run in either does not replace the baseline Karhu criterion. Use OCCT and HCI only for a specific diagnostic task.

07 7.9 ERROR DIAGNOSIS AND COMPLETION CRITERIA

After an error, first establish the conditions under which it appears. Examine the test, time, temperature, WHEA, boot type, and latest change; then revert only one parameter.

SYMPTOM -> FIRST HYPOTHESIS -> NEXT TEST

Symptom	First hypothesis	What to do next
The data-error counter rises immediately	Latest OC change; CPU/cache, memory, IMC, or signal integrity	Revert the step; repeat from a known-good baseline; save the error text and conditions
The test cannot allocate memory	Requested allocation, program limitations, or available RAM	Reduce the allocation; check program settings and messages
The test runs unusually slowly	Paging (page transfers between RAM and disk), background load, or test mode	Check RAM/page-file use and repeat under comparable conditions
Error only after warm-up	tREFI/tRFC, DRAM VDD, cooling, or 2R	Record the SPD Hub temperature; lower tREFI or improve daily-use airflow
SVT and VT3 fail	CPU/cache, ring, CPU power, or an overall CPU/IMC, thermal, or power limit	Back off the CPU OC; compare SFTv4/SVT and OCCT CPU
SVT passes, but VT3/FFTv4 fail	IMC, VDD2/MC, TX/SA, memory, or signal integrity	Compare with Karhu; restore Auto ODT; check the voltage ranges
MemTest86 reports errors before the operating system loads	Gross memory/IMC instability, addressing, or UEFI/BIOS	JEDEC, another DIMM/slot, then repeat after Clear CMOS and cold training
Error only after cold boot	Non-repeatable training result or accelerated boot path	Disable MRC Fast Boot; perform three cold boots and compare runtime readback
WHEA without a RAM error	CPU/IMC/interconnect, not necessarily DRAM	OCCT CPU + RAM and a separate CPU test; check the WHEA log

Data errors and memory-allocation errors are counted separately. Paging (transferring memory pages between RAM and disk) can dramatically slow the test; it is not a sufficient explanation for a rising RAM-error counter.

DO NOT TREAT AN ERROR BY RANDOMLY RAISING VOLTAGE

SA, TX, MC/VDD2, and DRAM VDD/VDDQ each have useful ranges: excess voltage can degrade the signal and training and increase heat. Return to the last verified step and move one rail in small increments in both directions.

COMPLETION CRITERIA FOR A DAILY PROFILE

Step	Requirement	What to save
1	Four error-free MemTest86 passes	HTML/photo of the report and the 11.x version
2	45–60 minutes of y-cruncher SVT + VT3 + FFTv4	Version, memory allocation, limit, and initial/final temperature
3	Karhu for 3–6 hours; TM5/RTP only as an additional run	Duration, coverage, memory size, threads, and 0 errors
4	Three cold boots and three warm restarts; sleep if used	POST behavior, Q-Code, and trained values
5	Final thermal run with daily-use cooling	Maximum SPD Hub temperature, WHEA, and ambient temperature
6	Normal workloads show no regressions	Archiver/game/rendering and a backup of the profile

STOPPING POINT

The profile is ready when it passes different algorithms, remains reproducible after complete power removal, and retains margin at daily-use temperatures.

088.1 WHAT A BENCHMARK ACTUALLY MEASURES

For DDR5, evaluate bandwidth, latency, cache effects and performance in real workloads. Check stability using the method in Chapter 7.

A comparison is meaningful only within the same program and version, with identical CPU/Ring frequencies, Windows background load, cooling, and operating-system security-feature state.

FOUR DIFFERENT TYPES OF RESULTS

Metric	What it shows	What affects it most
Read	Speed of reading data from memory	Frequency, IMC, Gear, channels, threads, and test implementation
Write	Speed of writing data to memory	CPU/IMC architecture, frequency, timings, and algorithm
Copy	Data copy: reading followed by writing	Entire memory path, cache, and working-set size
Latency	End-to-end access latency in nanoseconds	All timings, frequency, Gear, Ring/Uncore, and OS background activity

THREE LEVELS OF RESULT VALIDATION

1 SYNTHETIC

AIDA64, MLC, or OCCT shows the limit of a particular algorithm.

2 REAL-WORLD TEST

7-Zip, Cinebench, or a CPU-limited game checks whether the gain reaches the actual workload.

3 STABILITY

Chapter 07 searches for errors separately. A high score does not mean the profile is stable.

CHECK THE GAIN IN YOUR OWN WORKLOADS

Higher bandwidth does not guarantee better 1% lows, and lower AIDA64 latency will not ensure lower latency in a game. First evaluate the median across runs, then confirm the effect with a separate real-world workload.

RULE FOR THIS CHAPTER

Change one profile, keep the environment identical, and do not cherry-pick the best run. Do not count a difference smaller than the natural run-to-run variation as an improvement.

08 8.2 AIDA64 EXTREME



AIDA64 Cache & Memory Benchmark is a quick synthetic test for comparing profiles on the same system. According to the developer’s published description, Read/Write use a 64 MB block, while Copy transfers 32 MB and counts traffic in both directions. Latency uses random addresses within blocks.

HOW CACHE & MEMORY BENCHMARK WORKS

AIDA64 Cache & Memory Benchmark

	Read	Write	Copy	Latency
Memory	130.05 GB/s	126.38 GB/s	124.12 GB/s	49.8 ns
L1 Cache	6341.0 GB/s	4389.3 GB/s	9034.3 GB/s	0.9 ns
L2 Cache	1270.3 GB/s	659.36 GB/s	1007.3 GB/s	3.5 ns
L3 Cache	1002.6 GB/s	504.18 GB/s	738.58 GB/s	14.4 ns

CPU Type

8C+16c Intel Core i9-14900KS (Raptor Lake-S, LGA1700)

CPU Stepping

B0

CPU Clock

5898.6 MHz

CPU FSB

100.0 MHz (original: 100 MHz)

CPU Multiplier

59x

North Bridge Clock

4998.8 MHz

Memory Bus

4099.0 MHz

DRAM:FSB Ratio

41:1

Memory Type

Dual Channel DDR5-8200 SDRAM (36-48-48-60 CR2)

Chipset

Intel Raptor Point-S Z790, Intel Raptor Lake-S

Motherboard

Asus ROG Maximus Z790 Apex Encore

BIOS Version

1102

AIDA64 v7.20.6802 / BenchDLL 4.6.889.8-x64 (c) 1995-2024 FinalWire Ltd.

SaveStart BenchmarkClose

READ / WRITE

Multithreaded reads and writes. Higher is better.

COPY

Read + write through the CPU. Shows the entire path well.

LATENCY

Random access in ns. Lower is better; this is not just tCL.

MY REFERENCE 8200 BENCHMARK

130.05 / 126.38 / 124.12 GB/s and 49.8 ns on a 14900KS.

USEFUL TESTS FROM THE GENERAL BENCHMARK SECTION

Benchmark

- Memory Read
- Memory Write
- Memory Copy
- Memory Latency
- CPU CheckMate
- CPU PhotoWorxx
- CPU ZLib
- CPU AES
- CPU SHA3
- FPU Julia
- FPU Mandel
- FPU SinJulia
- FP32 Ray-Trace
- FP64 Ray-Trace

CORE SET

Memory Read, Write, Copy, and Latency directly compare the DDR5 profile.

CPU + MEMORY

CPU PhotoWorxx is especially sensitive to cache and latency; CPU ZLib has moderate memory sensitivity.

PRIMARILY CPU

AES, SHA3, Julia, Mandel, SinJulia, and Ray-Trace are useful as CPU checks, not as DDR5 evaluations.

Hardware Prefetcher on ASUS Z790 controls the MLC Streamer: it detects sequential accesses and fetches upcoming data into L2 ahead of demand. It is separate from Adjacent Cache Line Prefetch; the effect depends on the workload.

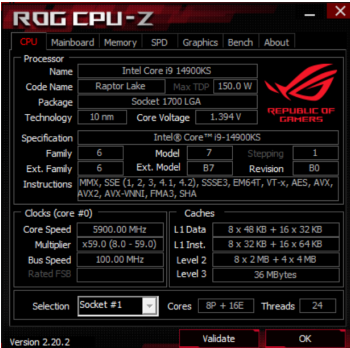
Disabling Hardware Prefetcher in BIOS reduces Read/Write/Copy. I don’t remember exactly which one it fucks up, but I think Copy takes the biggest hit.

08 8.3 CPU-Z: SETTINGS AND SPD

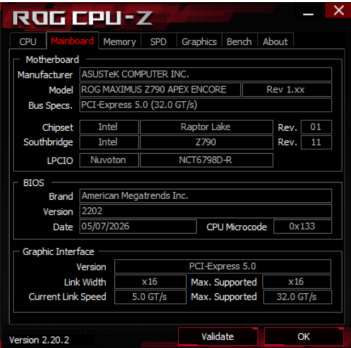
CPU-Z records the system configuration: CPU and motherboard models, BIOS version, actual memory clock, active primary timings and each module's SPD contents.

MY CPU-Z TABS: WHAT TO SAVE WITH THE RESULT

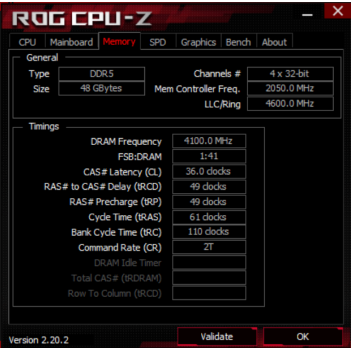
1. CPU



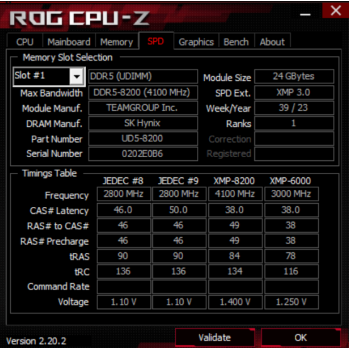
2. MAINBOARD



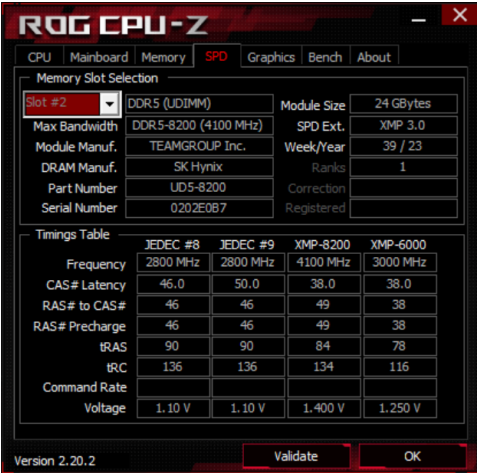
3. MEMORY



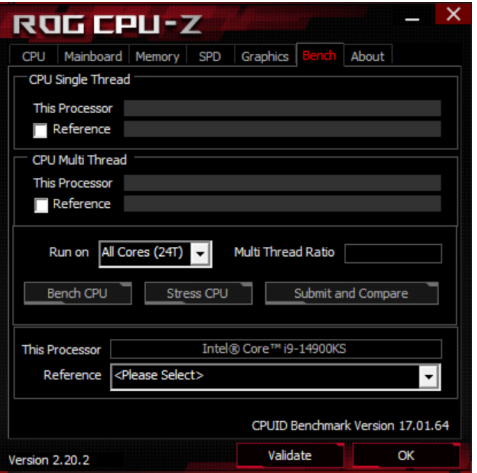
4. SPD / SLOT 1



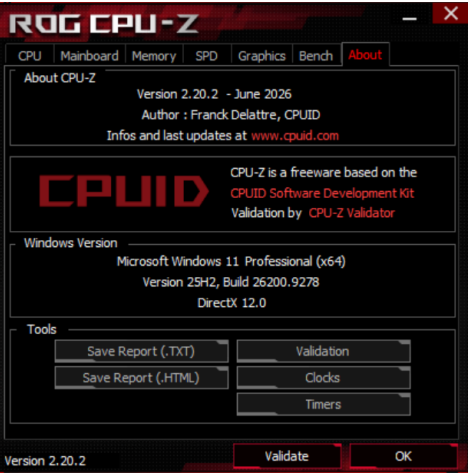
5. SPD / SLOT 2



6. BENCH



7. ABOUT



WHERE TO LOOK FIRST

Tab	What to check	How to read it
CPU / Mainboard	Model, stepping, BCLK, motherboard, BIOS, and microcode	Records the platform and CPU state for repeatability
Memory	DRAM Frequency, 4 x 32-bit, tCL/tRCD/trP/trAS/tRC, and CR	4100 MHz x 2 = DDR5-8200 ; these are the active parameters
SPD for every slot	Capacity, DRAM manufacturer, ranks, part/serial number, JEDEC, and XMP	SPD stores module profiles, but does not prove that XMP is currently active
Bench / About	Quick CPU score and exact CPU-Z version	Bench does not test memory; save the version with the screenshot

MEMORY AND SPD ANSWER DIFFERENT QUESTIONS

Memory shows what the system is running now. SPD shows the JEDEC/XMP profiles and identification data stored on the selected DIMM. CPU-Z Validation records the configuration and frequency, but does not confirm stability.

08 8.4 HWiNFO: MONITORING



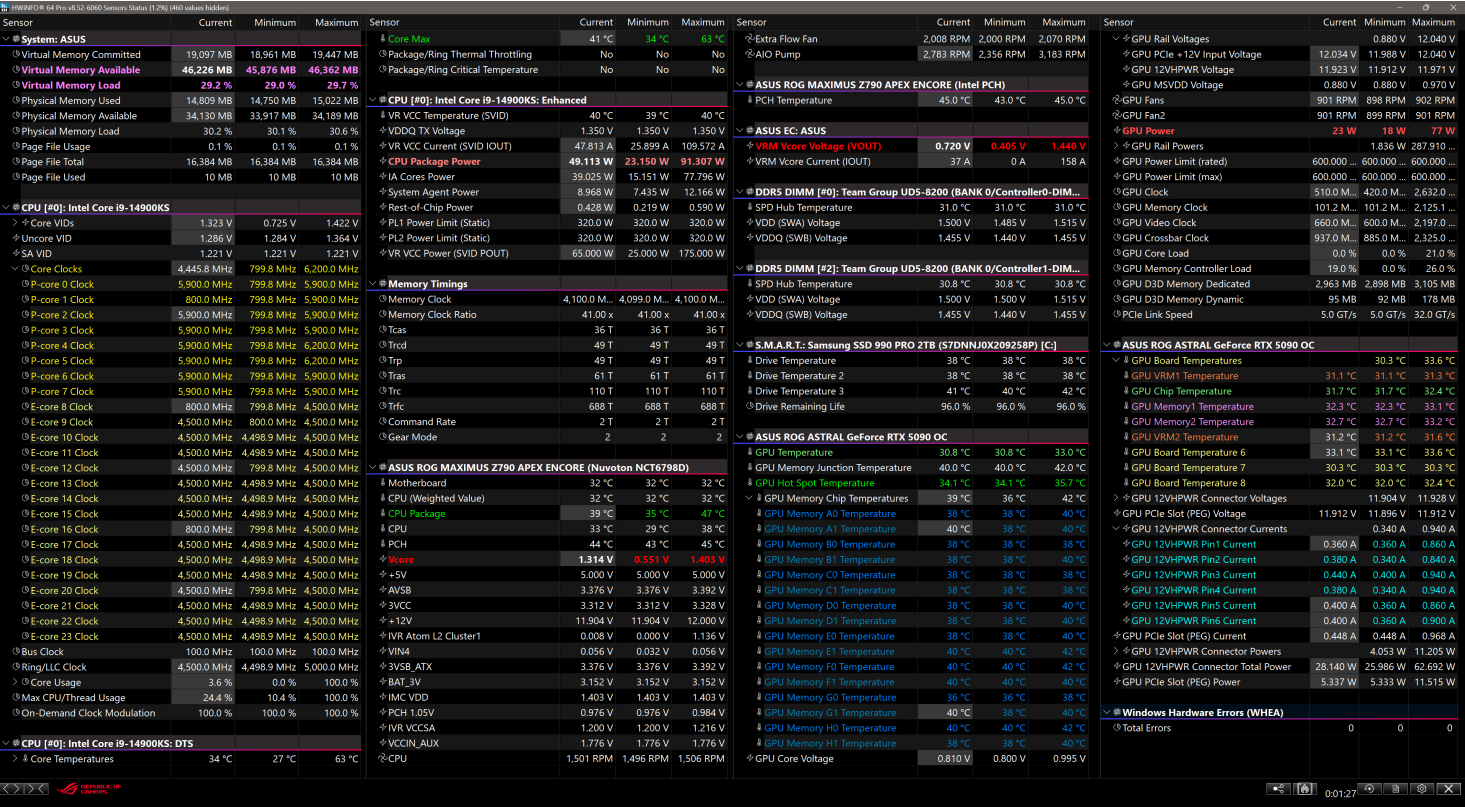
HWiNFO is my primary and, in my view, the best monitoring tool. It simultaneously shows module temperatures, actual* voltages, CPU/Ring frequencies, throttling, and WHEA counters.

* The readings are estimates: PMIC telemetry may be inaccurate. Actual voltage and ripple are checked with an oscilloscope.

MINIMUM SENSOR SET

Reading	What to save	Important nuance
SPD Hub Temperature	Current, Maximum, and Average for each DIMM separately	This is the SPD Hub temperature, not the temperature of the DRAM dies themselves
VDD / VDDQ	Readings from both modules	When supported; recheck anomalies with PMIC and software limitations in mind
Memory Timings	Memory Clock, Gear, and active timings	Quick check that the system loaded the intended profile
CPU / Ring	Frequencies, power limits, and indications of throttling	A different CPU mode changes benchmark results
WHEA	Counter before and after the run	An increase requires diagnosis, but does not automatically implicate RAM

MY WORKING SENSORS SCREEN



DOCUMENTATION REVIEWED: HWiNFO 8.55 documentation and developer guidance on SPD Hub Temperature and WHEA. Screenshots: my system.

08 8.4.1 HWiNFO: MEMORY TIMINGS WINDOW

In addition to the basic Memory Timings section in Sensors, HWiNFO can open a separate ‘Memory Timings’ window with an expanded set of active memory parameters. This is convenient for checking the values actually applied after memory training, including AUTO settings calculated by the platform.

In Sensors-only mode, the window is available from the context menu of the HWiNFO notification-area icon.

WHAT THE SEPARATE WINDOW ADDS

Additional secondary, tertiary, and turnaround timings: tFAW, tRRD_S/L, tWTR_S/L, tRDPRE, tRDPDEN, tWRPRE, tWRPDEN, tRDRD/tRDWR/tWRRD/tWRWR sg/dg, and others; plus some internal parameters, including RTL. The available fields depend on the platform and HWiNFO version.

HWiNFO® 64 Pro v8.55-6095 - Memory Timings @ ASUS ROG MAXIMUS Z790 APEX ENCORE

DIMM

Team Group UD5-8200 #0: BANK 0/Controller0-DIMM0

[24 GB] DDR5-8200 / PC5-65600 DDR5 SDRAM UDIMM, SK Hynix, 1R

PMIC5100: Richtek Power

Clock

	Ratio	RefClk	Clock	EffClock
MCLK	41.00 x	100.0	= 4100.0	
UCLK	20.50 x	100.0	= 2050.0	

SPD W-P

Channels 4

Gear Mode 2

PMIC1 CKD

PMIC2 (M)RCD

PMIC3 (M)DB

Timing

MC #0, CH #0	CR	2	tFAW	32	tWR	47	tCKE	8	
tCL	36	tCWL	34	tRRD_S	8	tWTR_S	8	tCPDED	21
tRCD	49	tRFC	688	tRRD_L	12	tWTR_L	18	tXP	26
tRCDwr		tRFC2		tRDPRE	12	tWRPRE	89	tXPDLL	63
tRP	49	tRFCpb	604	tRDPDEN	44	tWRPDEN	90	tXSDLL	2559
tRAS	61	tXSR	1282			tWTP		RTL	70 / 25 / 25 / 25
tRC	110	tREFI	131071						

Same Chipselect

Same Bank Group

Different Bank Group

Same DIMM

Different DIMM

tRDRD_sc		tRDRD_sg	16	tRDRD_dg	8	tRDRD_dr		tRDRD_dd	
tRDWR_sc		tRDWR_sg	22	tRDWR_dg	22	tRDWR_dr		tRDWR_dd	
tWRRD_sc		tWRRD_sg	62	tWRRD_dg	52	tWRRD_dr		tWRRD_dd	
tWRWR_sc		tWRWR_sg	16	tWRWR_dg	8	tWRWR_dr		tWRWR_dd	

DIMM SPD Write-Protection

Team Group UD5-8200

#0: BANK 0/Controller0-DIMM0

[24 GB] DDR5-8200 DDR5 SDRAM, SPD Hub: Montage Technology Gr

SPD Block Status

Base Config

Module Parameters

Manuf Info

XMP / EXPO / Programmable

Some SPD blocks that should not be modified are not write-protected.

Set recommended values

Write-Protect

Close

HWiNFO: advanced memory timings and SPD write-protection status

WARNING: DIMM SPD WRITE-PROTECTION

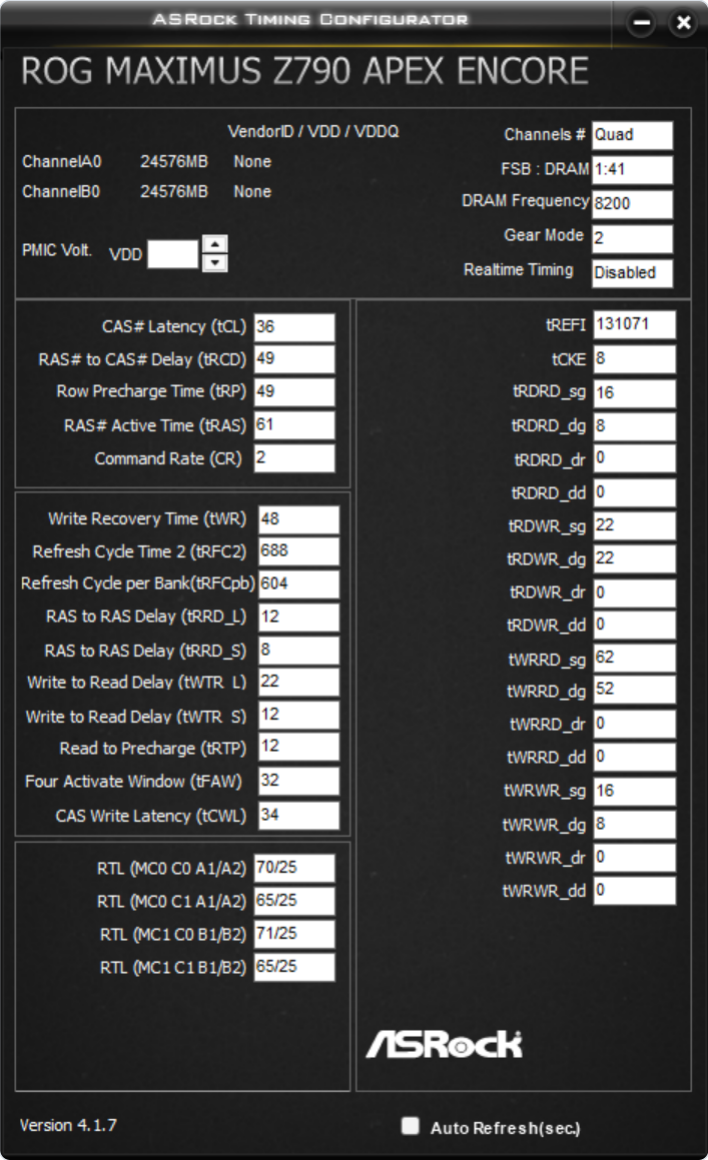
“Some SPD blocks that should not be modified are not write protected.”

This warning indicates the state of SPD write protection; it is not a timing read error. Changing SPD Write-Protection or using SPD write functions without understanding the consequences is not recommended. None of this is required for ordinary timing monitoring.

08 8.5 ASROCK TIMING CONFIGURATOR

ASRock Timing Configurator 4.1.7 is a convenient utility for viewing active primary, secondary, and tertiary timings directly in Windows. It provides a compact record of settings, including on compatible ASUS motherboards.

MY DDR5-8200 PROFILE ON Z790 APEX ENCORE



TOP

Motherboard, capacity, DRAM Frequency, FSB:DRAM, Gear Mode, and channel mode.

LEFT

Primary and major secondary timings, including tRFC and tFAW.

RIGHT

tREFI, tCKE, sg/dg/dr/dd transitions, and other BIOS-trained values.

IMPORTANT

Zeros may indicate a path that does not apply to 1R/1DPC. Compare the same platform and BIOS.

WINDOWS 11 CAVEAT

Memory Integrity/Core Isolation may block the utility’s driver. I do not recommend disabling security specifically to capture a timing screenshot: if the program does not launch, use the BIOS, CPU-Z, and HWiNFO.

WTR calculations depend on the utility version; DDR4/DDR5 formulas and corrections are compared in 3.7.

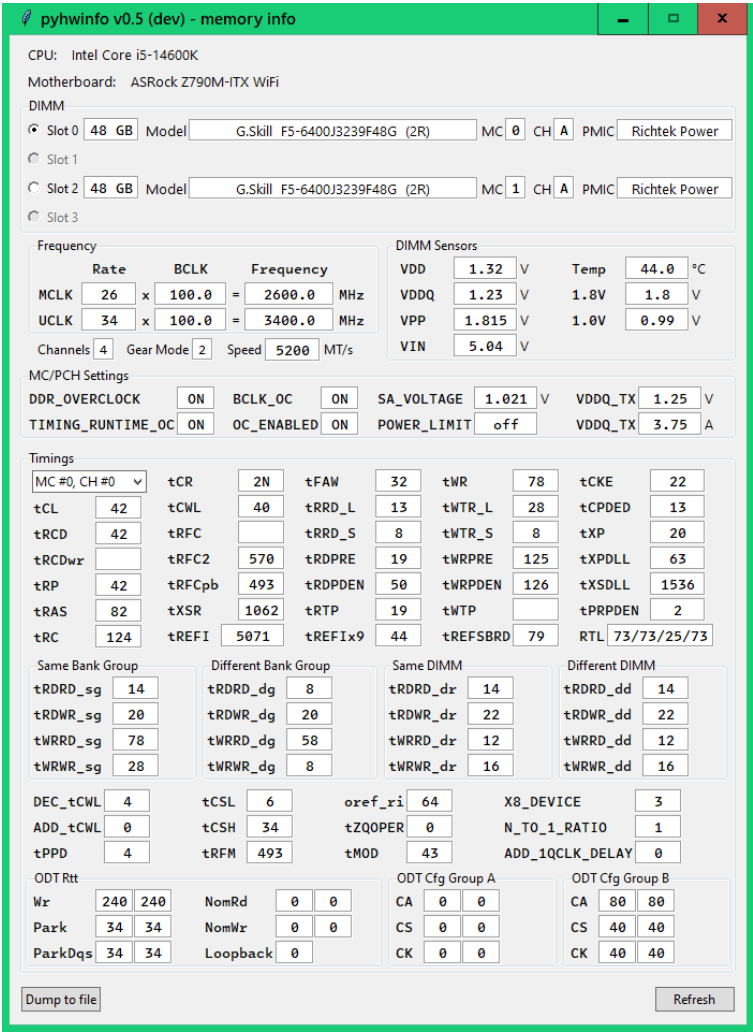
08 8.6 pyhwinfo: LOW-LEVEL MEMORY AND IMC SETTINGS

pyhwinfo 0.8 dev is a low-level diagnostic utility for DDR5 overclocking. It reads applied memory and IMC parameters that ordinary monitoring shows only partially or not at all.

WHAT IT LETS YOU CHECK

MCLK / UCLK / BCLK (interface fields), memory data rate, and Gear Mode; primary / secondary / tertiary timings by channel and MC0/MC1; RTL; ODT (Wr, Park, ParkDqs, NomRd, NomWr, and others); Vref; SA VID, VDDQ TX, AC_LL / DC_LL; DIMM, SPD / PMIC, and available module voltages and temperatures.

After Memory Training, it lets you compare BIOS settings with the values actually applied. Checking AUTO, tertiary/turnaround timings, RTL, ODT, and Vref is especially useful because the platform calculates them during training.



pyhwinfo: low-level DDR5 and memory-controller parameters

Screenshot shows v0.5 (dev): MC/PCH Settings section; separate Vref and AC_LL/DC_LL values are not shown here.

COMPATIBILITY LIMITATIONS

Supported systems use Windows 7 or later, Intel Core 12th/13th/14th/15th generations and DDR5. AMD and DDR4 support is not claimed. The project is in development: platforms, fields, and the interface may change. Low-level values require an understanding of DDR5/IMC; their purposes are covered in the relevant chapters.

SOURCES: pyhwinfo README and source code (September 11, 2026); OCN — link to the dedicated discussion.

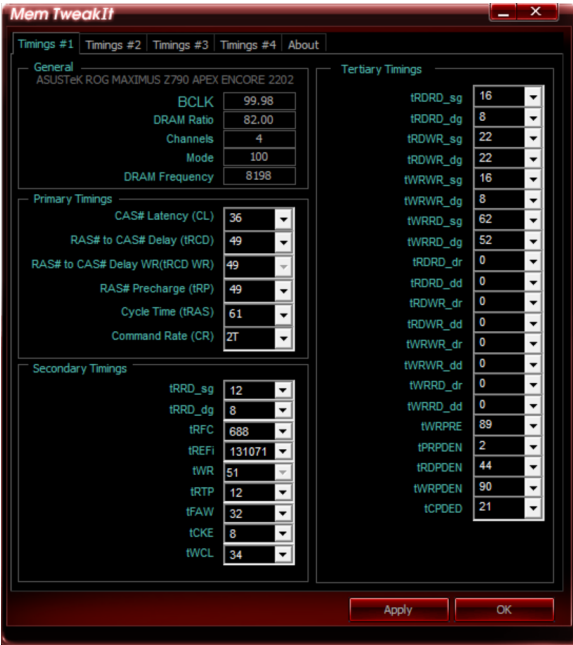
GitHub — pyhwinfo / remittor OCN — pyhwinfo: open-source tool for showing memory timings

08 8.7 ASUS MemTweakIt

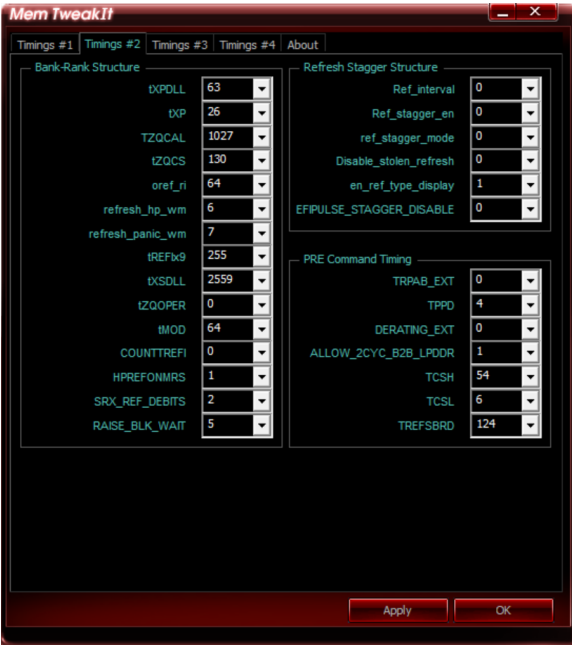
ASUS MemTweakIt shows more internal parameters than the compact ATC. On my Z790 Apex Encore, four tabs collect the primary, secondary, and tertiary timings, refresh behavior, scheduler, and RTL. In this manual, I use it to capture a detailed record of settings.

FOUR PAGES OF ONE DDR5-8200 CONFIGURATION

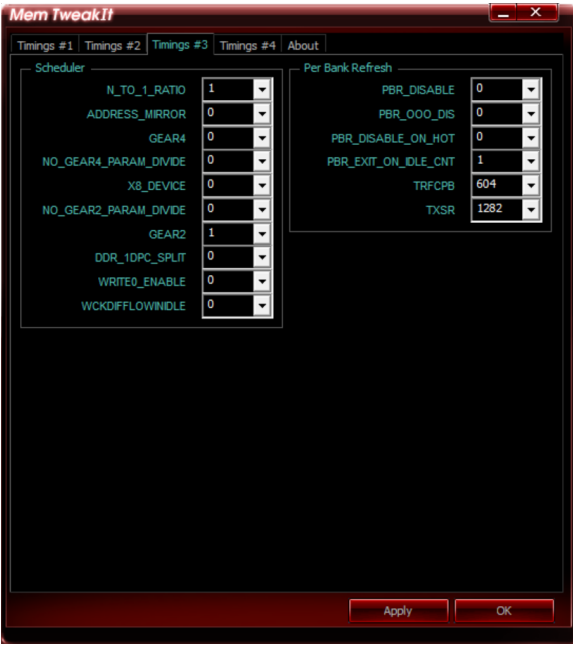
TIMINGS #1 / PRIMARY



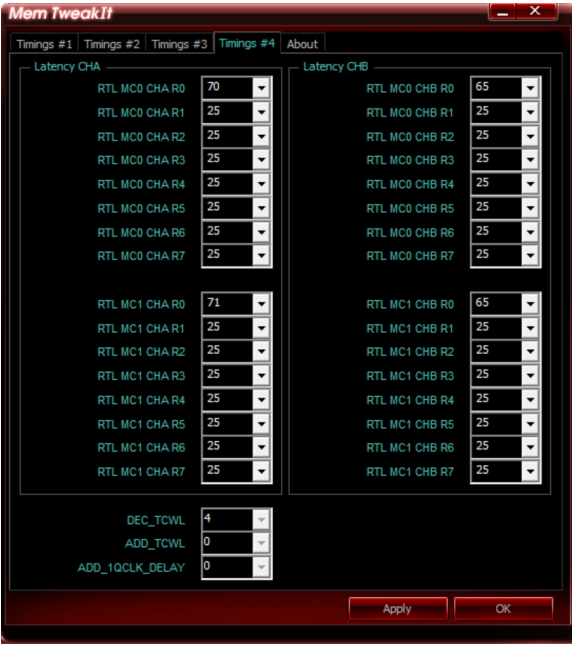
TIMINGS #2 / REFRESH



TIMINGS #3 / SCHEDULER



TIMINGS #4 / RTL



CHANGING TIMINGS FROM WINDOWS

Even when the fields are active, I use MemTweakIt only for reading and screenshots. Writing can crash the system instantly, and some values depend on the BIOS version and the utility itself. The current build is distributed by the community, not through the official ASUS catalog: verify the archive before running it.

WR calculations depend on the MemTweakIt version; the old and DDR5 formulas are compared in 3.7.

DOCUMENTATION REVIEWED: ASUS MemTweakIt manuals; HWBOT Z790 Apex community build and discussion. Screenshots: my system.

08 8.8 CURRENT ALTERNATIVE BENCHMARKS

AIDA64 is usefully supplemented with one independent synthetic test and one real-world test. Results from different programs cannot be converted into one another: each uses its own working set and algorithm.

Tool	What it measures	When useful	Limitation
Intel MLC 3.13	Bandwidth and latency under increasing load	In-depth IMC and memory analysis	CLI; record launch parameters
OCCT 17.1.8	Latency & Bandwidth L1/L2/L3/RAM	Modern graphical alternative to AIDA64	Compare OCCT only with OCCT
7-Zip 26.04	Compression/Decompression LZMA	Real-world response of CPU, cache, and RAM	Same dictionary and thread count
Cinebench 2026	Redshift scene rendering on the CPU	CPU score; tight timings sometimes add a few points	Not a memory test; gains may be within run variance
CapFrameX / PresentMon	Frame time, average FPS, and low percentiles	Benefit in a CPU-limited game	A GPU limit hides the effect
RTP Benchmark	Read/Write/Copy and random-access latency	An additional data point within RAM Test Pro	Methodology still developing

8.9 STANDARDIZED PROTOCOL: MAKING THE NUMBERS REPRODUCIBLE

Step	Action	What to record
1	Prepare an identical environment	BIOS, Windows, program versions, power, background activity, and cooling
2	Record the configuration	CPU-Z Memory/SPD and an ASRock Timing Configurator screenshot
3	Open HWiNFO Sensors	SPD Hub, VDD/VDDQ, WHEA, CPU/Ring, and throttling
4	Run five passes	Same test order, pauses, working set, and warm-up
5	Calculate the median and spread	Do not use the best run; do not count a small difference as a gain
6	Confirm with a workload	7-Zip, Cinebench, or a game; Chapter 07 searches for errors separately

MINIMUM REASONABLE TOOL SET

CPU-Z and Timing Configurator record the settings, HWiNFO records the conditions, AIDA64 provides the familiar synthetic test, MLC or OCCT provides an independent data point, and 7-Zip, Cinebench, or a CPU-limited game shows the practical effect.

09 SOFTWARE: WEBSITES, DOWNLOADS, AND MANUALS

Here I have collected links to the programs from Chapters 07 and 08. The link titles are clickable.

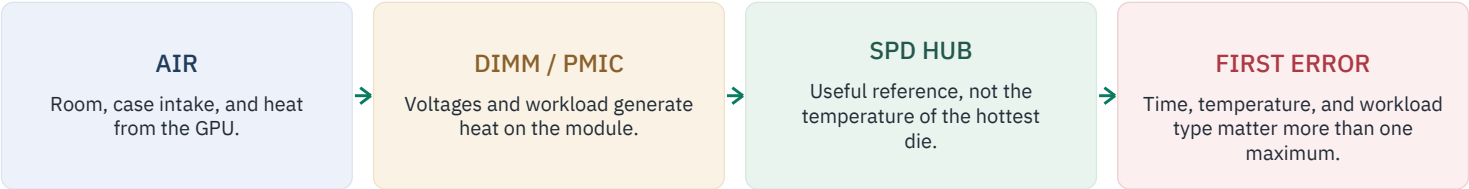
y-cruncher	§ 7.2
Windows and Linux; free. The direct link below is the Windows 0.8.7.9547b archive.	
Official website · Windows archive · Help / FAQ	
Karhu RAM Test	§ 7.3
Windows; paid license. The developer sends a download link after purchase.	
Site / purchase · README guide	
TestMem5 (TM5)	§ 7.4
Windows; free. Current CoolCmd branch; the archive includes the program and configs.	
CoolCmd repository · Latest 7z archive · README instructions	
MemTest86	§ 7.5
Boots from USB in UEFI. Free is available; the Pro distribution is provided after purchase.	
Official website · Downloads · Free archive · PDF guide	
RAM Test Pro / RTP Benchmark	§ 7.6 / 8.8
PCSTONKS; free memory test and built-in benchmark. Windows 1.5.0 archive.	
Website and guide · Windows archive	
OCCT Personal	§ 7.7 / 8.8
OCCT 17.1.8; Windows and Linux. Personal and paid-edition terms are on the website.	
Official website · Downloads · Windows Stable · Guide	
HCI MemTest	§ 7.7
Windows. A free version for home/noncommercial use and a paid Pro version are available.	
Official website · Free archive · Guide	
Monitoring · HWiNFO	§ 7.9 / 8.4
HWiNFO 8.54: sensors and logging. HWiNFO64 is free for noncommercial use.	
Official website · Downloads · EXE installer · Portable ZIP	
AIDA64 Extreme	§ 8.2
Version 8.40.5000; Read/Write/Copy and latency; limited 30-day trial.	
Site / downloads · EXE Windows · ZIP Portable · Guide	
CPU-Z / Validator	§ 8.3
Frequencies, timings, SPD, and configuration recording.	
Website and help · EXE Windows · ZIP Windows · Validator V3 · Validator: portal	
ASRock Timing Configurator 4.1.7	§ 8.5
Windows; displays active timings. Official ASRock archive.	
ASRock archive · FAQ ASRock	
pyhwinfo	§ 8.6
Version 0.8 dev; Windows, Intel DDR5. In development; limitations are covered in 8.6.	
Repository and instructions · OCN thread · master branch ZIP	
ASUS MemTweakIt	§ 8.7
Timing viewer; the Z790 build is community-hosted.	
Community build · HWBOT thread · ASUS guide (Z390)	
Intel MLC	§ 8.8
Memory latency and bandwidth under load.	
Intel downloads · Description and commands	
7-Zip	§ 7.8
Archiver and compression/decompression benchmark.	
Downloads · EXE Windows x64	
Cinebench	§ 7.8
Cinebench 2026.1.3: CPU/GPU rendering benchmark.	
Downloads · ZIP Windows x86-64 · Description and requirements	
CapFrameX	§ 7.8
CapFrameX 1.9.1: frame times; requires .NET 10 Desktop Runtime x64.	
Downloads · Installer ZIP · Portable ZIP · Guide	
Intel PresentMon	§ 7.8
Frame time capture; application and console version.	
Repository · Release/downloads · MSI installer · Console EXE x64 · Guide	

1010.1 DIMM COOLING AND THERMAL STABILITY

Check stability at operating temperature once thermal conditions have stabilized. A successful test immediately after a cold boot says nothing about memory behavior an hour later, after the DIMMs, PMIC, case air, and area around the CPU have warmed up.

The SPD Hub sensor is useful as a repeatable reference point, but it measures its own local temperature, not the hottest DRAM die. Some modules have no sensor at all. The trend for one kit and the temperature at the first error therefore matter more than someone else’s universal number.

THERMAL LOOP: RECORD THE ENTIRE CHAIN



WHAT TO RECORD DURING THE TEST

Metric	Why it is needed	How to interpret it
SPD Hub Temperature	SPD Hub temperature of each module where a sensor is available	Watch Current and Maximum; compare identical sensors on the same test bench
VDD / VDDQ and RPM	Links heat to voltage and actual airflow	Higher voltage may reduce thermal margin even if POST becomes easier
Time to first error	Shows whether the error is related to warm-up	Repeat the same test with the same settings and different airflow
Case temperature	Distinguishes a cold test bench from a real scenario	Test the final profile in the normal closed case with heat from the GPU

PRACTICAL SEQUENCE

1. COLD BASELINE
- Start the selected test and record the initial temperature, VDD/VDDQ, fan speed, and system background load.
2. STEADY-STATE WARM-UP
- Do not change conditions until the temperature plateaus; an early pass does not establish stability after warm-up.
3. REAL-WORLD WORST CASE
- Repeat the workload in a closed case and, if typical for your use, with the graphics card warmed up.
4. DIAGNOSTIC AIRFLOW
- With settings unchanged, direct airflow at the DIMMs. If the errors disappear, this indicates inadequate thermal margin, but it does not replace repeat testing.

PRACTICAL CONCLUSION

For high-frequency DDR5, directed airflow over the modules is part of the working configuration. With heat-related errors, first improve airflow and loosen aggressive refresh parameters; mindlessly adding VDD/VDDQ may only increase heat.

THERE IS NO SINGLE SAFE TEMPERATURE FOR EVERY OVERCLOCK

The threshold depends on the ICs, voltages, timings, DIMM construction, sensor, and case. Temperature grades and doubled-refresh thresholds stated in a datasheet must not be presented as guarantees of stability for an overclocked profile.

10

10.2 SOCKET, MOUNTING PRESSURE, AND IMC VARIATION

The IMC (Integrated Memory Controller) is located in the CPU, and its signals pass through the LGA contacts, motherboard traces, and DIMM slots. A missing channel, a sharp deterioration in training after remounting, or instability on one channel therefore calls first for mechanical diagnosis at JEDEC settings, not additional voltage.

A contact frame changes socket geometry and pressure distribution. It may affect temperature and contact, but it does not improve the IMC’s intrinsic quality or guarantee a higher memory data rate.

SIGNAL PATH



ISOLATE THE PROBLEM BEFORE TRYING TO FIX IT

Symptom	What to rule out	Action
A channel or DIMM is not detected	Module, slot, contamination, and socket contacts	One known-good DIMM in each recommended slot; then inspect the CPU and LGA
Training became worse after installing the cooler	Misalignment, tightening sequence, and tightening force	Return to the specified mounting procedure and retrain the memory completely
One channel is consistently weaker	Whether the error follows the module or the channel	Swap the DIMMs; repeat at JEDEC, then with the original profile
The frame lowered CPU temperature	Mistaking correlation for causation	Do not claim an IMC improvement without a repeatable increase in frequency or stability margin

SAFE REINSTALLATION

1. JEDEC, THEN REMOVE POWER

Save the profile and test at JEDEC. Shut down the PC, switch off the power supply, and unplug the power cord; make sure standby power is gone.

2. INSPECT THE SEATING

Follow the motherboard’s ESD instructions; hold the CPU and DIMMs by the edges. With the motherboard horizontal, place the CPU without sliding it or touching the LGA contacts.

3. FOLLOW ONE MANUAL

Tighten the cooler or frame only in the sequence and to the force specified by its manufacturer; do not transfer torque values from other hardware.

4. RETRAIN AND RETEST

After any remounting, clear saved training and repeat cold-boot, warm-restart, and stress testing.

HOW TO COMPARE IMC CAPABILITY

Even CPUs of the same model have different memory-controller headroom. Compare several training cycles on the same motherboard, with the same DIMMs and temperature. A random lucky POST and high SA are not measurements of IMC quality.

MOUNTING AND PRESSURE—FOLLOW THE MANUAL ONLY

LGA1700 and LGA1851 processors and sockets are incompatible, although cooler-mount geometry has been retained. Transfer contact frames, washers, and tightening torques only when supported by a component datasheet or manufacturer’s manual.

10

10.3 BIOS, MRC, AND REPEATABILITY

The BIOS version is part of the profile. An update may change MRC (Memory Reference Code, the memory-initialization code), CPU microcode, Intel ME, hidden Auto values, and Memory Fast Boot. Identical visible timings after a flash therefore do not guarantee the same training state.

For the Z790 Apex Encore, ASUS explicitly associates BIOS 2202 with the Intel IPU 2026.1 update and memory compatibility; ME changes at the same time, and its new version may remain after a BIOS rollback. Such a rollback does not always restore the previous software stack.

Stage	What to do	What to record
Before flashing	Screenshots and manual records of every changed setting	BIOS, ME/CSME, microcode, MRC/Silicon Init, Memory Fast Boot, and trained values
Safe baseline	Return to a stable profile or JEDEC before flashing	Control run and absence of errors before the update
First boot	Reset to Defaults, JEDEC, and complete training	POST codes, training time, and values actually applied
Profile recovery	Enter settings manually; do not blindly load the old profile	Cold boot, warm restart, hot stress test, and sleep behavior
Comparison	Change only the BIOS while keeping hardware and conditions identical	If ME or microcode differs, mark the comparison as non-equivalent

NEW BIOS—NEW TEST PLATFORM

Use a profile from another version as a reference. After updating, repeat several cold boots, several warm restarts, and the complete memory test; verify stability after warm-up.

10.4 DATA INTEGRITY AND A SAFE ENVIRONMENT

Unstable memory is dangerous for more than blue screens: an error can enter an archive, project, file system, or synchronized folder without any obvious warning. An experimental profile must not operate on the only copy of important data.

What to protect	Practical action	Verification
Important files	A 3-2-1 scheme, or at minimum a separate version on another medium/in the cloud	Open several files from the backup and know the restore procedure
OS and keys	Separate test installation/image; keep the BitLocker key off the test bench	Do not experiment in the only production environment
Firmware	Flash the BIOS only with known-stable memory and power	Do not update the BIOS on a marginal profile just to save one retraining cycle
Results	Store test logs, WHEA data, and settings outside a temporary folder	The last known-good point remains available after a failure

NO BENCHMARK IS WORTH DATA LOSS

Synchronization does not replace backups: if a file becomes corrupted, its corrupted version may spread to every device.

1010.5 SYNTHETIC AND REAL-WORLD PERFORMANCE

AIDA64 and Intel MLC let you assess changes in memory bandwidth and latency, but their results do not directly indicate FPS gains, changes in frame time, or archiving speed. The real-world effect depends on the workload, CPU/GPU limit, working-set size, and background load.

THREE LEVELS OF MEASUREMENT

SYNTHETIC
AIDA64 / MLC: bandwidth, latency, cache.

APPLICATION BENCHMARK
7-Zip / Cinebench: combined CPU, cache, and memory operation in a specific algorithm.

REAL-WORLD WORKLOAD
Game or project: frame time, 1% low, operation time, and absence of errors.

Metric	What it shows	Main pitfall
Read / Write / Copy	Peak performance of the selected memory and cache path	The result depends on CPU/Ring frequencies, program version, and run conditions
Latency, ns	Synthetic end-to-end latency	Windows background activity, power state, and one lucky run can easily create a false win
Application score	Response of a specific algorithm to the entire platform	Does not let you attribute the entire gain to memory alone
1% low / frametime	Rare slow frames and smoothness in a CPU-limited scene	Different programs calculate percentiles differently; use one methodology and several repeats

RULE FOR A MEANINGFUL BENEFIT

First confirm the change in AIDA64/MLC, then in an application benchmark and a real-world scenario. Five identical runs, their median, and their spread are more reliable than a record score; in an A/B test, alternate profile order to reduce the effects of warm-up and background noise. Calculate P1 FPS as $1000 / P99 \text{ frame time (ms)}$. Do not confuse this with the average FPS of the slowest 1% of frames.

10.6 DAILY, BENCHMARK, AND SCREENSHOT PROFILES

DAILY
Temperature and voltage margin, repeatable cold boot, several tests, and production data.

BENCHMARK
Short-term stability for a specific task. Isolated environment; the result does not transfer to daily use.

SCREENSHOT
POST and an impressive number without proven stability. Demonstrates only a bootable point.

STATE THE PURPOSE OF THE PROFILE

Label the profile honestly: daily, benchmark, or screenshot. Frequency without conditions, temperatures, BIOS version, and tests shows only that the system managed to boot and display those parameters.

HIERARCHY OF EVIDENCE

POST < Screenshot / Validation < Benchmark-stable-for-X < Daily-validated. Do not use the term ‘absolutely stable’ without stating the conditions. Better yet, do not use it at all.

1010.7 FOUR DIMMS AND LARGE CAPACITIES

Four modules, additional ranks, and higher electrical capacitance increase the load on the controller and signal path. Choose the configuration according to the required capacity: maximum frequency is a task for a 2-DIMM / 1SPC motherboard, while a 4-DIMM / 2SPC system requires a more moderate target and an exact QVL match.

Rank is determined by module organization, not by capacity alone. Two kits with the same gigabyte capacity can present different loads, so check the part number, rank count, and actual configuration of each DIMM.

Configuration	Priority	Practical conclusion
2 DIMM / 1DPC / 1R	Frequency and stability margin	Lowest load; best baseline for high-frequency overclocking
2 DIMM / 1DPC / 2R	Capacity without a second branch	More ranks may mean a lower frequency, but there is still only one DIMM per channel
4 DIMM / 2DPC / 1R	Capacity and availability	A second module per channel reduces electrical margin; two-DIMM XMP guarantees nothing
4 DIMM / 2DPC / 2R	Maximum capacity	Heaviest load; begin at JEDEC and raise the frequency gradually
CUDIMM	Clean CK clock signal	CKD restores CK, but does not train DQ/DQS or eliminate the load of four modules

OFFICIAL RATINGS FOR MSI Z790 GODLIKE MAX

For the MEG Z790 GODLIKE MAX, MSI lists up to 7800+ for 1DPC1R, 6800+ for 1DPC2R, 6400+ for 2DPC1R, and 6000+ for 2DPC2R. These figures apply to one motherboard, but clearly show the stated ceiling dropping as load increases.

LARGE-CAPACITY TUNING SEQUENCE

1. CHOOSE THE CAPACITY IN ADVANCE

Do not buy a second random kit later: even the same part number may receive a different IC revision.

2. CHECK THE QVL

Match the exact part number, module count, capacity, BIOS, and recommended slots.

3. START AT JEDEC

Verify that every channel and module works before enabling XMP or manual voltages.

4. LOWER THE DATA RATE BEFORE ADJUSTING VOLTAGE

If XMP is not repeatable, lower the frequency by one or two steps, then find the minimum voltages.

5. TUNE TIMINGS AFTER FREQUENCY

First stabilize training and booting, then tighten the timings in small groups.

6. VALIDATE EVERY MODE

Several cold boots and warm restarts, a hot memory test, and a normal workload.

CAPACITY FIRST, RECORDS SECOND

For a workstation, a stable 128–192 GB at a moderate speed is more valuable than an impressive POST. If maximum MT/s is the goal, choose a 2-DIMM / 1SPC motherboard and two suitably organized modules in advance.

1010.8 RECORDS FOR REPRODUCING A CONFIGURATION

To reproduce a profile, save its settings, test conditions and results. The materials must make it possible to reconstruct the test bench a month later and understand changes after a BIOS update, remount, or module replacement.

Material	What must be visible	Why
Platform record	CPU-Z CPU/Mainboard, BIOS, microcode, and Windows version	Distinguishes the profile from another firmware version and CPU sample
Memory + SPD	Frequency, Gear, primary timings, and every occupied SPD slot	Confirms the active mode and exact modules
Complete timings	ASRock Timing Configurator or MemTweakIt after boot	Shows the runtime values actually applied.
Sensors	HWiNFO Current/Minimum/Maximum: DIMM, VDD/VDDQ telemetry, CPU/Ring, WHEA	Records conditions, temperature, and logged WHEA events.
BIOS profile	File on USB plus screenshots of every changed page	The file may be incompatible with another version; screenshots remain readable
Tests and booting	Version, config, duration, result, cold/warm boot	Lets others repeat the test instead of merely trusting the word 'stable'

THE FOLDER NAME IS ALSO PART OF THE PROTOCOL

Example: 2026-09-03_8200_C36_BIOS2202_DAILY. Inside: BIOS, CPU-Z, SPD, timing tool, HWiNFO, test logs, and a short README with room temperature, airflow, and the latest change.

10.9 SOURCES, LIMITS OF EVIDENCE, AND CHANGE LOG

Level	Basis	How we use it
A	Datasheet, Intel/JEDEC, manual, QVL, and release notes	Record what the manufacturer actually stated for the specific version
B	Repeatable A/B test on the described system	Practical conclusion with conditions, multiple runs, and original logs
C	Several independent community results	A starting point for a hypothesis; not a universal rule or substitute for your own testing
D	Single screenshot or retelling	Only a reason to investigate; without the platform and methodology, it is not used as evidence

MINIMUM ENTRY IN THE REVISION LOG

- Date, document revision number, and changed section.
- Previous claim, new claim, and reason for the change.
- Primary source or link to a reproducible test.
- Platform, BIOS, DIMM capacity/rank, and test conditions.
- Whether previously published profiles must be retested.

REPRODUCIBILITY MATTERS MORE THAN A PERFECT SCREENSHOT

If a result cannot be reproduced from the saved conditions, it remains an observation. Good revisions honestly distinguish specifications, my experience, conclusions from testing, and unconfirmed hypotheses.

11 FORMULAS

DDR5/BL16 without CRC. Examples: 8200 MT/s, CL36/CWL34. Values are in cycles; overclocking guidelines.

PRIMARY TIMINGS

$t_{CWL} = t_{CL} - 2 = 34$; $t_{CL, ns} = t_{CL} \times 2000 / MT/s \approx 8.78 ns$.
 $t_{RAS} = t_{RCD(RD)} + t_{RTP}$ - guideline for an early read; $t_{RC} = t_{RAS} + t_{RP}$.

SECONDARY TIMINGS

$t_{WR} = 48$ - the overclocking standard used in this manual; do not reduce it further.
 $t_{RTP} = 12$; do not go lower: this is the minimum MR6 code. At high data rates, stability may require $t_{RTP} = 14$.
 $t_{FAW, 1 KB (x8)}: 4 \times t_{RRD_S} = 4 \times 8 = 32$.
 $t_{FAW, 2 KB (x16)}: \text{the greater of } 4 \times t_{RRD_S} \text{ and } 40 = 40$ with RRD_S8 .
 $t_{RFCpb} \approx t_{RFC} - 30 \times MT/s / 2000$: at 8200, $688 - 123 = 565$. Hynix/FGR estimate, where t_{RFC} means t_{RFC2} ; do not calculate this from t_{RFC1} . $t_{RFC, cycles} = t_{RFC, ns} \times MT/s / 2000$; round up. I leave t_{RFCpb} on Auto and do not tune it manually.

TERTIARY TIMINGS: BASE CALCULATION AND UTILITY READOUTS

Parameter	DDR5 calculation*	Old DDR4-burst calculation
t_{WTR_L}	$= t_{WRRD_sg} - t_{CWL} - 10$	$= t_{WRRD_sg} - t_{CWL} - 6$
t_{WTR_S}	$= t_{WRRD_dg} - t_{CWL} - 10$	$= t_{WRRD_dg} - t_{CWL} - 6$
t_{WR}	$= t_{WRPRE} - t_{CWL} - 8$	$= t_{WRPRE} - t_{CWL} - 4$

The old calculation reads **4 higher**: $CWL34/WRRD_dg52 \rightarrow 8$ versus **12**. Historically, ASRock had the WTR error and MemTweakIt the WR error; version-dependent. Details: 3.7.
*Read CWL from the controller. Corrections: **WR +1** with 2N, **WTR -1** with a long write-signal ending. $S \leftrightarrow dg, L \leftrightarrow sg$; WTR is linked to WRRD, not RDWR.
In reverse: $t_{WRRD} = t_{CWL} + 10 + t_{WTR}^*$. With the same settings, $WRRD +1 \rightarrow WTR +1$.
 $t_{RDRD_dg} = t_{WRWR_dg} = 8$ - for DDR5/BL16, always leave these at **8** in the profile.
 $t_{WRWR_sg} = 16$ - the lowest effective value in my tests; lowering it further changes nothing. **My own research.**

ADDITIONAL TIMINGS: POWER AND REFRESH

$t_{RDPDEN} = t_{MRPDEN} = t_{CL} + 8 + 1 = 45$.
 $t_{WRPDEN} = t_{WRAPDEN} = t_{CWL} + 8 + t_{WR} + 1 = 34 + 8 + 48 + 1 = 91$.
 $t_{ACTPDEN} = t_{PRPDEN} = t_{REFPDEN} = 2$; $t_{MRWPDEN} = t_{MRD}$.
 $t_{XS} = t_{RFC1}$; $t_{XS_DLL} = t_{DLLK}$ for standard DDR5. Leave these parameters on Auto.
 $t_{CKE} = 8$. With $PD = 0$ (Power Down Disabled), t_{CKE}/t_{XP} and PD-entry delays do not affect this transition; they can stay on Auto.
 $t_{XP} = 8$ is only the cycle limit; $PD = 1$ also requires 7.5 ns: at 8200, at least **31**. Sleep and self-refresh are separate modes.
 $OREF_RI = \text{Auto}$; **0** removes the idle threshold for refresh, but does not disable refresh. Test any gain.
 $t_{REFI} = \text{interval, } \mu s \times MT/s / 2$; round down. At 8200 and up to 85 °C: normal mode $3.9 \mu s \rightarrow 15\,990$; FGR $1.95 \mu s \rightarrow 7995$. Above 85 °C, halve the intervals.
Steps: 16 383 $\rightarrow$ 32 767 $\rightarrow$ 65 535 $\rightarrow$ 131 071 $\rightarrow$ 262 143. At 8200: **4.00 $\rightarrow$ 7.99 $\rightarrow$ 15.98 $\rightarrow$ 31.97 $\rightarrow$ 63.94 μs .** Field increment: 1; maximum **$2^{18} - 1$ (262 143)**. Use the maximum with active airflow or water cooling on the memory; stability depends strongly on temperature. Test with fully warmed memory.

RTL: ANTA777'S EMPIRICAL GUIDELINE

$RTL \approx MT/s / 800 + t_{CL} + 19 = 8200 / 800 + 36 + 19 = 65.25$. Training guideline, not ready-to-use values for the entire RTL group.

12

12.1 STANDARDS, PLATFORM, AND CONTROLLER

Basic names for the standard and platform. The English expansion is retained as the original name; the explanation column describes the term’s role in DDR5 tuning.

Term	English name	Explanation
DDR5	Fifth-Generation Double Data Rate Synchronous Dynamic Random-Access Memory	The fifth generation of synchronous dynamic memory with data transfers on both clock edges.
SDRAM	Synchronous Dynamic Random-Access Memory	Dynamic memory whose operation is synchronized to a clock signal.
DRAM	Dynamic Random-Access Memory	Volatile memory: data is stored as charge in cell capacitors. Periodic refresh is required to retain data.
JEDEC	Joint Electron Device Engineering Council	The organization that publishes DDR5 and SPD standards and timing requirements.
JESD79-5	JEDEC Standard 79-5: DDR5 SDRAM	The primary DDR5 device standard; its letter and version number identify the revision.
MT/s	Megatransfers per Second	Millions of transfers per second; the correct unit for effective DDR data rate.
MHz	Megahertz	Millions of clock cycles per second; for DDR, MT/s is approximately twice the physical fCK.
fCK	Clock Frequency	Physical frequency of the memory clock signal.
QCLK	Memory Controller Clock	Intel controller clock domain. For a confirmed Gear G mode: $tQCLK = G \times 2000 / MT/s, ns$. Check utility readout units separately. See 5.7.
CPU	Central Processing Unit	Central processing unit; on LGA1700/LGA1851, it contains the memory controller.
Ring	Ring Interconnect	Ring interconnect linking cores, cache, and other CPU blocks on the LGA1700 platforms covered here; it is not the IMC itself.
IMC	Integrated Memory Controller	Controller integrated into the CPU: accepts requests, schedules DRAM commands, and services memory channels.
MC	Memory Controller	Intel memory-controller block; MC0/MC1 are its indices. The MC/C labels in ATC are explained in 5.7. MC is also part of the MC/VDD2 BIOS name.
Intel ME	Intel Management Engine	Intel platform-management subsystem with its own firmware; ME in a BIOS/ME label refers to it.
MRC	Memory Reference Code	Intel code inside the BIOS that initializes the IMC/PHY at startup and manages training.
FSP	Firmware Support Package	Intel package for platform initialization. Public FSP fields specify settings but do not expose the entire MRC algorithm.
PHY	Physical Layer	Physical interface layer: signal transmitters, receivers, delays, and calibrations.
BIOS	Basic Input/Output System	The familiar name for motherboard firmware and its settings menu; technically, a modern implementation is generally UEFI.
UEFI	Unified Extensible Firmware Interface	Modern firmware interface; also the environment from which MemTest86 runs.
POST	Power-On Self-Test	Initial self-test after power-on; a successful POST still does not prove stability.
POR	Plan of Record	An Intel-supported operating mode for a specific number of DIMMs, ranks, and data rate.
SKU	Stock Keeping Unit	Inventory identifier for a product. One SKU does not guarantee the same DRAM ICs across every batch; check the hardware revision separately.
Microcode	Processor Microcode	Low-level code controlling some CPU operations. Updates can be loaded by BIOS/UEFI or the operating system and can change processor behavior.
LGA	Land Grid Array	Type of CPU interface with contacts in the socket: LGA1700 and LGA1851.
PCH	Platform Controller Hub	Platform chipset that handles peripherals; it is not the IMC itself.
QVL	Qualified Vendors List	List of memory kits tested by the motherboard manufacturer in the stated configurations.
OC	Overclocking	Operation above the stock conditions of a specific component combination; XMP is also overclocking.

RTL/IOL ANALYSIS AND CALCULATION EXAMPLES — SECTION 5.7

12

12.2 MODULE, ORGANIZATION, AND TOPOLOGY

Module formats, support ICs, and DRAM construction. Rank organization, package placement, and topology are covered on the next page.

Term	English name	Explanation
DIMM	Dual In-line Memory Module	Full-size memory module with independent contacts on both sides of the PCB.
UDIMM	Unbuffered Dual In-line Memory Module	Ordinary unbuffered desktop module; commands reach DRAM without a register buffer.
SO-DIMM	Small Outline DIMM	Compact memory module for laptops and small systems; a standard DDR5 SO-DIMM has 262 contacts.
RDIMM	Registered DIMM	Module with a register that buffers commands, addresses, and the clock signal; used on compatible server platforms.
CUDIMM	Clocked Unbuffered Dual In-line Memory Module	UDIMM with a separate CKD driver that restores the clock signal.
CKD	Clock Driver	The IC on a CUDIMM that receives and reshapes CK; it does not train DQ/DQS lines.
RCD	Registering Clock Driver	RDIMM register buffer between the controller and DRAM for commands, addresses, and CK; it is not a DRAM device.
PMIC	Power Management Integrated Circuit	On-module controller generating VDD, VDDQ and VPP. Voltage range and control depend on the device model and configuration.
SPD	Serial Presence Detect	Module data set: organization, JEDEC profiles, XMP, and service information.
SPD Hub	Serial Presence Detect Hub	DDR5 IC that consolidates access to SPD, PMIC, and a temperature sensor.
EEPROM	Electrically Erasable Programmable Read-Only Memory	Rewritable nonvolatile memory in which SPD is stored.
XMP	Extreme Memory Profile	Enhanced Intel profile with frequency, timings, and voltages above the JEDEC baseline.
EXPO	Extended Profiles for Overclocking	AMD memory-overclocking profile for a compatible platform. Profile support and operation of a particular kit depend on the CPU, motherboard, and BIOS.
PCB	Printed Circuit Board	The printed circuit board of a module or motherboard; its routing affects the signal.
IC	Integrated Circuit	Integrated circuit. In a module description, it often means the complete packaged device; the term itself does not define the number of dies in the package.
Chip	Chip / Microchip	Colloquial name for a die or a complete DRAM device. When counting, clarify whether packages or dies are meant.
Package	IC Package	Structure around the die: substrate, protective encapsulation, and external contacts. Each separate component is counted when counting packages.
Substrate	Package Substrate	Small board inside a package: carries the die and connects it to the external contacts. Distinct from the module PCB.
FBGA	Fine-Pitch Ball Grid Array	Package with a fine-pitch array of solder balls underneath; the package designation does not specify die or rank count.
Die	Semiconductor Die	Piece of silicon on which the DRAM circuitry is fabricated: memory cells and control circuits.
Density	DRAM Die Density	Capacity of one die in Gbit; it determines many refresh requirements.
SDP / DDP	Single-Die Package / Dual-Die Package	One or two dies in one package. Die count alone does not determine rank count; organization and die selection matter.
MMR	Hynix MMR (Device Designation)	Hynix designation from the RAMGuide example: two 4 Gbit MFR dies (a DRAM revision) in a DDP package. This is not a separate rank type.
Low-loss	Low-Loss PCB Material	PCB material with low signal loss. This is a material property, not a guarantee of a particular memory data rate.
Back-drilling	Back Drilling	Removal of unused plated via stubs to reduce signal reflections.

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12.2 MODULE, ORGANIZATION, AND TOPOLOGY

Package construction, rank organization, and PCB sides describe different properties. Next come DRAM width, channels, and slot routing.

Term	English name	Explanation
RDL	Redistribution Layer	Layer that redistributes die contact pads. In the DRAM packages discussed here, moving pads toward the edges facilitates wire bonding.
Monolithic DDR5	Monolithic DDR5 SDRAM	DDR5 devices with one DRAM die per package, without a 3DS stack. This describes the device, not the number of chips or ranks on the DIMM.
3DS / TSV	3D-Stacked DRAM / Through-Silicon Via	3DS is a stack of DRAM dies linked vertically by through-silicon vias (TSVs). Do not equate every DDP package with 3DS.
SS / DS	Single-Sided / Double-Sided	DRAM packages are soldered on one or both sides of the PCB. The number of sides does not determine rank count.
Rank	Memory Rank	Group of DRAM devices selected together by Chip Select; in DDR5, selection occurs by subchannel. Rank does not define the PCB side.
1R / 2R; R0 / R1	Single / Dual Rank; Rank 0 / Rank 1	One or two ranks on a module. R0 and R1 are rank numbers; 1R has R0, while 2R has R0 and R1.
x4 / x8 / x16	DRAM Device Data Width	DRAM data width: 4, 8, or 16 bits; by itself, it does not determine package or rank count.
1Rx4 / 1Rx8 / 2Rx8	Rank Count and Device Width	Notation for rank count and DRAM width: for example, 1Rx4 is one rank built from x4 devices.
Matched Kit	Factory-Matched Memory Kit	A kit tested by the manufacturer in precisely the stated composition.
Speed Bin	Speed Grade / Component Binning	Operating-class designation and the result of IC selection; an XMP bin is not the ultimate potential.
Non-binary DDR5	Non-Binary-Density DDR5	DDR5 with a die density that is not a power of two; for example, 24 Gbit with typical module capacities of 24 and 48 GB.
Channel	Memory Channel	Independent logical path between the IMC and memory.
Subchannel	Independent Memory Subchannel	One of two independent paths on a DDR5 DIMM: 32 data bits, or 40 bits with system ECC. These are not two CPU channels.
DPC / 1DPC / 2DPC	DIMMs Per Channel / One or Two DIMMs Per Channel	Number of modules actually installed per channel; a key measure of the current electrical load.
SPC / 1SPC / 2SPC	Slots Per Channel / One or Two Slots Per Channel	Number of slots physically routed per channel; this is a motherboard property, not the current DIMM installation.
true-1DPC	Community/Vendor Shorthand for True One-Slot-Per-Channel Topology	Common but terminologically imprecise name for a 1SPC motherboard; this manual uses SPC for routing.
2-DIMM / 4-DIMM	Two / Four DIMM Slots	Motherboard slot count; 2-DIMM models are generally optimized for memory overclocking.
Point-to-point	Point-to-point Memory Topology	A connection from the controller to the only DIMM slot on each channel. At the slot level, this routing corresponds to 1SPC.
Daisy Chain	Daisy-Chain Memory Topology	Daisy-chain routing of channel slots, generally preferred with one DIMM per channel.
T-topology	T-Topology Memory Routing	Branched routing with similar lengths to two slots, intended for 2SPC.
Gear	Memory Controller Gear Ratio	Ratio of MC frequency to the physical DRAM clock: Gear 2 = 1:2; Gear 4 = 1:4. Gear 2 is generally used with DDR5 on Raptor Lake.
OEM / reference	Original Equipment Manufacturer / Reference Module	In the catalog, desktop modules and reference entries; a supply category, not an IC type, rank count, or indication of ECC.
P/N / SKU	Part Number / Stock Keeping Unit	P/N is the manufacturer part number; SKU identifies a stock item. For a kit, keep the full code and suffix to distinguish capacity, profile and variant.
BOM	Bill of Materials	List of components making up a product. The manufacturer may change it between batches while retaining the product SKU.
DRAM revision	DRAM Die Revision	Die revision, not PCB revision or speed grade. S32M means Samsung DDR5, 32 Gbit, M-die.
Native JEDEC	Native JEDEC Speed Grade	Stock speed grade without XMP/EXPO. A component bin alone does not establish the SPD profile or rated operating mode of a finished module.

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12.3 COMMANDS, BUSES, AND SIGNAL PATHS

DDR5 commands operate on banks, rows, and columns. Bus abbreviations show the physical path over which a command, address, or payload is transferred.

Term	English name	Explanation
Bank	Memory Bank	Independent array of rows and columns within DRAM.
Bank Group	Bank Group	Group of banks; transitions within one bank group and between different bank groups have different timings.
Row	Memory Row	Row of cells opened into the row buffer by an ACT command.
Column	Memory Column	Part of an open row accessed by read or write commands.
ACT	Activate	Opens the selected bank row before data access.
PRE	Precharge	Closes an open row and prepares the bank for the next activation.
PREab	Precharge All Banks	Closes open rows in every bank of the selected rank.
PREpb / PREsb	Precharge Per Bank / Same Bank	PREpb closes the selected bank; PREsb closes the bank with the same number in every bank group of the selected logical rank.
RD	Read Command	Command that reads data from an open row.
WR	Write Command	Command that writes data to an open row.
CAS	Column Address Strobe	Historical name for the column phase; appears in the names of CL and CAS-to-CAS timings.
RAS	Row Address Strobe	Historical name for the row phase; used in the names of ACT/PRE timings.
DQ	Data Input/Output	Bidirectional payload data lines between the IMC and DRAM.
DQS	Data Strobe	Data strobe used by the receiver to capture DQ bits.
CA	Command and Address	Command and address bus from the controller to the module.
CK	Clock	Primary differential memory clock signal.
CS / CS0 / CS1	Chip Select / Chip Select 0 / 1	Rank selection: CS0 corresponds to R0, and CS1 to R1. In DDR5, the select signals are independent for each subchannel.
CKE	Clock Enable (Legacy/Controller Term)	Historical and controller-side mode name; DDR5 has no separate CKE pin.
CMD / CTL	Command / Control	General labels for command and control signals.
MR / MRW / MRR	Mode Register / Mode Register Write / Read	DRAM mode register and its write/read commands. MRs configure modes and provide device-defined information; they are not SPD.
WCK	Write Clock	Separate high-speed LPDDR5 data clock; do not confuse it with CK on desktop DDR5.
BL16	Burst Length 16	A burst of 16 data transfers; the baseline burst length for DDR5.
BC8	Burst Chop 8	Shortened transfer of half a BL16 for a supported scenario.
Bus	Electrical Bus	A set of signal lines used to carry data, addresses, commands, or clock signals.
Turnaround	Bus Turnaround	Reversal of bus direction or change of bus target requiring a guard interval.
RMW	Read-Modify-Write	Read a block, modify part of it, and then write it back.

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12.4 PRIMARY, SECONDARY, AND TERTIARY TIMINGS

The letter t means time. Main BIOS timing fields are usually in CK cycles; maintenance fields may use other units. The same CK count at different MT/s represents a different time in nanoseconds.

Term	English name	Explanation
Timing	Memory Timing	Memory timing parameter: latency, duration, or interval between events.
tCK	Clock Period	Duration of one physical clock cycle: tCK, ns = $2000 / MT/s$.
tCL	CAS Latency	Latency from the READ command until the first data appears.
tRCDRD	Row-to-Column Delay for Read	Interval from ACT to the subsequent READ command.
tRCDWR	Row-to-Column Delay for Write	Interval from ACT to the subsequent WRITE command.
tRP	Row Precharge Time	Time required to close a row before opening another row in that bank.
tRAS	Row Active Time	Minimum time for which a row remains open.
tRC	Row Cycle Time	Here, tRC = tRAS + tRP is a calculation. The actual ACT-to-ACT interval for the same bank can be longer because of the last READ/WRITE. See 3.3.
CR / 1N / 2N	Command Rate / One-N / Two-N	Command issue rate: every clock cycle or every other clock cycle.
tCWL	CAS Write Latency	Latency from WRITE to the start of data transfer.
tWR	Write Recovery Time	Minimum interval from the end of a write data burst to PRE for the same bank.
tRTP	Read-to-Precharge Time	Minimum interval from a READ command to PRE for the same bank.
tRRD_S / L	Row-to-Row Delay Short / Long	Interval between ACT commands: S for different bank groups, L for the same bank group.
tFAW	Four Activate Window	Minimum interval from the first to the fifth ACT in one rank; the window restarts with each new ACT.
tCCD_S / L	CAS-to-CAS Delay Short / Long	Interval between column commands: S for different bank groups, L for the same bank group.
tCCD_L_WR	Long CAS-to-CAS Write Delay	WR -> WR interval within one bank group when the second WRITE requires Read-Modify-Write.
tCCD_L_WR2	Long CAS-to-CAS Write Delay 2	Shortened WR -> WR interval within one bank group when the second WRITE does not require Read-Modify-Write.
tWTR_S / L	Write-to-Read Delay Short / Long	Interval from the end of a write data burst to READ: S for a different bank group, L for the same one.
tRDRD	Read-to-Read Delay	Family of tertiary transitions between two reads.
tWRWR	Write-to-Write Delay	Family of tertiary transitions between two writes.
tRDWR	Read-to-Write Delay	Bus turnaround from read to write.
tWRRD	Write-to-Read Delay	Bus turnaround from write to read.
S / L	Short / Long	Short and long timing variants. Their exact meaning depends on the timing family; they do not describe trace length.
sg / dg	Same Group / Different Group	Same or different bank group.
dr / dd	Different Rank / Different DIMM	Different rank or different module.

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12.5 REFRESH AND MAINTENANCE INTERVALS

Refresh restores cell charge. Higher tREFI means less frequent refresh; lower tRFC means shorter refresh pauses. Both reduce overhead but increase sensitivity to temperature and the retention capability of the specific ICs.

Term	English name	Explanation
Refresh	DRAM Refresh	Periodic restoration of charge in memory cells.
Retention	Data Retention	A cell's ability to retain data between refresh operations.
REFab	All-Bank Refresh	Refresh of all banks in the selected rank.
REFsb	Same-Bank Refresh	Refresh of the same-numbered bank in every bank group.
PBR	Per-Bank Refresh	Generic name for partial refresh. In Intel BIOS, Per Bank may refer to REFsb; it does not necessarily mean refreshing just one bank.
FGR	Fine Granularity Refresh	More frequent refresh with a shortened service cycle.
tREFI	Refresh Interval Time	Average interval between refreshes; increasing it reduces overhead and temperature margin.
tRFC	Refresh Cycle Time	Practical designation for the refresh-cycle duration actually applied by BIOS/MRC; converted to nanoseconds at the current data rate.
tRFC1 / tRFC2	Refresh Cycle Time 1 / 2	Requirements for normal REFab and REFab in 2x FGR mode, respectively; these are different standard modes, not two mandatory practical BIOS fields.
tRFCsb / tRFCpb	Same-Bank / Per-Bank Refresh Cycle Time	Platform-dependent names for a separate refresh path. In practice, tuned after tRFC.
tREFIx9	Maximum Refresh Interval	Refresh limit for one rank, in 1024 DCLK. Calculating $8 \times tREFI / 1024$ can exceed the field range. The result depends on the controller/MRC. Leave Auto.
Power Down	DRAM Power-Down State	Memory power-saving state while idle.
Self Refresh	Self-Refresh Mode	Mode in which DRAM performs refresh by itself.
tCKE	Clock-Enable Timing	Internal interval for entering and exiting Power Down.
tXP	Exit Power-Down Time	Delay from exiting Power Down until the next command.
tXS	Exit Self-Refresh Time	Delay when exiting Self Refresh.
tXS_DLL / tDLLK	Exit Self-Refresh DLL / DLL Locking Time	After Self Refresh, commands requiring the DLL must wait for it to be ready: tXS_DLL = tDLLK. This is a separate requirement from tXS.
tRDPDEN	Read-to-Power-Down Entry Delay	Interval from READ to entry into Power Down.
tWRPDEN	Write-to-Power-Down Entry Delay	Interval from WRITE to entry into Power Down.
tMRD / tMOD	Mode-Register Delay / Update Delay	Intervals between internal commands and application of a mode register.
tMRR	Mode Register Read Command Period	Minimum period between Mode Register Read (MRR) commands. Do not confuse the tMRR timing parameter with the MRR command itself.
ZQ Calibration	Impedance Calibration against ZQ	Calibration of DRAM output resistances against the ZQ reference.
tZQSPeriod	ZQ Calibration Short Period	Interval at which short ZQ calibration is performed.
tZQOPER	ZQ Calibration Operation Time	Duration of a full ZQ-calibration operation.
RFM	Refresh Management	Mechanism for additional refresh under frequent activations; not a replacement for tRFC.
tRFM	Refresh Management Cycle Time	Minimum RFM-cycle duration; this is a timing parameter, not the RFM mechanism itself.
tRPab	All-Bank Precharge Time	Interval after PREab. Check the controller-specific scope of the field; do not automatically substitute the tRP setting.
tCA2CS	Command/Address-to-Chip-Select Delay	Internal interval between the CA path and CS selection.
Vendor fields	Controller/Vendor-Specific Timing Fields	Labels such as tSR, tOSCO, and tXPDLL are not expanded by guesswork and remain on Auto unless a specific task calls for them.

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12.6 VOLTAGES AND POWER DOMAINS

Identical VDDQ letters in different menus do not mean the same physical rail. Record the name, measurement source, and platform together.

Term	English name	Explanation
Rail	Power Rail	A separate power rail with its own physical role.
DRAM VDD	DRAM Core Supply Voltage	Power for the array and internal peripheral circuits of DRAM devices.
DRAM VDDQ	DRAM I/O Supply Voltage	Power for the data interface on the module side.
CPU VDDQ TX	CPU Transmit I/O Supply Voltage	Power for the memory transmitter inside the CPU; not the same as DRAM VDDQ.
MC VDD / VDD2	Memory-Controller I/O Supply Voltage	Platform-specific names for the IMC interface rail, not two independent regulators.
SA / VCCSA	System Agent Supply Voltage	Power for the Intel System Agent; not a universal memory-frequency knob.
VPP	DRAM Wordline Pump Supply Voltage	Power for row activation, nominally about 1.8 V.
VDDIO	Input/Output Supply Voltage	Generic designation for the I/O power of a specific block.
VLDO	Low-Dropout-Regulator Output Voltage	Output of a local linear regulator, for example inside the SPD Hub.
LDO	Low-Dropout Regulator	Linear regulator with a low dropout voltage.
IVR	Integrated Voltage Regulator	Integrated CPU voltage regulator.
PMIC Sync All	Synchronize All PMICs	Applies the same control to the PMICs of all installed DIMMs.
Per-PMIC	Per-Power-Management-IC Control	Separate PMIC configuration for each module.
High DRAM Voltage	Extended DRAM-Voltage Range Mode	Extended VDD/VDDQ range on compatible PMICs; does not set voltage.
VOUT	Voltage Output	Regulator output voltage; in monitoring, its telemetry reading.
VID	Voltage Identification	Requested voltage, which does not have to match VOUT under load.
SVID	Serial Voltage Identification	Intel digital interface for power control and telemetry.
LLC	Load-Line Calibration	Compensation for voltage droop under current load; aggressive LLC may cause overshoot.
PLL	Phase-Locked Loop	Loop that synchronizes and recovers frequency and phase.
DLL	Delay-Locked Loop	Loop that aligns delays without synthesizing a new frequency.
TDDB	Time-Dependent Dielectric Breakdown	Time-dependent dielectric breakdown: insulation damage from prolonged electrical stress.
ppm	Parts Per Million	One millionth; 1 ppm = 1 in 1,000,000. In the TI chart, this is the calculated failure fraction.
TCASE	DRAM Package Case Temperature	DRAM package case temperature at the specified measurement point. The SPD Hub sensor reading is not a direct TCASE measurement.
VRM	Voltage Regulator Module	Power circuitry for the CPU or another rail. Phase count and power-stage ratings alone do not determine memory overclocking.
PWM	Pulse-Width Modulation	A PWM controller regulates the power converter by controlling the switching pulses sent to its phases.
SPS	Smart Power Stage	Integrated power stage with a driver and protection functions. Its current rating is not the current capability of the whole board.
PMIC5120	JEDEC PMIC5120	JEDEC PMIC class for client DDR5; Renesas RRG5332 is one example. The class does not identify a silicon revision.

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12.7 TERMINATION AND SIGNAL INTEGRITY

ODT, driver resistance, and Vref define the electrical receive window. Their goal is not the lowest number, but a clean signal with margin in every bus state.

Term	English name	Explanation
ODT	On-Die Termination	Line termination using resistors integrated into the die. Active termination depends on transfer direction and rank state.
RTT	Termination Resistance	Generic designation for ODT resistance; not a separate technology.
RTT_NOM	Nominal Termination Resistance	Nominal termination for the selected DRAM state.
RTT_WR	Write Termination Resistance	DRAM termination during writes.
RTT_PARK	Park Termination Resistance	Termination of an inactive, parked rank.
RON	Driver On-Resistance	Output resistance of the active transmitter.
PU / PD	Pull-Up / Pull-Down	Upper and lower parts of the driver or termination.
Vref	Reference Voltage	Reference level for distinguishing a logical zero from one.
VrefDQ	Data Reference Voltage	Reference level of the DQ data path.
VrefCA	Command/Address Reference Voltage	Reference level of the CA command/address path.
VrefCS	Chip-Select Reference Voltage	Reference level for receiving CS; distinct from VrefCA and VrefDQ. Adjustable only when the platform provides the corresponding field.
Drive Strength	Transmitter Drive Strength	Output-stage strength; the maximum value is not necessarily optimal.
Power Training	DDR I/O Power Training	MRC stage that selects ODT, driver strength, and related buffers to reduce DDR I/O power while preserving operating margin.
Slew Rate	Signal Slew Rate	Rate of a signal edge's rise and fall.
EQ	Equalization	Compensation for frequency-dependent channel loss and distortion.
CTLE	Continuous-Time Linear Equalizer	Linear receiver equalizer.
DFE	Decision-Feedback Equalization	Distortion correction based on previously received symbols.
DCC	Duty-Cycle Correction	Duty-cycle correction for CK, DQS, DQ and other PHY signals.
DCA	Duty-Cycle Adjuster / Adjustment	DRAM signal duty-cycle tuning.
PVT	Process, Voltage, Temperature	Process, voltage, and temperature variation accounted for by calibrations.
Eye	Signal Eye	Permissible time and voltage ranges for correct signal reception.
Margin	Signal Margin	Margin to the error boundary; not a guarantee of operating-system stability.
Crosstalk	Signal Crosstalk	Electromagnetic coupling between adjacent lines.
Tap	Delay Tap	Discrete increment of a programmable delay line.
Bypass	Bypass Mode	Circuit/path bypass; VccDLL Bypass reroutes power while the DLL remains active.

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12.8 TRAINING, BOOTING, AND RECOVERY

Training selects delays, Vref, and compensation for the current startup. One successful POST may not be repeatable, so both cold and warm boots must be checked.

Term	English name	Explanation
Memory Training	Memory Interface Training	Selection of delays, Vref, ODT, and memory-interface compensation.
Auto	Automatic Firmware-Controlled Value	A BIOS/MRC decision; does not necessarily mean a standard or minimum value.
Trained Value	Value Determined by Training	Actual value found by the current training cycle.
Full Training	Full Memory Training	The complete BIOS/MRC cycle configured for the current system; its stages depend on the platform and settings.
Full Retrain	Full Memory Retraining	Another full training cycle after conditions change.
Cold Training	Training after a Cold Start	Training after power removal; not every cold start guarantees a complete MRC cycle.
1D / 2D	One-/Two-Dimensional Training	A search across one or two tuning parameters.
RDTC2D	Read Timing Centering 2D	Switch for a training stage in Intel FSP and corresponding BIOS implementations. Not a numerical timing; its exact use depends on the firmware.
Per-Bit	Per-Bit Training	Individual calibration of each DQ bit.
MPR	Multi-Purpose Register	In DDR4, a pattern register; DDR5 training patterns use MR settings.
WL	Write Leveling	Alignment of write DQS relative to CK.
RTL	Round-Trip Latency	Intel Alder Lake / Raptor Lake field: READ to first data at the MC, per rank, in QCLK. Utility scaling and conversion to ns require verification. See 5.7.
RTLA / RTLB	Round-Trip Latency A / B	A/B-side designations in the empirical formula; they do not automatically correspond to every MC/C row in ATC. See 5.7.
IOL	I/O Latency	Separate I/O delay in the BIOS of some DDR4 platforms. On DDR5, the parameters and access to them are arranged differently. See 5.7.
RTL Init	Round Trip Latency Initial Value	Initial RTL search setting during training; not a promise of the final RTL.
RTL Max	Round Trip Latency Maximum	Upper bound of the RTL search during training in ASUS BIOS; does not guarantee that final result.
RTL Offset	Round Trip Latency Offset	RTL offset with separate sign and magnitude in ASUS BIOS; behavior depends on the implementation. Not a universal rule to subtract 1–2.
TAT	Turn-Around Timing	Transition intervals between bus directions and targets.
RMT	Rank Margin Tool	Tool for evaluating a rank’s timing and voltage margin.
Cold Boot	Cold Boot / Cold Start	Startup after shutdown; the state of standby power must be specified.
AC Cold Start	Cold Start after AC-Power Removal	Startup after complete removal of external and standby power.
Warm Restart	Warm Boot / Warm Restart	Restart without complete power removal.
S5	ACPI S5 Soft-Off State	Software-initiated operating-system shutdown that may preserve standby power.
MRC Fast Boot	Memory Reference Code Fast Boot	Shortened memory reinitialization path.
BIOS Fast Boot	Firmware Fast Boot	Shortens overall POST; not the same as MRC Fast Boot.
Windows Fast Startup	Operating-System Fast Startup	Hybrid Windows shutdown; not a cold boot.
No-POST	Failure to Complete POST	The system did not complete hardware initialization.
Recovery	Firmware Recovery Procedure	Return to bootable settings after a failed POST.
Clear CMOS	Clear CMOS Settings (CMOS: Complementary Metal-Oxide-Semiconductor)	Reset of saved BIOS settings; CMOS is a historical name here.
DIMM Fit	ASUS DIMM Fit	Automatic search for parameters around an already bootable baseline.
DIMM Fit Pro	ASUS DIMM Fit Pro	Extended ASUS process for selecting and testing memory parameters.
Training Consistency	Memory-Training Consistency	Feature for improving training repeatability, not a stress test.
Memory Preset	Firmware Memory Preset	Manufacturer-prepared set of baseline memory settings.

RTL/IOL ANALYSIS AND CALCULATION EXAMPLES — SECTION 5.7

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12.9 PROFILES, ERRORS, AND STABILITY

Stability always refers to stated conditions. POST, a benchmark pass, one screenshot, and daily reliability are different levels of evidence.

Term	English name	Explanation
Baseline	Baseline Configuration	Recorded starting configuration for a controlled comparison.
Profile	Saved Configuration Profile	Saved set of settings and conditions; by itself, does not prove stability.
Daily	Daily-Validated Profile	Daily profile with validated thermal and electrical margin.
Benchmark profile	Benchmark-Stable Profile	Settings validated only by the stated benchmark.
Screenshot profile	Screenshot-Only Profile	Profile for capturing settings without full validation.
Safe JEDEC	Safe JEDEC Baseline	Backup stock profile for system recovery.
Validation	Configuration Validation	Checking against specified conditions. In CPU-Z/HWBOT, also registration of settings or a result; it does not by itself prove stability.
Stability	Operational Stability	Absence of errors under the listed conditions and scenarios.
Pass	Successful Test Pass	Completed pass without logged errors.
Fail / Error	Test Failure / Detected Error	Test error or failure; the result requires diagnosis and does not count as a pass.
Coverage	Test Coverage Percentage	An internal program metric, not a probability of overall stability.
Cycle	Test Cycle	One complete set of algorithms in a particular test.
A/B Test	Controlled A/B Comparison	Comparison of two variants with one variable changed.
Sweet Spot	Optimal Operating Window	Best balance of results, temperature, voltage, and repeatability.
Hot Stability	Stability at Thermal Equilibrium	Stability after memory and the system reach their thermal plateau.
Thermal Margin	Temperature Margin	Margin to the temperature at which errors appear.
Pre-OS	Pre-Operating-System Environment	Environment before Windows loads, such as UEFI MemTest86.
ECC	Error-Correcting Code	Code for detecting and correcting data errors.
On-die ECC	On-Die Error-Correcting Code	Internal error correction within a DRAM die; does not protect the entire data-transfer path.
ECS	Error Check and Scrub	Checks and corrects stored data using on-die ECC, with the specified counters. Reading them requires platform support; this is not a system ECC report.
Side-band ECC	Side-Band Error-Correcting Code	System-level correction using additional ECC bits; requires a compatible CPU/IMC, motherboard, and ECC DIMM.
Corrected ECC errors	Corrected ECC Error Events	Corrected and logged ECC errors; increases must not be ignored.
ECC injection	Error-Correcting Code Error Injection	Deliberate introduction of an error to verify ECC operation.
WHEA	Windows Hardware Error Architecture	Windows subsystem that logs hardware errors.
DMA	Direct Memory Access	Direct device access to memory without normal CPU data handling.
NUMA	Non-Uniform Memory Access	Architecture in which the cost of accessing different memory regions varies.
CRC	Cyclic Redundancy Check	Checksum used to detect data corruption.
Row disturbance / Row Hammer	Row-Disturbance Bit Flips / Row Hammer	Data errors in victim rows caused by repeated activations of aggressor rows. A particular scenario can involve multiple rows.
PPR	Post-Package Repair	Row repair: Soft PPR is temporary; Hard PPR survives power loss.

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12.10 TOOLS, WORKLOADS, AND METRICS

A stress test searches for errors; a benchmark measures a result.

Term	English name	Explanation
Stress Test	Stress Test	Workload used to find errors, not to achieve a record result.
Component Stress	Component-Specific Stress Test	Algorithm that deliberately loads the CPU, IMC, or RAM.
y-cruncher	y-cruncher Component Stress Tester	Set of computational workloads for the CPU, IMC, and memory.
SVT	Small In-Cache VT3	Small in-cache variant of the VT3 family: primarily tests CPU/cache without a large RAM working set.
VT3	Vector-Scalable Transform, Version 3	Direct replacement for the obsolete VST: heavy floating-point workload with a large CPU + IMC + RAM working set.
FFT	Fast Fourier Transform	Fast Fourier transform; intensive floating-point and memory operation.
NTT	Number-Theoretic Transform	Integer number-theoretic transform.
AVX	Advanced Vector Extensions	Set of wide vector instructions for the CPU.
FPU	Floating-Point Unit	Compute unit for floating-point operations.
TM5	TestMem5	Windows memory-testing engine with pluggable configs.
Karhu	Karhu RAM Test	Test of an allocated amount of RAM in Windows; progress is reported as coverage.
MemTest86	PassMark MemTest86	UEFI memory test run before the operating system starts.
RAM Test Pro	PCSTONKS RAM Test Pro	Windows utility with configurable memory tests, error logging and WHEA monitoring.
OCCT	Historically: OverClock Checking Tool	Suite of platform stress tests and benchmarks; the product’s current name is OCCT.
AIDA64	AIDA64 Cache & Memory Benchmark	Measures Read, Write, Copy, and synthetic latency.
MLC	Memory Latency Checker	Intel tool for measuring latency and bandwidth.
CPU-Z	CPU-Z	Shows the CPU, motherboard, active memory parameters, and SPD.
ATC	ASRock Timing Configurator	Utility for viewing memory timings and RTL; the set of fields depends on the platform and version. See 5.7.
HWINFO	HWINFO	Tool for monitoring sensors, minimums, and maximums.
Benchmark	Performance Benchmark	Performance measurement; not a stability test.
Latency	Access Latency	Time spent waiting for access or a response, generally in nanoseconds.
Bandwidth	Memory Bandwidth	Amount of data transferred per unit of time.
Throughput	Sustained Throughput	Actual stream performance including overhead.
GB/s / ns	Gigabytes per Second / Nanoseconds	Units of bandwidth and latency.
Median / P1 / P99	Median / First / Ninety-Ninth Percentile	Central result and distribution tails; the metric’s direction must be stated.
FPS / 1% Low	Frames per Second / Slowest-One-Percent Frame Metric	Average frame rate and a measure of rare slow frames; the calculation method must be recorded.
Frametime	Frame Time / Frame Interval	Interval between consecutive frames or Present events; the precise meaning depends on the selected metric.
CPU-/GPU-limit	CPU-/GPU-Limited Workload	CPU or GPU limitation that changes how visible the RAM effect is.
Throttling	Thermal/Power Throttling	Automatic frequency reduction due to temperature, current, or a power limit.
Gbit / GB	Gigabit / Gigabyte	Die density in bits and module capacity in bytes are different quantities; 8 bits = 1 byte. Do not confuse Gbit, GB, and binary GiB.

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12.11 ADVANCED TRAINING ALGORITHMS

Terms used in the advanced analysis of memory training.

Term	English name	Explanation
RxVref	Receiver Reference Voltage	The CPU receiver's decision threshold during reads. It is adjusted separately from DRAM VrefDQ, which is used during writes.
DQS gating	DQS Receive Gating	Controls the DQS receive window so that the receiver opens for the expected start of a read transfer.
Deskew	Timing Deskew	Compensation for timing differences between signal lines. Per-bit deskew adjusts the timing of individual DQ bits separately.
FIFO	First In, First Out	A buffer that releases data in the order received. Receive-FIFO delays help align returning data with the memory controller.
PI	Phase Interpolator	A phase interpolator positions a signal edge between available clock phases.
LVR	Linear Voltage Regulator	A linear voltage regulator. In the Intel architecture discussed here, these regulators supply internal memory-PHY circuits.
LFSR	Linear Feedback Shift Register	A shift register with linear feedback that generates pseudorandom bit sequences used in training patterns.
Swizzle	DQ/DQS Swizzle	The mapping of logical DQ/DQS signals to physical routing, accounting for permitted signal permutations.
Address aliasing	Address Aliasing	Different logical addresses refer to the same physical memory location. An incorrectly described DRAM organization can cause this.
BDAT	BIOS Data ACPI Table	An ACPI table for diagnostic data, including RMT results. Its generation is enabled separately and does not guarantee a visible BIOS report.

13 DOCUMENTATION

List of primary and technical materials used to verify terminology, platform limitations, and the tuning and testing methodology. The strength of evidence depends on the basis for a claim, not on the platform where it appears.

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REVISIONS AND ACCESS DATE

Revision numbers and historical dates are preserved. Current downloads and links were checked on October 15, 2026.

AIDA64 downloads have been updated to 8.40.5000; the Chapter 7 results refer to version 8.35, as stated there.

14 CATALOG OF DDR5 KITS AND DESKTOP MODULES

OPEN AND DOWNLOAD THE CATALOG — EN (PDF)

Separate PDF on pakt.cc

To save the file, open the link and use the download button in the PDF viewer.

The complete catalog of DDR5 kits and desktop memory modules is available as a separate document through the link above. This chapter now provides a single page for accessing the catalog.

WHAT THE CATALOG CONTAINS

- Factory DDR5 memory kits.
- Desktop OEM/reference UDIMM and CUDIMM modules.
- DRAM revision classification, notes, and source links.

THE CATALOG IS UPDATED SEPARATELY

The list of models and part numbers can grow without increasing the size of the practical manual. Consult the separate PDF for the tables and kit specifications.

