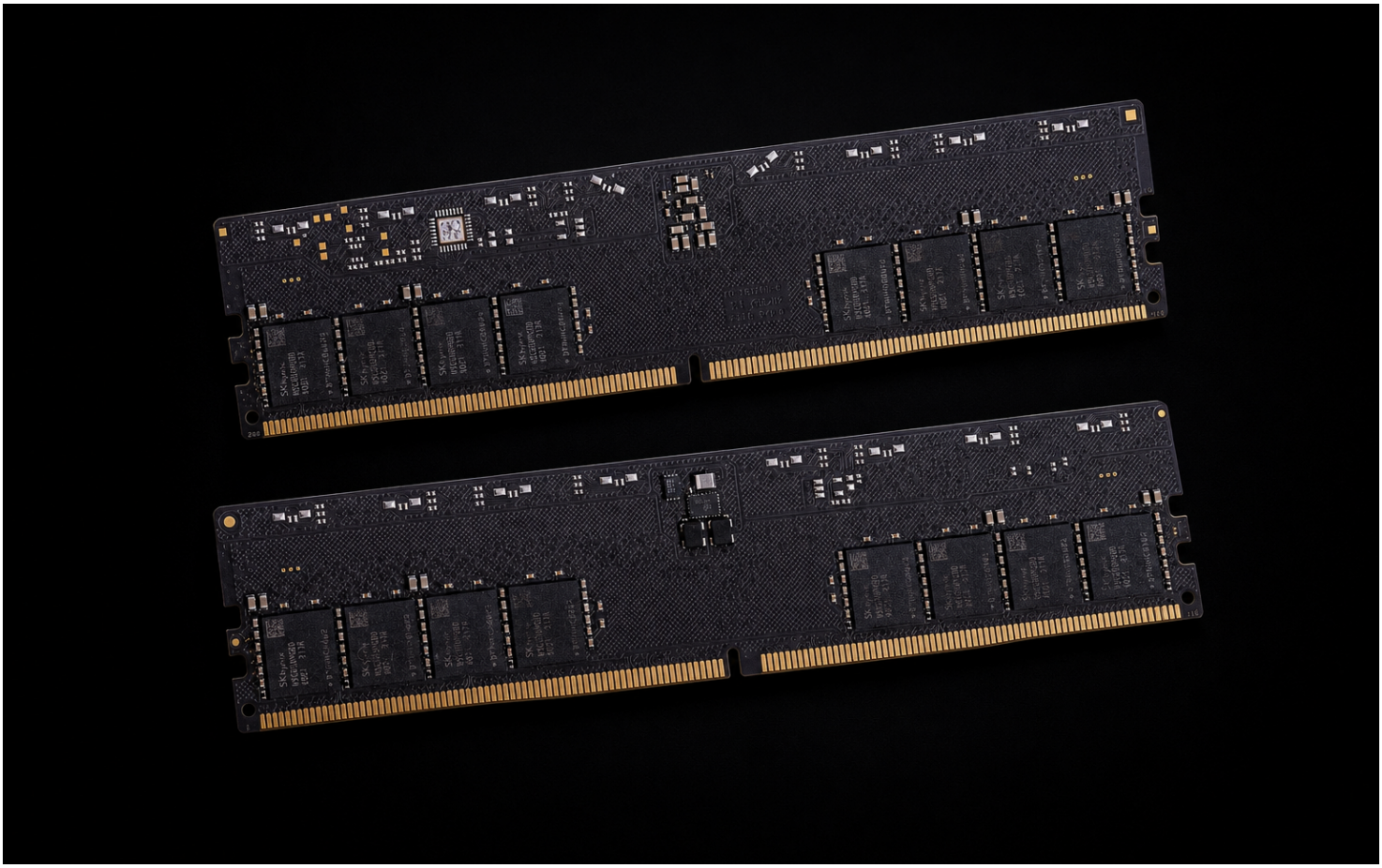
2026



DDR5 MEMORY TUNING AND OPTIMIZATION ON INTEL LGA1700 / LGA1851 PLATFORMS

FUNDAMENTALS / TIMINGS / VOLTAGES / TRAINING / STABILITY

ROG Maximus Z790 Apex (BIOS 3202)
ROG Maximus Z790 Apex Encore (BIOS 2202)
ROG Maximus Z890 Apex (BIOS 3402)

REV 5.03 (30.10.2026)

THE COMPLETE MANUAL FOR DDR5 TUNING AND OPTIMIZATION

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01 / Introduction

1.1 APPROACH AND LIMITS: REQUIRED READING

> Even a deep understanding of interface physics and a degree in electrical engineering do not, by themselves, guarantee reliable results. A comparison requires comparable conditions, control of relevant variables, and allowance for the uncertainty of the measurement method. Oscilloscope measurements through an interposer must account for how the probe and interposer affect the signal; register readouts require knowing what the fields mean, when they were read, and the system state at that time. Even when these conditions are met, overlooked factors or errors in interpretation can affect the validity of the final conclusion.

AT WHAT LEVEL ARE WE INVESTIGATING?

There are five levels at which to investigate memory behavior. Choose the method to suit the question: repeatable tests, technical documentation, BIOS code or signal measurements.

1. Theory	Study how memory works, what its parameters mean, and how they interact, so that we understand what we change and what results to expect.
2. Hands-on testing	Change BIOS settings, repeat POST and tests. Check stability, performance, and temperature.
3. Documentation and parameter readout	Compare specifications, other people's results, and parameters read from the system. Separate the meaning of a field from assumptions about how it works.
4. BIOS/MRC and registers	Examine the code, registers, and logs of a specific firmware version. Establish which memory-training stage ran and what it changed.
5. Physical measurements	Observe signals and timing intervals with an oscilloscope or analyzer. Interface measurements do not reveal every process inside the die.

WHERE I WORK AND WHAT I CAN CLAIM

I work at the first three levels: studying the theory, testing system behavior and examining technical data. I assess individual settings by comparing repeatable results. When no difference is visible, I leave the question open. My contribution is practical verification of recommendations and the organization of technical data. This work has value in its own right.

> **I distinguish verified results from explanations of their causes. When evidence is insufficient, I say so. As new measurements become available, I refine the conclusions and correct errors.**
>
> When overclocking memory, there are no “correct” training results or ODT values that suit every configuration. My recommendations draw on my own experience, the community’s experience, and verified technical documentation. They provide a starting point: the settings need to be selected and tested on your system. Even a small increase in DRAM temperature may affect the outcome of the next training run and the stability margin with the current settings, especially when the system is operating close to its limits.

MY EXAMPLE: READ TIMING CENTERING 2D

In a recent discussion, I examined Read Timing Centering 2D under Training Algorithms. This switch enables or disables a training stage. The ASUS BIOS Manual [1] lists Auto/Disabled/Enabled without explaining the algorithm. The RDTC2D field in Intel FSP for Raptor Lake-S [2] also controls whether the stage runs. These sources explain the field's purpose; its use by a particular BIOS requires separate verification. I prefer Enabled. This option needs to be tested separately for your profile. The Training Algorithms chapter provides a detailed discussion of the settings.

1.2 Who this manual is for and how to use it

You can read this manual from start to finish if you are just getting started, or use it as a reference if you already know the fundamentals. In both cases, the goal is the same: to understand why a setting is changed, how it relates to the other settings, and how to verify the result.

IF YOU ARE TUNING DDR5 FOR THE FIRST TIME

First, distinguish JEDEC from XMP and understand how capacity, rank, and topology affect frequency. Then establish a known-good baseline. Do not start with a full set of someone else's values: if something goes wrong, it will be difficult to find the cause. The links below provide a short tuning path.

IF YOU ALREADY HAVE EXPERIENCE

The manual can be used as a reference. Go directly to the relevant group of timings, voltages, or training parameters, but consult the fundamentals chapter whenever the platform, memory capacity, or module type changes. For LGA1851 and CUDIMM, use the relevant sections: the IMC, CKD and training differ from Z790.

HOW TO APPROACH TUNING

1. SAVE THE BASELINE

First test JEDEC/Auto, then test XMP separately. Record the BIOS version, actual frequency, voltages, and trained values.

2. CHANGE ONE THING AT A TIME

In each iteration, change one parameter or one predefined group of parameters. Even related voltages should initially be adjusted one at a time; change them together only once the role of each is understood.

3. REPEAT MEMORY TRAINING

After significant changes, check not only a reboot but also a boot after idle. One successful boot does not yet prove repeatability.

4. USE MULTIPLE TESTS

A combination of tests is needed to check for different types of errors. Your test suite must check the modules themselves, the memory controller, and system behavior in real workloads.

5. LEAVE SOME MARGIN

The daily-use profile should be slightly more conservative than the last identified stability threshold and remain stable at a different temperature and after idle.

WHAT TO RECORD AFTER EACH STEP

For each journal entry, it is enough to record the changed parameter, frequency, main voltages, module temperature, test results, and behavior during boots after idle. A short, clear entry is more useful than a large collection of unexplained screenshots: it lets you quickly identify the last successful point and determine which change introduced the error.

WHEN YOU CAN STOP

A profile can be considered ready when it is repeatable across several boots after idle, passes a suite of different tests, and produces no errors in normal workloads at operating temperature. Running one test indefinitely provides less confidence than several workloads that exercise different parts of the system.

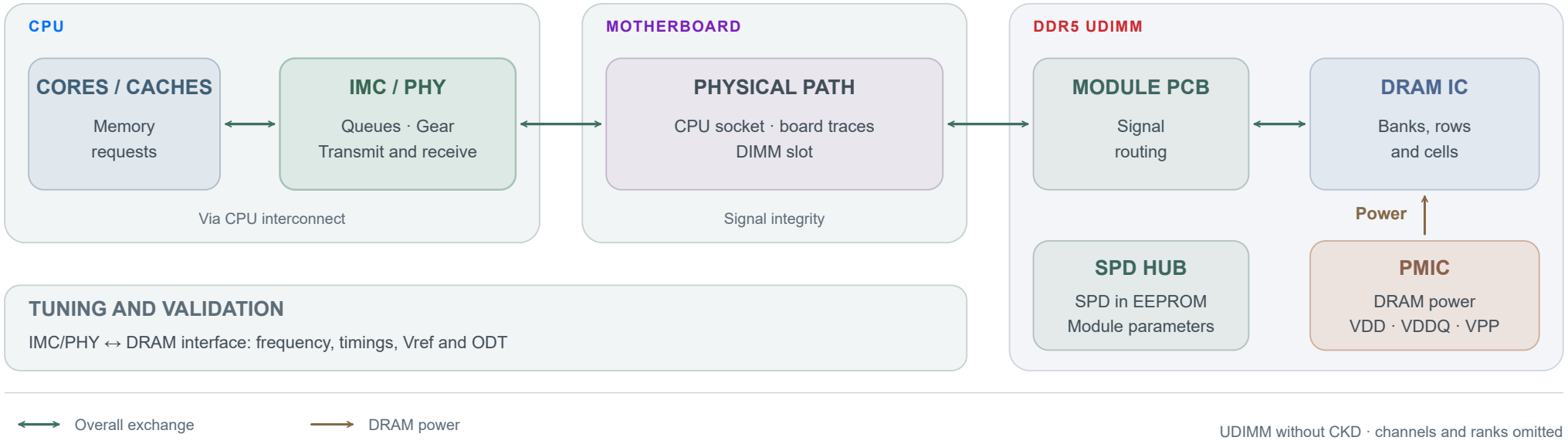
> **IMPORTANT BEFORE YOU BEGIN**
>
> XMP is also overclocking relative to the baseline JEDEC mode. Memory errors may be obvious or go unnoticed while causing data corruption. Keep a backup of important files on another storage device or in the cloud, and perform experiments on a system that can be safely recovered.

02 / DDR5 fundamentals and platform selection

2.1 WHAT EXACTLY ARE WE OVERCLOCKING?

DDR5 overclocking means tuning the entire chain from the memory controller in the processor to the DRAM cells. Increasing Memory Frequency places greater demands on the entire signal path: the CPU socket, motherboard traces and DIMM slot. The interface must then train correctly and reproduce the result at every boot.

FROM THE CPU TO DRAM CELLS



DATA RATE AND CLOCK FREQUENCY

Data rate R is measured in MT/s, or millions of transfers per second on each data pin. DDR5 transfers data on both clock edges, so the interface clock frequency **fCK** is half the data rate. **tCK** is the duration of one clock cycle.

For R in MT/s:

- fCK (MHz) = R / 2
- tCK (ns) = 1000 / fCK = 2000 / R
- Bandwidth of one 64-bit channel (GB/s) = R × 8 / 1000
- Bandwidth of two 64-bit channels (GB/s) = R × 16 / 1000

DDR5-4800 example:

- fCK = 4800 / 2 = **2400 MHz**
- tCK = 2000 / 4800 ≈ **0.417 ns**
- One-channel bandwidth = 4800 × 8 / 1000 = **38.4 GB/s**
- Two-channel bandwidth = 4800 × 16 / 1000 = **76.8 GB/s**

Mode	fCK	tCK	Bandwidth / 64 bits	Bandwidth / 2 × 64 bits
DDR5-4800	2400 MHz	0.417 ns	38.4 GB/s	76.8 GB/s
DDR5-5600	2800 MHz	0.357 ns	44.8 GB/s	89.6 GB/s
DDR5-6000	3000 MHz	0.333 ns	48.0 GB/s	96.0 GB/s
DDR5-7200	3600 MHz	0.278 ns	57.6 GB/s	115.2 GB/s
DDR5-8000	4000 MHz	0.250 ns	64.0 GB/s	128.0 GB/s
DDR5-8800	4400 MHz	0.227 ns	70.4 GB/s	140.8 GB/s

GB/s uses decimal units. This is theoretical data-bus bandwidth; actual throughput depends on the access pattern, DRAM refresh and controller behavior.

CL, LATENCY AND FREQUENCY

CL (CAS Latency) is the number of clock cycles between a READ command and the start of DRAM data output. The duration of this interval in nanoseconds is:

CAS latency (ns) = CL × tCK = CL × 2000 / R, where **R** is the data rate in MT/s.

For example, **DDR4-3600 CL18** and **DDR5-7200 CL36** have the same CAS latency of **10 ns**. DDR5 uses twice as many cycles, but each cycle is half as long. The theoretical bandwidth of one 64-bit channel is **28.8 GB/s for DDR4-3600** and **57.6 GB/s for DDR5-7200**.

DDR5's key advantage is high bandwidth enabled by substantially higher data rates. At comparable CAS latency, DDR5 can transfer considerably more data per unit of time than DDR4.

CHANNEL, SUBCHANNELS, AND CONTROLLER

A standard DDR5 UDIMM remains 64 bits wide, but is split into two independent 32-bit subchannels. They increase parallelism within a single memory channel. Two 64-bit CPU channels still require at least two correctly installed modules.

Gear indicates the ratio of the controller-domain frequency to the DRAM clock frequency. Gear 1, or 1:1, exists in Intel terminology and remains practically relevant primarily for DDR4. Official Intel operating points for DDR5 on LGA1700 use Gear 2, while LGA1851 uses Gear 2 or Gear 4; Gear 1 is not relevant as a high-frequency DDR5 mode. A higher Gear makes high MT/s easier to achieve, but adds command-path latency.

WHICH GROUPS OF SETTINGS CHANGE IN BIOS

Group	Examples	What changes in practice
Frequency / Gear	Memory Frequency, Gear 2/4	Bandwidth ceiling and command-path latency.
Timings	tCL, tRCD, tRP, tRFC, tREFI	Delays between operations and access efficiency.
Voltages	VDD/VDDQ, SA, TX VDDQ	Signal margin, heat, and IMC behavior.
Training	Vref, ODT, line delays	The mode's ability to train and remain repeatable after boot.

> **PRACTICAL TAKEAWAY**
>
> MT/s sets the bandwidth ceiling, timings determine the delays, and the IMC and physical signal path determine whether the system can reproduce the mode. Choose frequency and timings that suit the IMC and motherboard.

DOCUMENTATION REVIEWED: JEDEC JESD79-5D v1.41; Micron DDR5 SDRAM and Client Module Features; Intel EDC 832586. Diagram: Intel DDR5 I/O · Altera DDR5 routing · Renesas PMIC · SPD Hub.

2.2 Gear Mode and Command Rate

In this chapter, let’s look at the controller clock mode and command scheduling. Gear Mode sets the IMC-to-DRAM clock ratio. Command Rate (CR) governs command spacing on the command/address interface through stretched cycles and scheduled gaps. These settings affect memory access alongside operation-specific delays such as tCL. That is why I chose to place this chapter here.

GEAR MODE

Mode	IMC : DRAM	IMC clock
Gear 1 / G1	1:1	Same as DRAM
Gear 2 / G2	1:2	Half the DRAM clock
Gear 4 / G4	1:4	Quarter of DRAM clock

The Intel DDR5 platforms covered here use G2 and G4. At DDR5-8000, DRAM runs at 4000 MHz and the IMC at 2000 MHz in G2 or 1000 MHz in G4.

Gear 1 and Gear 2 were already used with DDR4 on 11th Gen desktop Core CPUs; the specified mode depended on the CPU model. G1 is included in the table for comparison with DDR4.

COMMAND RATE

CR	Meaning
Auto	BIOS/MRC chooses the mode for the configuration; it may select a setting other than 2N.
1N / CR1	A mode with tighter command spacing. Availability and actual use depend on the platform and BIOS; for the high data rates considered here, 2N remains the baseline.
2N / CR2	More conservative command issuance with additional timing margin on the command/address interface.
3N	An additional controller mode for stretching command cycles.
N:1	Intel: N valid command cycles in succession, then one gap; N = 1–7.

ASUS Z790 E21287 lists Auto / 1N / 2N / 3N / N:1 and N to 1 ratio from 1 to 7. For Z890, C25061 specifies Auto / 1N / 2N; Intel documents only 1N and 2N for Core Ultra 200S. The 3N and N:1 modes in this chapter apply to Z790.

PRACTICAL STARTING POINT

For daily DDR5 overclocking, we use Gear 2 + CR2 as the baseline

Moving to another mode should deliver a measurable gain. POST and benchmarks should be followed by separate daily-stability testing. The proposed daily DDR5 setup does not use 3N or N:1.

With DDR4, CR1/1T was used to reduce command delays. It was a basic target for tight tuning, particularly with Samsung B-die.

HIGH SPEEDS AND CUDIMM

G4 lowers the required IMC clock, usually at the cost of higher latency. It works with both UDIMMs and CUDIMMs. CKD improves the CUDIMM clock signal; Gear is selected in the CPU memory controller. On 20 Nov 2024, ASUS showed 8800–9000 MT/s in G2 and described Auto selecting G2 through 9066 MT/s. The usable G2 range depends on the CPU, BIOS and memory kit.

Kingston compared one 48 GB (2 × 24 GB) CUDIMM kit at 8800 G2 and after overclocking to 9600 G4. The system used a Z890 Apex, BIOS 1801 and a Core Ultra 7 265K.

AIDA64	8800 · G2	9600 · G4
Read, GB/s	127.15	126.71
Write, GB/s	102.14	101.79
Copy, GB/s	112.47	117.85
Latency, ns	74.6	86.7

8800 G2 has lower latency, read and write speeds are almost equal, and 9600 G4 copies faster. These are two complete memory profiles. An FPS gain has not been confirmed. Technically, a G2 configuration is more efficient.

On 24 Oct 2024, G.SKILL demonstrated 9600 CL46-58-58 in G4 with 2 × 24 GB CUDIMM on a Z890 Taichi OCF and Core Ultra 7 265K. That result applies to the demonstrated system; a similar kit needs its own stability testing.

BIOS CR AND MEMORY COMMANDS

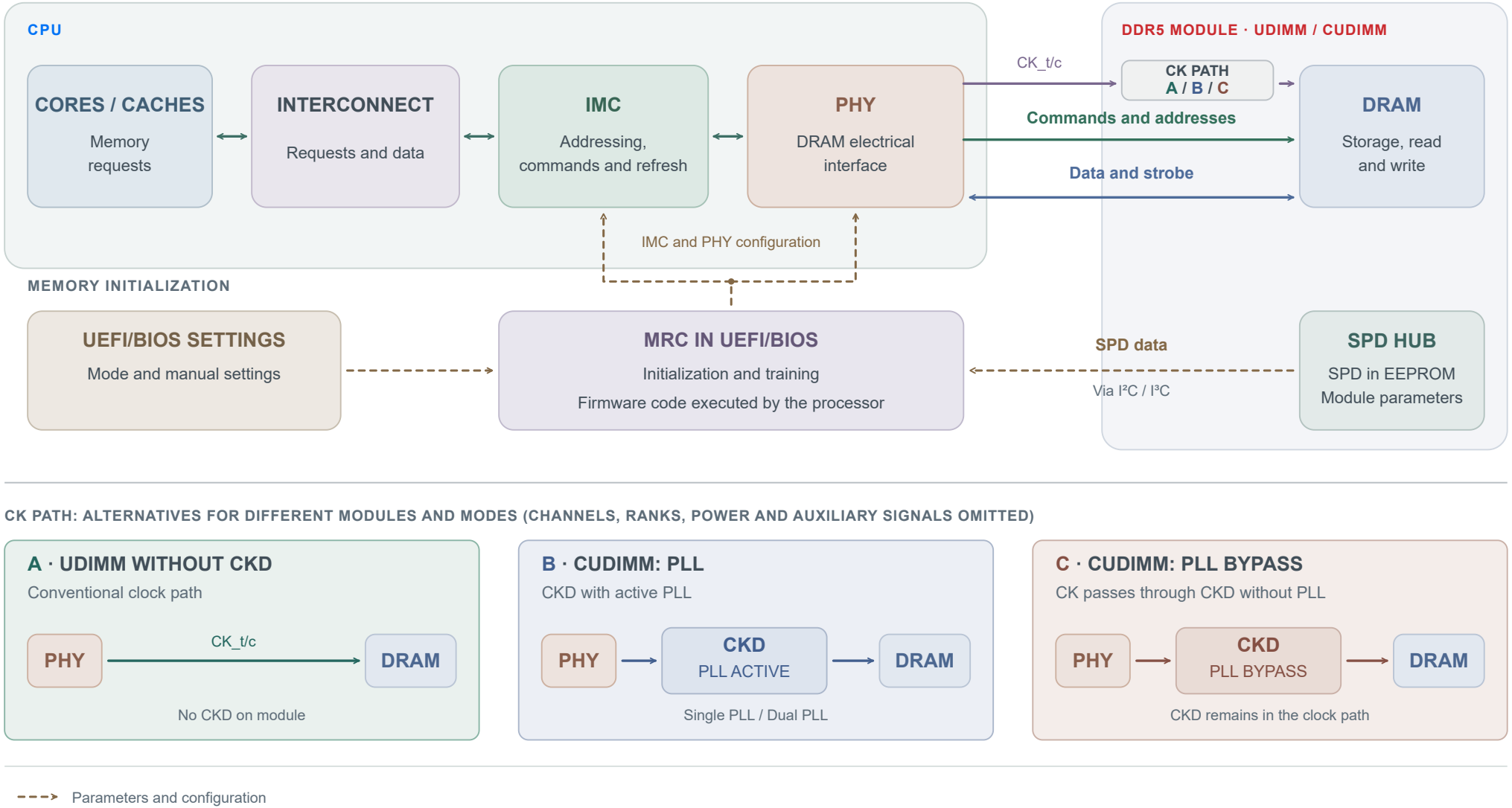
CR describes how the controller stretches command cycles and inserts gaps. The memory protocol sets the one- or two-cycle format of DDR5 commands. In Gear 2, the controller runs at half the DRAM clock, so the BIOS CR number does not state the length of every command. Intel's 2N/4N note also requires checking how ASUS applies the setting. N:1 on Z790 has a separate discrepancy: Intel counts cycles before one gap; ASUS counts gaps between cycles. The N value alone therefore cannot identify the faster mode.

DOCUMENTATION REVIEWED: Intel DDR4 · Z790 BIOS · Z890 BIOS · Intel ADL · ASUS CKD · Kingston · G.SKILL · SK hynix · Corsair · Intel ARL · DDR5 1T · B-die 1T

2.3 IMC: MEMORY CONTROLLER

The IMC, or integrated memory controller, is the memory controller built into the processor. It accepts requests, distributes them among channels, ranks, and banks, builds the DRAM command queue, and services refresh. The PHY handles the electrical interface with the memory lines. The MRC within the BIOS operates only during boot: it reads the SPD, configures the IMC/PHY, runs memory training, and leaves behind a working configuration. The MRC is not part of the memory request path during operation.

MEMORY REQUEST PATH



UDIMM and CUDIMM: clock paths A–C are alternatives.

TWO CHANNELS AND FOUR DDR5 SUBCHANNELS

Raptor Lake-S remains a dual-channel desktop platform. In DDR5 mode, each of memory channels A and B comprises two independent 32-bit subchannels, totaling 64 data bits per channel. With both channels in use, four 32-bit subchannels are available. Here, four 32-bit subchannels form two 64-bit channels. A quad-channel platform has four 64-bit channels.

Intel describes two independent MC blocks, one per memory slice. The practical takeaway for the user is that both channels should be populated symmetrically using the motherboard's recommended slots, while the subchannels allow the scheduler to interleave requests more flexibly.

Component	How it works	What this means for overclocking
Gear	Ratio of the MC frequency to the DRAM clock frequency: G1=1:1, G2=1:2, G4=1:4.	Official Raptor Lake DDR5 operating points use Gear 2. It makes high MT/s easier to achieve, but adds command-path latency.
Training	The MRC reads the SPD, initializes the IMC/PHY, and trains delays, Vref, and ODT.	A successful POST confirms only that the system booted. Stability must be demonstrated with separate tests and repeated boots.
Load	Rank, DIMM count, the second slot, and routing change the electrical load.	The limit depends on the individual CPU, motherboard, modules, and BIOS. More voltage does not always produce a better result.

HOW LOAD LOWERS THE OFFICIAL RATING

DDR5 configuration on Raptor Lake-S	Intel, MT/s
1SPC / 1DPC, one single-rank DIMM per channel	5600
1SPC / 1DPC, one dual-rank DIMM per channel	5200
2SPC / 1DPC, one DIMM installed per channel	4400
2SPC / 2DPC, two single-rank DIMMs per channel	4000
2SPC / 2DPC, two dual-rank DIMMs per channel	3600

Official operating modes for higher-end 13th Gen Intel Core desktop processors. Some CPU models have lower limits; operation above specification is overclocking.

PRACTICAL TAKEAWAY

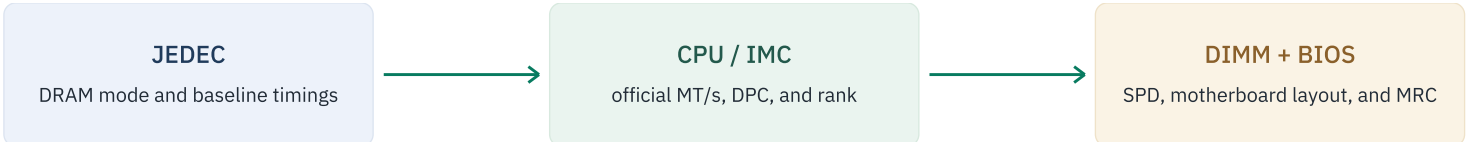
A memory test error does not prove a DRAM defect: the limitation may lie in the IMC, signal path, training, or voltages. First find the frequency and Gear using loose timings, then change one parameter at a time and test boots after idle alongside stability after warm-up under load.

DOCUMENTATION REVIEWED: Intel 13th/14th Gen Core Processor Datasheet, Vol. 1: Memory Controller, Organization Mode, System Memory Frequency, SAGV Points, and Power Training (DDR interface power-consumption training). Diagram: Intel DDR5 signals · Intel FSP · Renesas SPD Hub · Kingston CKD · Rambus CKD modes · Renesas CKD and PLL bypass.

2.4 JEDEC, MT/s, AND VOLTAGES

The word "standard" has three different meanings here. JEDEC defines operating modes for the DRAM devices themselves, Intel specifies the official memory-controller limit for a particular processor, and the module manufacturer writes supported parameters to the SPD. A mode is standard for the entire system only when all three layers support it simultaneously.

THREE LAYERS OF COMPATIBILITY



JEDEC SPEED BINS USED IN THIS CHAPTER

This chapter uses JEDEC JESD79-5D v1.41, dated November 2025. It defines DDR5-3200, 3600, 4000, 4400, 4800, 5200, 5600, 6000, 6400, 6800, 7200, 7600, 8000, 8400, 8800, and 9200. The system's operating data rate also depends on CPU, motherboard and module support.

JEDEC bin	fCK	tCK	Bandwidth / 64 bits
DDR5-4800	2400 MHz	0.417 ns	38.4 GB/s
DDR5-6400	3200 MHz	0.313 ns	51.2 GB/s
DDR5-8000	4000 MHz	0.250 ns	64.0 GB/s
DDR5-9200	4600 MHz	0.217 ns	73.6 GB/s

WHAT IS CONSIDERED STANDARD ON OUR PLATFORMS

Platform	Official maximum	What matters
LGA1700 / 12th Gen	up to DDR5-4800	Depends on DPC and ranks; 2DPC lowers the supported mode.
LGA1700 / 13th–14th Gen	up to DDR5-5600	True 1SPC, 2R: 13th Gen - 5200; 14th Gen - 5600*. Modes are lower for 2SPC.
LGA1851 / Core Ultra 200S	1DPC: UDIMM 5600; CUDIMM 6400	CKD improves the clock signal; OC also depends on IMC capability.
LGA1851 / 200S Plus	1DPC CUDIMM up to 7200	The official POR is defined for a specific Intel configuration; check its conditions to determine whether it applies to the selected modules.

* In Intel's technical documentation for 14th Gen Core processors, support for DDR5-5600 with dual-rank modules (2R) is still pending official enablement by Intel; the product brief still lists DDR5-5200. We therefore do not treat 5600 as an unconditionally available current POR.

NOMINAL DDR5 VOLTAGES

For standard DDR5, the nominal DRAM VDD and DRAM VDDQ values are 1.10 V, while VPP is 1.80 V. However, a manual mode at 1.10 V does not automatically become JEDEC-compliant: the IC speed bin, SPD data, CPU support, and motherboard configuration must all match. XMP often uses higher VDD/VDDQ and tighter timings.

The key notation rule is: DDR5-8000 or 8000 MT/s is correct; "8000 MHz" is common slang. The clock frequency of this interface is approximately 4000 MHz.

WHY JEDEC-8000 CAN STILL BE OVERCLOCKING

The DDR5-8000 speed bin in JESD79-5D means that the standard defines such a mode for compatible DRAM devices. But a DDR5-8000 XMP kit may use its own timings and higher voltages, while the official CPU limit remains 5600, 6400, or 7200 MT/s. For such a system, 8000 MT/s is overclocking regardless of the number 8000 appearing in the JEDEC standard.

POR, or Plan of Record, is the officially supported Intel mode for the specified module and rank configuration. Operation above POR is overclocking.

DOCUMENTATION REVIEWED: JEDEC JESD79-5D v1.41; Intel EDC 655258, 743844, and 832586; Micron DDR5 SDRAM.

2.5 SPD AND INTEL XMP 3.0

SPD (Serial Presence Detect) is information about a module's organization and parameters stored in nonvolatile memory. In DDR5, this EEPROM is integrated into the **SPD Hub**. The BIOS reads SPD data when the computer starts.

SPD CONTENTS

Group	Stored data	Purpose
Organization	DIMM type, capacity, rank count, DRAM organization (x8/x16) and bus width	Determine the memory configuration.
JEDEC parameters	tCK range, supported CL values and minimum timing intervals	Calculate baseline frequency and timings.
Identification and integrity	Manufacturer, module P/N, serial number, date; data CRC	Identify the model and check SPD integrity.
Extensions	XMP and manufacturer/user areas	Additional profiles and module features.

XMP 3.0: OVERCLOCKING PROFILES

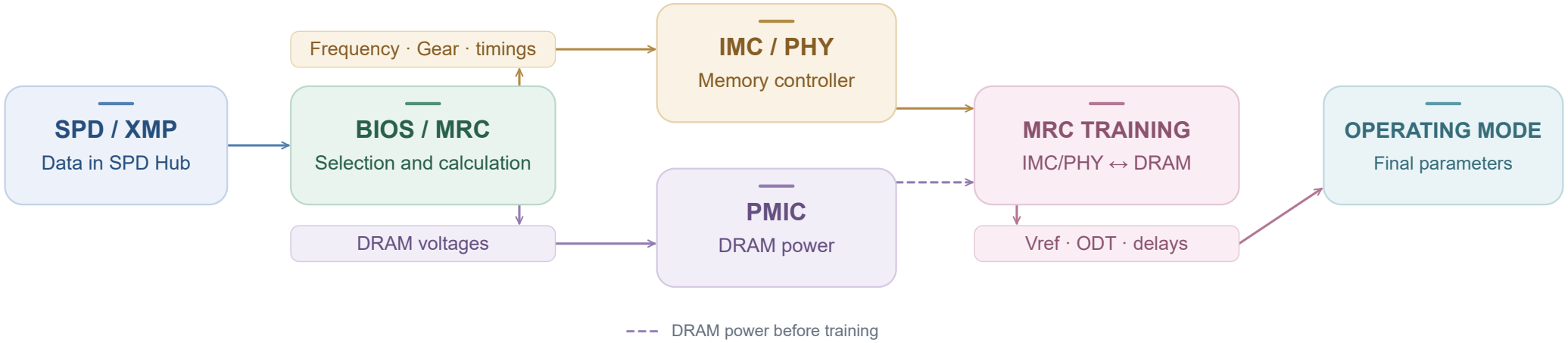
Intel XMP 3.0 is an overclocking profile format for DDR5. A factory profile combines data rate, timings and voltages validated by the kit manufacturer.

Up to five profiles are supported: **up to three factory profiles and two rewritable user profiles**. The factory profiles available depend on the model. User XMP profiles are written to the module through a BIOS or utility that supports this feature. BIOS profiles store the motherboard's own settings.

At first boot, baseline JEDEC parameters are used. XMP is selected separately in the BIOS.

BUILDING THE OPERATING MODE

BIOS/MRC uses SPD/XMP to select frequency, Gear, timings and IMC parameters; the PMIC supplies the specified DRAM voltages. During training, MRC determines Vref, ODT and interface delays.



Module data is supplemented by Auto calculations, including some secondary and tertiary timings, and training results. Automatic settings depend on the motherboard and BIOS version; trained values also depend on the CPU, modules, temperature and boot conditions. The same XMP can therefore produce different operating parameters on different boards, after a BIOS update or after retraining.

XMP IN ASUS BIOS

XMP I, XMP II and XMP Tweaked determine how the selected profile is applied. The module profile itself is selected separately.

Mode	How the profile is applied
XMP I	CL, tRCD, tRP and tRAS from XMP; ASUS optimizes the remaining parameters.
XMP II	Loads the complete parameter set recorded in the selected XMP profile.
XMP Tweaked	XMP with additional ASUS performance settings.

COMPATIBILITY AND QVL

Before enabling XMP, check the motherboard QVL against the **full part number (P/N) of the kit or module on its label or packaging**. Also check the revision if specified, capacity, module count and tested speed. The entry applies to the tested configuration. A different CPU sample, BIOS version or combination of kits requires separate verification.

The QVL lists models tested by the manufacturer. For other kits, assess compatibility from the memory and platform specifications, then test the actual system.

MY APPROACH TO TUNING

For daily use, I recommend **manual tuning from a stable baseline**. On Auto, motherboards may set excessive voltages, and training results need verification. After tuning, check the actual frequency, timings and voltages, then verify stability under load and repeatable boots.

DOCUMENTATION REVIEWED: Intel XMP; Renesas SPD5118; ASUS BIOS Manual; ASUS QVL; G.SKILL FAQ; Intel FSP.

2.6 PMIC — POWER CONTROL ON A DDR5 MODULE

The PMIC (Power Management Integrated Circuit) converts motherboard power into the DRAM supply rails: VDD, VDDQ and VPP. It sets their voltages, manages startup and monitors overloads and overheating. The PMIC is one chip; the complete power circuit also includes inductors, capacitors and other components on the module PCB.

Desktop DDR5 solutions include Richtek RTQ5132/RTQ5136, Renesas P8911 and ANPEC APW8502C. As of 11 October 2026, newer confirmed client designs include the second-generation Renesas RRG5332, a JEDEC PMIC5120-class device, and Think Future SY5889 with CUDIMM support. Model names and JEDEC classes describe the product and its capabilities; silicon revisions require separate identification. The table lists models or literal package markings checked against teardown photographs.

For overclocking, check the available voltage range, module configuration, BIOS support and power stability under load. Richtek RTQ5136 and Think Future SY5888 offer an extended VDD/VDDQ range up to 2.2 V; SY5888 also specifies Intel XMP 3.0 OC support. Access to higher voltages depends on the module and motherboard. A High DRAM Voltage switch in the BIOS cannot remove every restriction. Check physical markings when identifying the PMIC: SPD and BIOS identification can be wrong.

PMICS FOUND IN REVIEWED KITS

Kit, exact SKU	Rated profile	PMIC: model / marking	Source, year
Kingston Fury Beast KF560C40BBK2-64	2 × 32 GB 6000 CL40	Richtek 0P=AC UG1	Tom's HW 2024
G.Skill Trident Z5 NeoX RGB F5-6000A3038F16GX2-TZ5NXRK	2 × 16 GB 6000 CL30	ANPEC APW8502C / VBA50	Tom's HW 2026
Patriot Viper Venom RGB PVVR532G640C32K	2 × 16 GB 6400 CL32	Richtek 0P=AL	TweakTown 2026
Patriot Viper Venom PVV532G640C32K	2 × 16 GB 6400 CL32	Think Future SY5888	Igor'sLAB 2025
Patriot Viper Xtreme 5 Aurum VXA532G8038K	2 × 16 GB 8000 CL38	MPS MPSG 5431 CQ83	TweakTown 2025
Corsair Dominator Titanium First Edition CMP48GX5M2X7200C36FEW	2 × 24 GB 7200 CL36	Richtek 0P=AD 7G1	Tom's HW 2023
G.Skill Trident Z5 RGB F5-6400J3239F48GX2-TZ5RW	2 × 48 GB 6400 CL32	Richtek 0P=AJ 7G1	Tom's HW 2024
G.Skill Trident Z5 Neo RGB F5-6000J3444F64GX2-TZ5NR	2 × 64 GB 6000 CL34	Richtek 0P=CF MY2	Tom's HW 2026
V-Color Manta XFinity RGB TMXFAL6464832KWK	2 × 64 GB 6400 CL32	Richtek 0P=BH 3YM	Tom's HW 2026

These are the reviewed samples; PMICs may differ between production batches of the same SKU.

> **WHAT MATTERS WHEN CHOOSING A KIT**
>
> A newer PMIC alone does not improve overclocking. Check whether it supports your intended profile. A 2.2 V capability is a power-controller feature, not a safe DRAM voltage. Memory ICs and the IMC still set the final overclocking limits.

DOCUMENTATION REVIEWED: Richtek RTQ5136; Renesas RRG5332; Think Future SY5888; SY5889; ANPEC

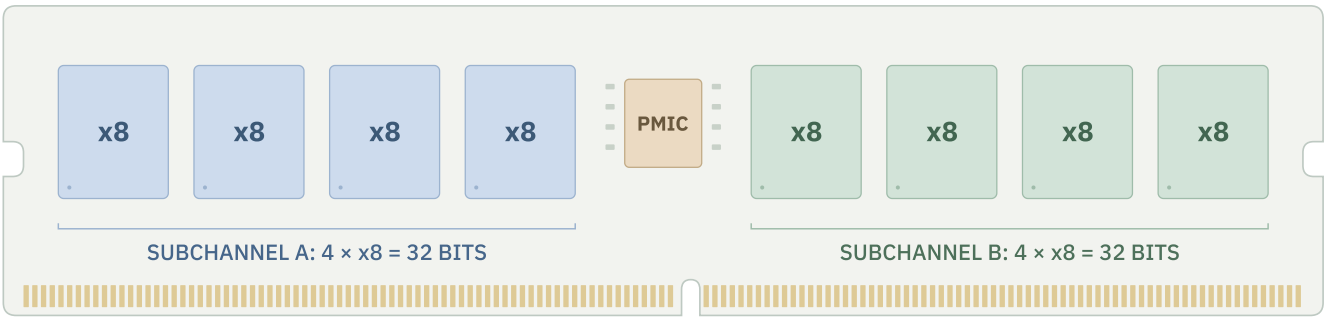
2.7 RANK, X4/X8/X16 ORGANIZATION AND DENSITY

A "32 GB" label indicates only total capacity. It does not show the number of ranks, device width, or density of a single die. These characteristics are independent and are often more important for overclocking than capacity itself.

BASIC DDR5 RANK ORGANIZATION: x4, x8 AND x16

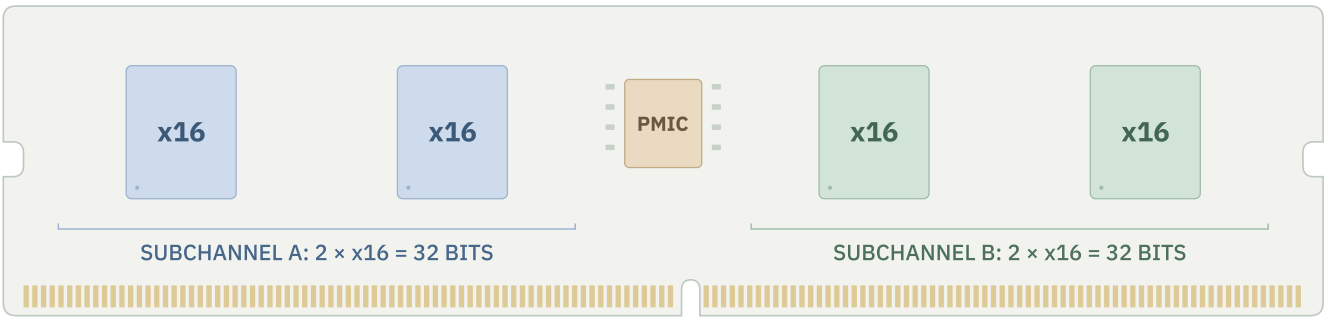
Each diagram shows one rank: two independent 32-bit subchannels and 64 data bits in total. x4, x8 and x16 are the data interface widths of individual DRAM devices.

1Rx8 · 8 data DRAM devices



1 rank · 64 data bits · 2 subchannels of 32 bits

1Rx16 · 4 data DRAM devices



1 rank · 64 data bits · 2 subchannels of 32 bits

Component placement is schematic: rows do not represent PCB sides or additional ranks. Only the rank's 64-bit data portion is shown; additional DRAM devices for system ECC check bits and stacked-die packages are outside the scope of these diagrams.

x4, x8 and x16 describe the data interface width of an individual DRAM device: 4, 8 and 16 DQ lines. Organization determines the device's internal architecture and how a rank is built. Density in gigabits is a separate device parameter.

Parameter	x4	x8	x16
DQ width	4 bits	8 bits	16 bits
DRAM page size	1 KB	1 KB	2 KB
Bank groups (BG)	8	8	4
Banks	32	32	16
Minimum tFAW	32 CK	32 CK	40 CK

For 16 Gbit DRAM at DDR5-5600. Micron specifies tFAW ≥ max(32 CK, 11.428 ns) for x4/x8 and max(40 CK, 14.285 ns) for x16. See Section 3.5 for details. For other densities and speeds, consult the specification for bank counts and timing limits.

Page size depends on the number of columns in a bank row and the DQ width. For x16: 1024 × 16 / 8 = 2048 bytes (2 KB). ACT opens a row, placing its data in the row buffer.

In a standard DDR5 UDIMM without system ECC, a rank uses 8 x8 devices (8 × 8 = 64 bits) or 4 x16 devices (4 × 16 = 64 bits). At equal device density, x16 needs half as many DRAM packages. These 64 bits span two 32-bit DIMM subchannels, distinct from CPU memory-controller channels.

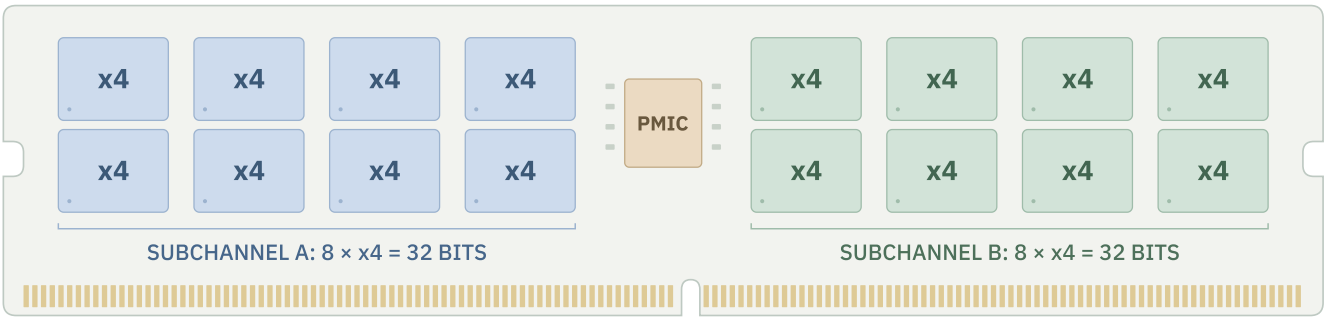
Desktop DDR5 uses x16 primarily in 8 GB modules: four 16 Gbit devices provide 8 GB. Other device densities allow other capacities. The table lists 288-pin UDIMMs with confirmed organization.

Manufacturer / P/N	Capacity	Data rate	Organization
Kingston KVR56U46BS6-8	8 GB	5600 MT/s	1Rx16
Kingston KCP556US6-8	8 GB	5600 MT/s	1Rx16
Lexar LD5U08G56C46ST-BGS	8 GB	5600 MT/s	1Rx16
Transcend JM4800ALG-8G	8 GB	4800 MT/s	1Rx16
Transcend JM5600ALG-8G	8 GB	5600 MT/s	1Rx16

X4 ORGANIZATION

x4 is mainly used in server ECC RDIMMs. Kingston KSM56R46BD4-64MH, KSM64R52BD4-64MH, KSM64R52BD4-96MC, KSM48R40BD4-64HA, KSM48R40BD4-64MD and KSM64R52BD4-128MB are all 2Rx4.

1Rx4 · 16 data DRAM devices



1 rank · 64 data bits · 2 subchannels of 32 bits

A dual-rank DIMM still has two physical subchannels; each one simply has two ranks available. The term “four subchannels” is sometimes used for the four rank × subchannel combinations. Such a DIMM has two physical subchannels.

DIE DENSITY DETERMINES RANK CAPACITY

x8 die density	One die	1Rx8	2Rx8
16 Gbit	2 GB	16 GB	32 GB
24 Gbit	3 GB	24 GB	48 GB
32 Gbit	4 GB	32 GB	64 GB

WHAT IS CALLED NON-BINARY DDR5

Non-binary DDR5 refers to memory built with 24-Gbit dies, typically in 24 GB and 48 GB capacities. In a standard non-ECC DIMM using x8 SDP devices, one package contains one die. Capacity in GB = density of one die in Gbit × number of dies per rank × number of ranks / 8.

HOW TO CHECK YOUR MODULE'S ORGANIZATION

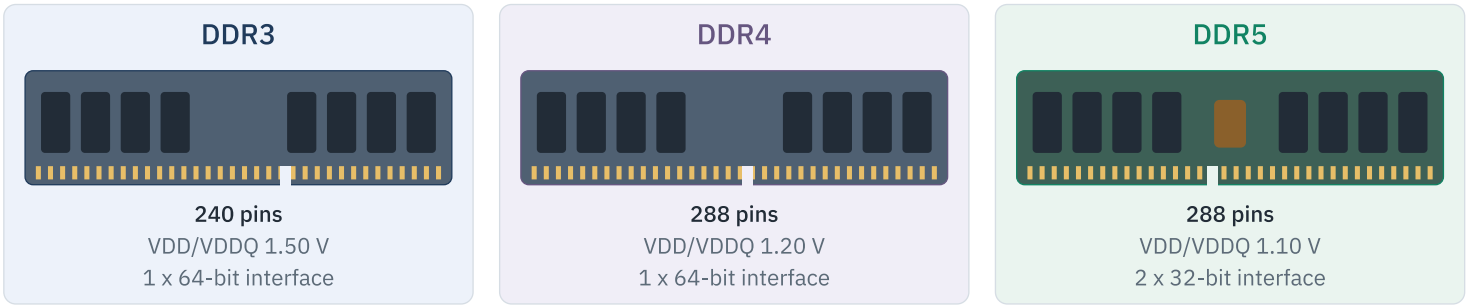
Source	What to look for	Reliability
SPD	Module organization: ranks, x8/x16, and capacity	A quick way to check an installed module.
Label / datasheet	Exact part number and official specification	The best source for a production module.
PCB inspection	Package count and markings	A PCB side alone does not confirm rank count. Check the IC marking.

DOCUMENTATION REVIEWED: Micron DDR5 Client Module Features; Kingston DDR5 overview, glossary, and 32Gbit DRAM guide.

2.8 PCB DESIGN: SIDES AND RANKS

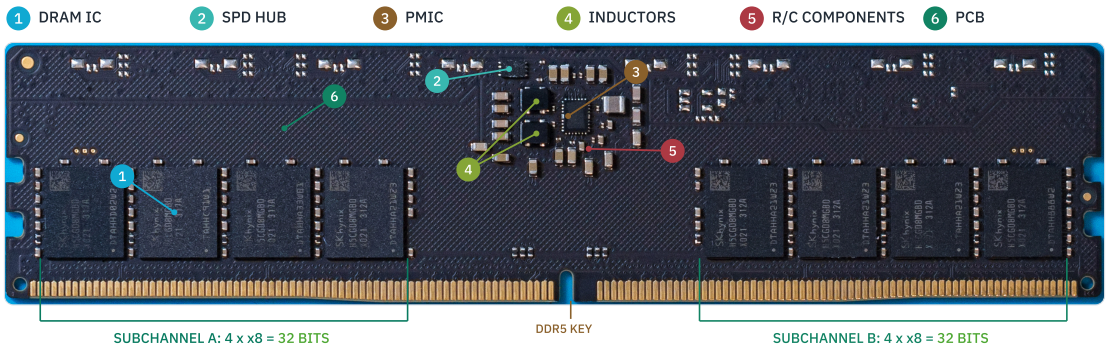
A new memory generation changes more than speed. The electrical interface, operating voltage, pinout, key position, and internal DIMM organization change with it. Similar appearance does not imply compatibility, and with DDR5 the physical IC layout must be distinguished from logical rank organization.

THREE GENERATIONS — THREE INCOMPATIBLE SLOTS



DDR3L uses 1.35 V. DDR4 and DDR5 both have 288 pins, but differ in pinout and key position.

WHAT IS FOUND ON A TYPICAL DDR5 1Rx8 UDIMM



TeamGroup T-Force Xtreem DDR5-8200, 24 GB: 1Rx8, eight SK hynix 24-Gbit x8 DRAM ICs.

RANK AND DEVICE PLACEMENT ON THE PCB

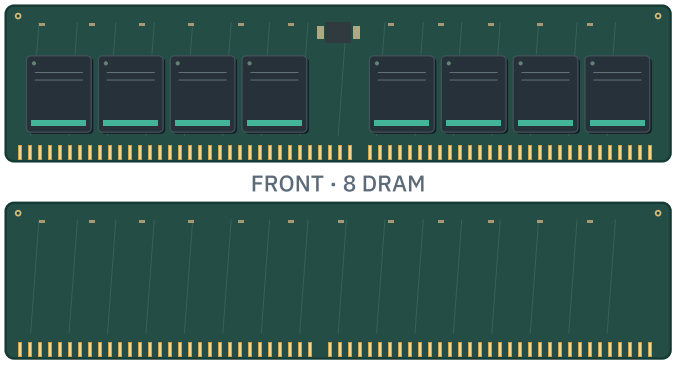
A rank is a group of DRAM devices selected by a Chip Select signal. Each 32-bit DDR5 subchannel selects its own group of DRAM devices; together, the two groups form a 64-bit module rank. 1Rx8 means one rank built with x8 devices; 2Rx8 means two. The number of PCB sides is not a reliable indicator: check the SPD, markings, and datasheet.

PCB SIDES AND RANK: DIFFERENT CHARACTERISTICS

Rank organization and the placement of ICs on PCB sides are different characteristics. **Single Rank (1R)** denotes one group of DRAM devices selected by one group of Chip Select signals. **Double-sided (DS)** means only that ICs are physically soldered to both sides of the PCB. These characteristics coincided on many DDR3/DDR4 modules, which perpetuated the confusion.

1R + SS (Single Side)

One rank, one side

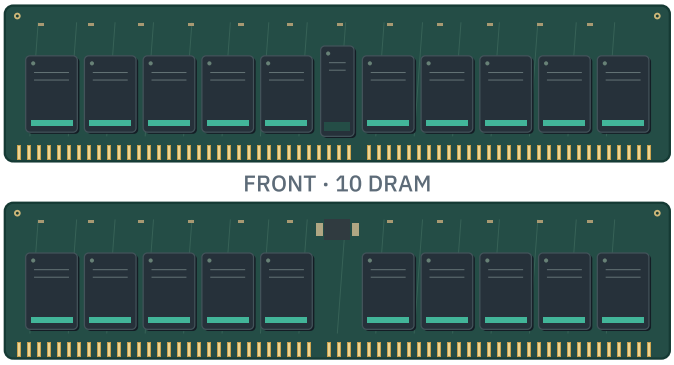


CS0 / R0

A typical DDR5 1Rx8 UDIMM. Eight x8 packages form 2 x 32 bits. Both groups are R0.

1R + DS (Double Side)

One rank, two sides

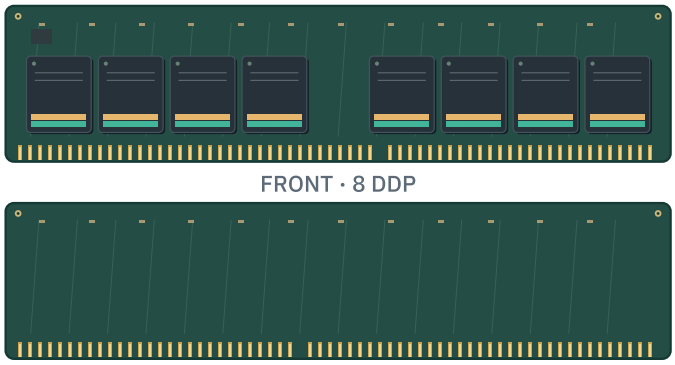


CS0 / R0

Kingston **KSM48R40BS4TMI-32MDI** [1]. DDR5, 32 GB, 1Rx4 ECC RDIMM. 20 x x4 = 2 x 40 bits.

2R + SS (Single Side)

Two ranks, one side

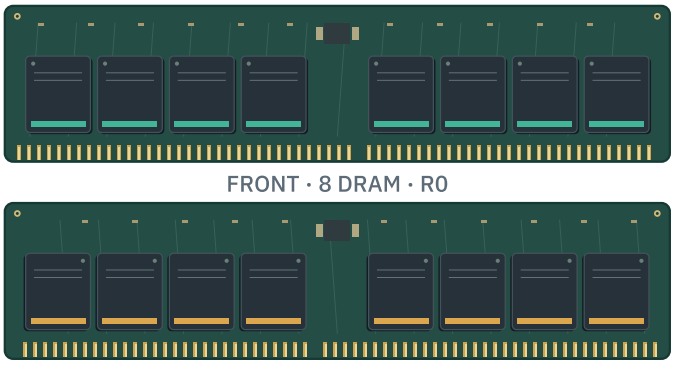


CS0 / R0 CS1 / R1

Example from RAMGuide: early Corsair DDR4 8 GB, Hynix MMR. The source does not identify the exact SKU.

2R + DS (Double Side)

Two ranks, two sides



CS0 / R0 CS1 / R1

DDR5 2Rx8 UDIMM: one module, 16 x8 ICs. 16 Gbit → 32 GB; 24 Gbit → 48 GB. [1, 10] Examples: 2 × 32 and 2 × 48 GB kits.

> The colored bars indicate membership in R0 and R1. Verify rank through the SPD and datasheet.

DIAGRAM SOURCES: 1R + DS — [1] Kingston KSM48R40BS4TMI-32MDI; 2R + SS — RAMGuide; 2R + DS — [1] Kingston KVR56U46BD8-32, [10] Kingston KVR56U46BD8-48.

> **Rank organization and IC placement on the PCB sides are different characteristics. Among standard DDR5 UDIMMs/SO-DIMMs in production, I found no confirmed 2R + SS module. Every verified 2Rx8 DDR5 module uses 16 DRAM packages and is DS.**

> On mainstream desktop DDR5 UDIMMs, 2R is usually built from 16 separate x8 SDPs (Single-Die Packages), resulting in 8 packages on the front and 8 on the back. For example, Kingston describes current 64 GB DDR5 UDIMMs built with 32-Gbit DRAM as exactly 16 x x8 = 64 GB, 2 ranks.

2.8.1 DRAM IC: DIE AND PACKAGE

DRAM stands for Dynamic Random Access Memory. On a memory module, it takes the form of **ICs** (Integrated Circuits). A single package may contain one or more dies.

> **SILICON DIE**
>
> Silicon containing memory cells. Data is stored as charge in capacitors; **refresh** periodically restores that charge.

> **IC PACKAGE**
>
> Protects the die and connects it to the board. Inside are the die, interconnects, and a substrate with traces.

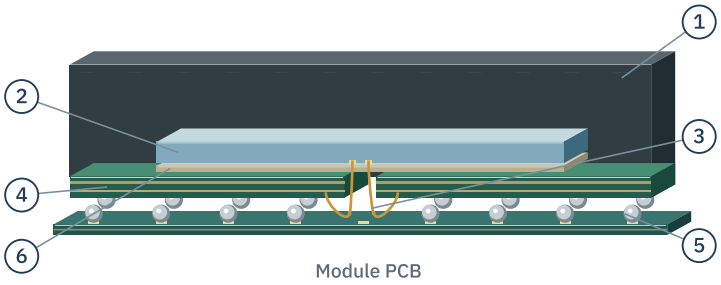
> **MODULE PCB**
>
> Holds the packaged ICs. Each package has its own small substrate.

ONE PACKAGE, DIFFERENT DIE COUNTS

Examples of wire-bonded packages

SDP · one die

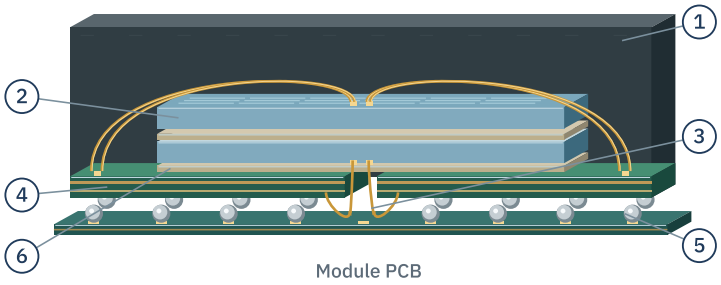
Single-Die Package



- 1 Molding compound
- 3 Bond wires
- 5 Solder balls

DDP · two dies

Dual-Die Package



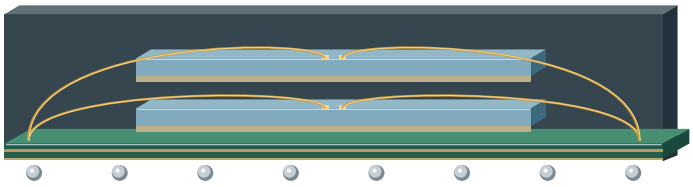
- 2 Silicon die
- 4 Package substrate
- 6 Adhesive layer

FBGA (Fine-Pitch Ball Grid Array) is a package with closely spaced solder balls. The balls on its underside are soldered to the module PCB.

HOW TWO DIES FIT INTO ONE PACKAGE

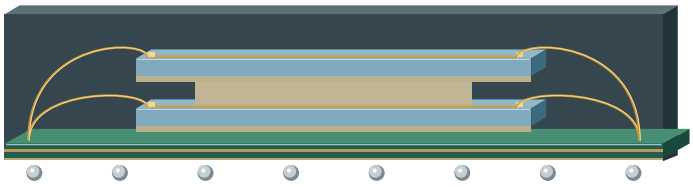
DDP assembly variants · Invensas

1. Center pads



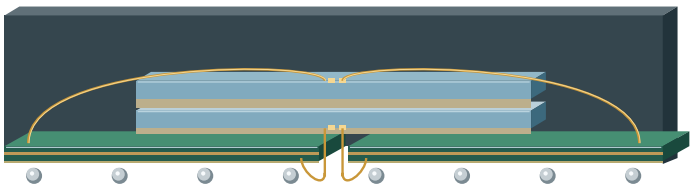
Both dies face up. Bond wires connect the center pads to the substrate.

2. Edge pads



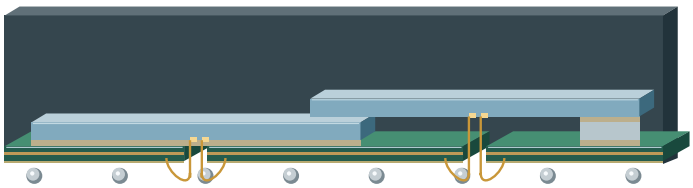
RDL routes the pads to the edges. A spacer separates the dies.

3. Back-to-back



The lower die connects through a window in the substrate; the upper die connects from above.

4. Both dies face down



The dies are offset. Bond wires pass through windows in the substrate.

RDL (Redistribution Layer) relocates the pads across the die surface.

READING THE MODULE LAYOUT

8 DDP packages contain 16 dies. Rank organization depends on their connections and select signals. I check rank organization and device width against the **SPD data and the module datasheet**.

Intel: IC, die, package SIMMTECH: substrate Micron: DDR5 DDP Invensas: cross-sections

2.9 ERROR CORRECTION: ECC AND ON-DIE ECC

SYSTEM ECC, on-die ECC AND non-ECC

System ECC — Error correction performed by the CPU memory controller. A separate layer of correction typically used in server or workstation systems.

on-die ECC — Error correction inside a DRAM IC (chip). The IC stores its own check bits and corrects a single-bit error in its internal data block before returning it. This is a basic feature of all standard DDR5 memory, including ordinary desktop UDIMMs and CUDIMMs.

non-ECC — In a module designation, this means the absence of system ECC. DDR5 modules of this type retain internal on-die ECC.

SYSTEM ECC WITHOUT on-die ECC

System ECC can operate independently. Ordinary DDR4 memory with system ECC is an example: the CPU controller checks data using additional bits, while this configuration has no on-die ECC. In DDR5, internal correction is already part of the DRAM design.

TWO LEVELS OF DDR5 PROTECTION

DDR5 with active system ECC uses both levels. During a read, DRAM's internal decoder first corrects an error within its capability in the cell array. Data then crosses the module and motherboard traces, and the CPU controller checks it with the external check bits. Internal correction is thus complemented by protection of storage and transfer between memory and the processor.

Error correction is an advantage of the memory subsystem as a whole. Chip quality and overclocking binning are assessed separately.

APPLICATION AND OPERATING REQUIREMENTS

System ECC preserves data integrity and supports reliable long-running computations. It is uncommon on ordinary desktop platforms.

The DDR5 gaming and overclocking configurations covered here use on-die ECC, which corrects errors inside DRAM chips. System ECC additionally protects storage and data transfer between DRAM and the CPU memory controller. It requires compatible CPUs, motherboards and memory modules with system ECC, and is found mainly in servers and workstations, including selected desktop platforms.

A particular build also requires a BIOS version supporting the selected CPU and system ECC. Check module and slot-population compatibility against the motherboard documentation and QVL.

INTEL PROCESSOR SUPPORT FOR SYSTEM ECC

The table lists desktop LGA1700 and LGA1851 models based on official specifications. "Yes" identifies CPU support; active system ECC also requires a compatible motherboard, BIOS and memory.

Family / socket	System ECC	Processor models
Core 12th Gen · LGA1700	Yes	i9-12900KS, i9-12900, i9-12900T, i9-12900K, i7-12700, i7-12700T, i7-12700K, i5-12500, i5-12500T, i5-12600, i5-12600T, i5-12600K
Core 12th Gen · LGA1700	No	i9-12900F, i9-12900KF, i7-12700F, i7-12700KF, i5-12400, i5-12400F, i5-12400T, i5-12600KF, i3-12100, i3-12100F, i3-12100T, i3-12300, i3-12300T, i5-12490F
Core 13th Gen · LGA1700	Yes	i9-13900KS, i9-13900, i9-13900T, i9-13900K, i7-13700, i7-13700T, i7-13700K, i5-13500, i5-13500T, i5-13600, i5-13600T, i5-13600K
Core 13th Gen · LGA1700	No	i9-13900F, i9-13900KF, i7-13700F, i7-13700KF, i5-13400, i5-13400F, i5-13400T, i5-13600KF, i3-13100, i3-13100F, i3-13100T, i5-13490F, i7-13790F
Core 14th Gen · LGA1700	Yes	i9-14900KS, i9-14900, i9-14900T, i9-14900K, i7-14700, i7-14700T, i7-14700K, i5-14500, i5-14500T, i5-14600, i5-14600T, i5-14600K
Core 14th Gen · LGA1700	No	i9-14900F, i9-14900KF, i7-14700F, i7-14700KF, i5-14400, i5-14400F, i5-14400T, i5-14600KF, i3-14100, i3-14100F, i3-14100T, i5-14490F, i7-14790F
Core 5 Series 1 · LGA1700	No	5 120, 5 120F
Core Ultra 200S and A/TA · LGA1851	Yes	Ultra 5 235, Ultra 5 235T, Ultra 5 245, Ultra 5 245T, Ultra 7 265, Ultra 7 265T, Ultra 9 285, Ultra 9 285T, Ultra 5 245K, Ultra 7 265K, Ultra 9 285K, Ultra 5 235A, Ultra 5 235TA
Core Ultra 200S and A/TA · LGA1851	No	Ultra 5 225*, Ultra 5 225F, Ultra 5 225T, Ultra 7 265F, Ultra 5 245KF, Ultra 7 265KF, Ultra 5 230F
Core Ultra 200S Plus · LGA1851	Yes	Ultra 5 250K Plus, Ultra 7 270K Plus
Core Ultra 200S Plus · LGA1851	No	Ultra 5 250KF Plus

> **SYSTEM ECC IS UNAVAILABLE ON Z790 AND Z890**
>
> Although some processors support system ECC, motherboards based on Intel Z790 and Z890 do not. An ECC module, if accepted by the motherboard, operates without system ECC. Internal DDR5 on-die ECC remains active.

* Core Ultra 5 225: Intel ARK states No; the ASUS W880 CPU list states Yes. The table follows the CPU manufacturer’s specification.

INTEL MOTHERBOARDS WITH SYSTEM ECC SUPPORT

These are workstation motherboards for desktop professional systems. They use Intel LGA1700/LGA1851 platforms, DDR5 and system ECC. Check CPU, BIOS and ECC UDIMM compatibility for the selected model.

Platform	Manufacturer	Motherboard models
LGA1700 · W680	ASUS	Pro WS W680-ACE; Pro WS W680-ACE IPMI; Pro WS W680M-ACE SE
LGA1700 · W680	ASRock Rack	W680 WS
LGA1700 · W680	Supermicro	X13SAE; X13SAE-F
LGA1700 · W680	Sixunited	W680M6
LGA1851 · W880	ASUS	Pro WS W880-ACE SE
LGA1851 · W880	ASRock Rack	W880M WS
LGA1851 · W880	GIGABYTE	W880 AI TOP
LGA1851 · W880	Supermicro	X14SAE; X14SAE-F
LGA1851 · W880	Sixunited	W880M37

PRACTICAL SUMMARY

Z790/Z890 gaming and overclocking motherboards: ordinary DDR5 with on-die ECC, without system ECC.

W680/W880 workstation motherboards: system ECC is available with a compatible CPU, memory and BIOS.

2.10 KIT CAPACITY AND IMC LOAD

Memory-controller load depends on DIMMs and ranks per channel, x8/x16 organization, die density, motherboard routing, frequency and timings. The same total capacity can therefore impose a very different electrical load.

TYPICAL KITS FROM 2024–2026

Kit	Common organization	Ranks/channel	Practical significance
2 × 16 = 32 GB	16 GB 1Rx8, 16 Gbit	1	With H16A, second to non-binary H24M in OC potential. I consider this capacity outdated.
2 × 24 = 48 GB	24 GB 1Rx8, 24 Gbit	1	Best overclocking potential, but only with H24M (Hynix M-die).
2 × 32 = 64 GB	2Rx8/16 Gbit or 1Rx8/32 Gbit	1 or 2	Limited OC potential. Look for H16A (Hynix A-die) and newer revisions.
4 × 16 = 64 GB	four 1Rx8 modules	2 (2DPC)	Second branch: usually harder to drive than two 32 GB DIMMs.
2 × 48 = 96 GB	48 GB 2Rx8, 24 Gbit	2	Little OC headroom, which is not the priority here. For high frequency, 2 × 48 GB is usually preferable to 4 × 24 GB.
4 × 24 = 96 GB	four 1Rx8 modules	2 (2DPC)	High load and less signal margin.
2 × 64 = 128 GB	64 GB 2Rx8, 32 Gbit	2	Requires a validated BIOS, QVL support, and a conservative starting point.

> The highest established frequency overclocking limit for A-DIE revision chips in 2x32 and 2x48 kits is 7200 MT/s. In very rare cases, 7400 MT/s for 2x32.

SAME NUMBER OF RANKS, DIFFERENT ELECTRICAL TOPOLOGY

64 GB: 2 x 32 GB 2R

1 DIMM per channel
two ranks on the channel
fewer installed loads

64 GB: 4 x 16 GB 1R

2 DIMMs per channel
two ranks + second branch
second branch is active

WHAT REDUCES FREQUENCY HEADROOM THE MOST

A second DIMM on a channel is usually a heavier load than a second rank within one module: it engages the second routing branch and adds the electrical load of another module. Four DIMMs therefore tend to require a lower frequency than two, even with the same total number of ranks. A true 1SPC motherboard with one slot per channel also differs from a four-slot 2SPC motherboard, where the empty second branch still physically exists.

At the same MT/s, 2R may slightly improve performance by alternating accesses between ranks (Rank Interleaving, which had a dedicated BIOS option to enable it on MSI Z690 boards): while one rank is busy with an internal operation, the IMC accesses the other. In extreme overclocking, this benefit is often outweighed by the lower achievable frequency.

OFFICIAL INTEL MODES SHOW THE EFFECT OF LOAD

Configuration	POR (Intel mode)	How to interpret it
LGA1700 13th, true-1SPC / 1DPC	1R 5600; 2R 5200	For 13th Gen, the second rank lowers POR.
LGA1700 14th, true-1SPC / 1DPC	1R 5600; 2R 5600*	* Support for DDR5-5600 with 2R is pending official enablement by Intel; the product brief lists 5200.
LGA1700 13th–14th, 2SPC	1DPC 4400; 2DPC: 1R 4000, 2R 3600	Motherboard layout and actual population are listed separately.
LGA1851 Core Ultra 200S	1DPC: UDIMM 5600; CUDIMM 6400	With 2 DIMMs/channel: 1R 4800, 2R 4400.

HOW TO APPROACH HIGH-CAPACITY CONFIGURATIONS

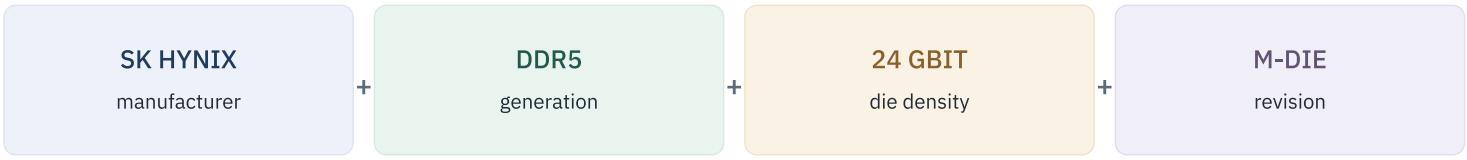
Start at more conservative MT/s, rerun memory training, and verify rank organization through the SPD. A heavier load does not by itself mean that SA, TX VDDQ, or other voltages should be raised immediately: excessive voltage can also reduce stability.

DOCUMENTATION REVIEWED: Intel EDC 743844 and 832586; Kingston 24Gbit/32Gbit guides; Micron DDR5 module features.

2.11 MANUFACTURER, DENSITY, AND REVISION

DRAM die density (also called DRAM IC density) is the amount of data stored by one die. It is specified in gigabits, such as 16, 24 or 32 Gbit. The brand on the heat spreader identifies the kit manufacturer, but the DRAM dies themselves may have been made by SK hynix, Samsung, or Micron, for example. An exact description requires four fields: manufacturer, DDR generation, density, and revision.

CORRECT NOTATION



OVERCLOCKING SHORTHAND

Abbreviation	Full notation	What matters
H16M	SK hynix DDR5 16 Gbit M-die	An early 16-Gbit die, distinct from H24M.
H16A	SK hynix DDR5 16 Gbit A-die	Another revision in the 16-Gbit family; commonly found in 2 × 16 kits.
H24M	SK hynix DDR5 24 Gbit M-die	The basis of typical 24/48 GB modules and 48/96 GB kits.
S16B	Samsung DDR5 16 Gbit B-die	A revision in the DDR5 family. Unrelated to Samsung DDR4 B-die
Micron Rev.B/D	Micron DDR5 + density + :revision	Micron uses the same letter for different densities.

HOW TO READ THE DRAM PART NUMBER

A full SK hynix code such as H5CGD8M... can be read by field: H5C indicates DDR5, GD indicates 24-Gbit density, 8 indicates x8 organization, and M indicates the die generation; the remaining suffix encodes other product parameters. Micron places the revision after a colon: for example, 16-Gbit :D and 24-Gbit :B are different products. Samsung must be tied to the full K4R... part number because the letter B appears in both DDR4 and DDR5.

The most reliable sources are the module's official datasheet and the full number printed on the DRAM IC. The SPD and utilities help, but if the exact revision cannot be determined, label it accordingly as an assumption. XMP frequency, voltage, and capacity alone do not prove the die type: the kit manufacturer may change ICs without changing the marketing name.

DIE REVISION AND PROCESS NODE

A-die, B-die, and M-die describe a revision or design generation within a manufacturer's naming scheme. 1anm, 1bnm, 1alpha, and 1beta name a process node. The letter is not an official quality grade and does not promise specific MT/s, tCL, or a permissible voltage.

HOW TO CONFIRM THE IC TYPE

Step	Source	What you can conclude
1	Module datasheet and part number	The organization and rated specification of the specific product.
2	Full DRAM IC marking + official decoder	Manufacturer, density, x8/x16 organization, and die revision.
3	SPD and diagnostic utilities	A useful clue; a clickable field in HWiNFO Memory Timings does not replace confirmation from the marking.
4	XMP bin and observed behavior	Only an indirect assumption, which must be labeled as such.

Manufacturers can use the same ICs in kits with different XMP profiles, PCBs, PMICs and voltages. The revision describes the die design; binning establishes the kit's validated operating point.

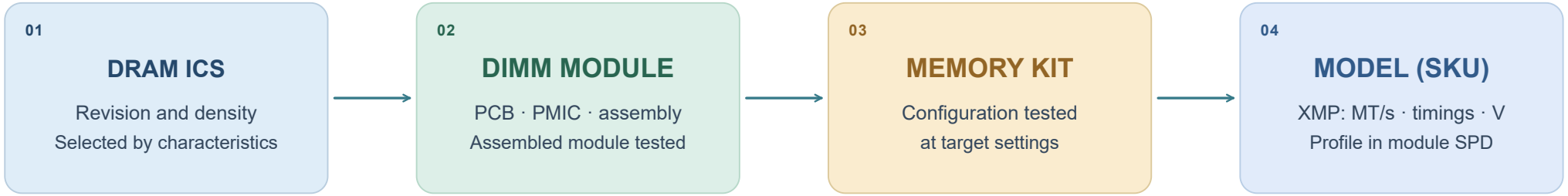
> **IMPORTANT**
>
> Always state the manufacturer, DDR5 designation, density, and revision. H16M and H24M identify different dies. Samsung DDR4 B-die and Samsung DDR5 B-die belong to different memory generations. Micron Rev.B denotes a revision; 1beta denotes a process node. **You can find details on all IC revisions in the Memory Kit Catalog's REVISION CLASSIFIER section.**

DOCUMENTATION REVIEWED: SK hynix DDR5 PN decoder and 24Gb announcement; Micron DDR5 catalog/FBGA decoder; Kingston PN decoder.

2.12 XMP BINNING AND KIT SCREENING

Binning, or screening, is the sorting of ICs and assembled modules by their ability to operate at a specified point: particular MT/s, timings, and voltage. The manufacturer validates the result and sells it as a separate SKU with a specific XMP profile.

HOW AN XMP KIT IS CREATED



HOW TO COMPARE KIT BINNING

The same H16A or H24M ICs appear in kits with different profiles. One kit is selected for frequency, another for low tCL, lower voltage or capacity. Compare them for the same task and with matching module organization.

ONE DATA RATE — DIFFERENT OPERATING POINTS

Kit	Profile	VDD/VDDQ	CAS, ns	Interpretation
2 × 16 GB	XMP 6000 36-36-36	1.35 V	12.00	Looser CL at the same MT/s.
2 × 16 GB	XMP 6000 30-36-36	1.35 V	10.00	Tighter tCL without raising V.
2 × 16 GB	XMP 6000 28-36-36	1.40 V	9.33	Lower tCL, with higher voltage.
2 × 32 GB	XMP 6000 30-36-36	1.40 V	10.00	Capacity and rank change the conditions; capacity is the main OC constraint.
2 × 24 GB [1]	EXPO 6000 28-36-36	1.35 V	9.33	H24M changes the conditions and raises OC potential.
2 × 48 GB [2]	XMP 6000 30-36-36	1.35 V	10.00	H24M changes the conditions and raises potential; capacity is the main OC constraint.
2 × 64 GB [3]	EXPO 6000 32-44-44	1.40 V	10.67	S32M changes the conditions and raises potential; higher capacity constrains OC even further.

[1] G.SKILL F5-6000J2836F24GX2-TZ5NRW

[2] G.SKILL F5-6000J3036F48GX2-TR5S

[3] G.SKILL F5-6000J3244G64GX2-TZ5NR

WHAT A LOWER PROFILE VOLTAGE TELLS YOU

With matching ICs, density, capacity, rank, PCB, frequency and timings, lower VDD/VDDQ suggests the kit needs less voltage at that operating point. The manufacturer specifies a validated voltage; testing establishes the minimum working value and OC headroom. The IMC, motherboard and cooling also affect the result. Kits are validated as a set, so mixed kits require fresh testing.

DOCUMENTATION REVIEWED: Intel XMP 3.0; G.SKILL DDR5-6000 product specifications; Kingston and Corsair materials on screened ICs.

2.13 DPC/SPC, MODULES, AND ROUTING TOPOLOGY

Desktop LGA1700 and LGA1851 platforms have two memory channels: **A and B**. First count the slots on the board, then the modules installed in each channel.

SPC — slots per channel

Slots Per Channel

1SPC: one slot in A and one in B. **2 slots** total.

2SPC: two slots each in A and B. **4 slots** total.

DPC — DIMMs per channel

DIMMs Per Channel

1DPC: one DIMM installed in each channel.

2DPC: two DIMMs installed in each channel.

2-DIMM / 4-DIMM board describes its slot count. **2 × 24 GB** means two 24 GB modules.

1R / 2R means one or two ranks in a DIMM. **1DPC 2R** means one dual-rank DIMM per channel.

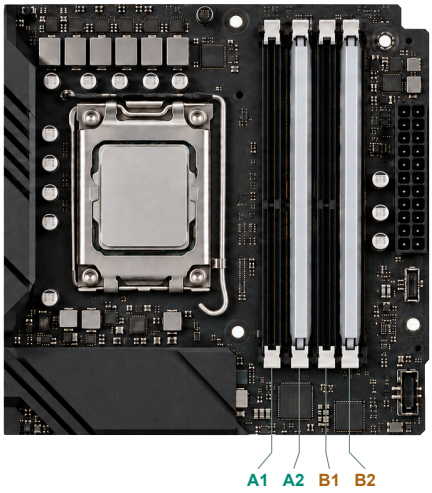
WHAT THIS LOOKS LIKE ON A BOARD

1SPC + 1DPC



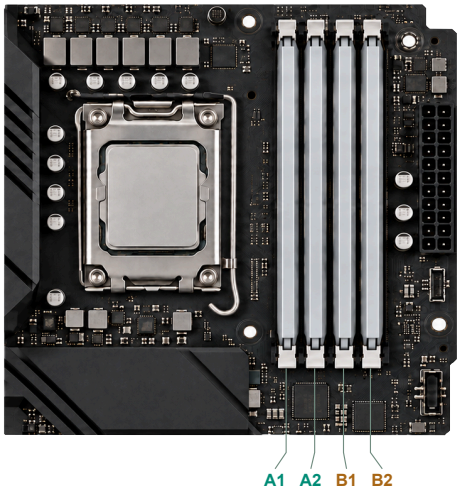
2 slots, 2 modules. One each in A and B. There is no room for four DIMMs.

2SPC + 1DPC



4 slots, 2 modules. A2 and B2 are populated; A1 and B1 are empty. The board remains 2SPC.

2SPC + 2DPC



4 slots, 4 modules. A1, A2, B1, and B2 are populated. Two DIMMs per channel.

HOW SLOTS IN ONE CHANNEL ARE CONNECTED

Daisy Chain and T-topology allow 1DPC and 2DPC. Population does not change the board's routing.

1SPC · one slot



One connector on the path. No second slot or branches to it.

2SPC · Daisy Chain



The line passes through the A1 and A2 connection points in sequence.

2SPC · T-topology



Branches of similar electrical length run from a common point to the slots.

WHAT I CHOOSE FOR OVERCLOCKING

For high frequencies, choose only **1SPC + 1DPC**: this is the most effective layout. On 2SPC boards, use only **1DPC** with two modules. Populate all four slots only when capacity takes priority over frequency.

With **2DPC**, electrical loading increases, and the data rate often has to be reduced. T-topology equalizes the paths to the slots, but retains the load of four DIMMs. The result also depends on the IMC, ranks, memory kit, and BIOS.

With three DIMMs, A and B have different populations. A/B are the platform's two channels; DDR5's 32-bit subchannels do not change this classification.

2.14 CHOOSING AN LGA1700 MOTHERBOARD: Z690 AND Z790

When choosing between Z690 and Z790 for memory overclocking, first compare physical 1SPC routing, PCB quality, BIOS/MRC, recovery features, and enthusiasts' experience. The selections below include 2-DIMM models, standard 4-DIMM Z790 boards, and expensive E-ATX flagships. Overall, 2-DIMM motherboards provide better memory training than the rest.

2-DIMM / TRUE 1SPC: MOTHERBOARDS FOR MAXIMUM FREQUENCY

Motherboard	Format	DIMMs / max., GB	Official MT/s	Practical takeaway
ASUS Z690 Apex	ATX	2 / 96	6600	Post-launch lottery: some 2021 boards could not even hold XMP-6400; good later samples reached around 7000. Buy used only after testing both DIMM slots and the BIOS.
MSI Z690 Unify-X	ATX	2 / 96	6800+	A top Z690 board: full OC/recovery features and a convenient BIOS. My findings on it are coming in the next revision.
MSI Z690I Unify	Mini-ITX	2 / 96	6800+	A very short signal path and strong memory performance; fewer POST diagnostics and bench-overclocking tools.
Gigabyte Z690 Tachyon	E-ATX	2 / 128	7000	Bench-oriented routing and a hardware OC Kit; the BIOS is designed for an experienced enthusiast.
EVGA Z690 DARK K|NGP|N	E-ATX	2 / 64	6600+	Strong hardware, but the product line is no longer being developed; buy used only with full awareness of this.
ASUS Z790 Apex, white	ATX	2 / 96	8000+	The first white revision remains top-tier: mature BIOS and a complete OC Toolkit.
ASUS Z790 Apex Encore	ATX	2 / 96	8400+	The foundation for this manual: a clear BIOS, diagnostics, recovery, and strong daily-profile potential.
ASUS Z790-AYW OC WiFi	ATX	2 / 96	8200+	An Apex alternative: good 2-DIMM routing; notably simpler power delivery, I/O, and OC/recovery features.
MSI Z790MPOWER	mATX	2 / 128	8000+	An affordable specialized 2-DIMM board; simpler and less fully equipped than flagship models.
MSI Z790I Edge WiFi	Mini-ITX	2 / 128	8000+	A strong compact option for daily use. Apex/Tachyon is preferable for test-bench overclocking.
ASRock Z790I Lightning WiFi	Mini-ITX	2 / 128	8600+	Strong 8-layer board: XMP-8000/8200 in reviews. I have reservations about ASRock/BIOS; OC/recovery is more modest than on flagships. IMC and kit determine the limit.
Gigabyte Z790 Tachyon	E-ATX	2 / 128	8333	Excellent routing and hardware switches; the BIOS requires an understanding of the settings.
EVGA Z790 DARK K|NGP|N	E-ATX	2 / 64*	8000+	A 9400 profile needs verification on the specific system; in 2026 this is more of a collectible OC platform.

EVGA: STRONG MOTHERBOARDS, BUT A POOR BUY TODAY

EVGA has released no platforms since Z790; BIOS updates are rare and some remain beta. In 2026, DARK K|NGP|N is not worth buying for a main system: it is a collectible or dedicated bench platform tied to a specific firmware.

* 64 GB according to the original EVGA specification; 96 GB confirmed by later 2 × 48 GB kits.

DOCUMENTATION REVIEWED: ASUS, MSI, Gigabyte, and EVGA specifications/QVL/BIOS; Igor'sLAB Z690 Apex batch comparison; ROG Forum; September 1, 2026. ASRock: specification and manual; independent testing by Tom's Hardware / PC Gamer. Checked September 11, 2026. G.SKILL QVL: 2 x 48 GB ASRock: specification ASRock: manual Tom's Hardware: review PC Gamer: review

4-DIMM / 2SPC: CURRENT Z790 MOTHERBOARDS FOR DAILY USE AND CAPACITY

Motherboard	DIMM / max., GB	Official MT/s	Practical significance
ASUS ROG Strix Z790-E Gaming WiFi II	4 / 256*	8000+	Useful for memory tuning: Q-Code, rear FlashBack and Clear CMOS buttons. An SSD in M.2_1 switches the GPU to x8.
ASUS TUF Gaming Z790-Pro WiFi	4 / 256*	7800+	For a daily build: four Gen4 M.2 slots without sharing GPU lanes. No FlashBack; CMOS reset uses onboard pins.
ASUS ProArt Z790-Creator WiFi	4 / 256*	7200	Choose for 10GbE and two Thunderbolt 4 ports. FlashBack is available; an SSD in M.2_4 disables SATA 5–8.
MSI PRO Z790-A MAX WiFi	4 / 256	7800+	For several SSDs: four Gen4 M.2 slots without sharing GPU lanes. Flash BIOS is available; CMOS reset uses JBAT1 pins.
MSI MAG Z790 Tomahawk MAX WiFi	4 / 256	7800+	For many SATA/USB devices and memory tuning: rear Flash BIOS and Clear CMOS buttons. An SSD in M2_1 switches the GPU to x8.
MSI MPG Z790 Edge Ti MAX WiFi	4 / 256	7800+	For five M.2 slots and rear Flash BIOS / Clear CMOS. Four Gen4 M.2 slots retain GPU x16; the fifth, M2_1, switches it to x8.
GIGABYTE Z790 AORUS PRO X	4 / 256	8266	Choose for 5GbE and five M.2 slots. An SSD in Gen5 M2C_CPU switches the GPU to x8. Q-Flash Plus; CMOS reset uses pins.
GIGABYTE Z790 AORUS ELITE X WIFI7	4 / 256	8266	For four Gen4 SSDs and Wi-Fi 7; Q-Flash Plus and a Clear CMOS button. An NVMe SSD in M2M_SB disables SATA 2/3.
GIGABYTE Z790 GAMING X AX rev. 2.1	4 / 256	7600	For a daily build with four Gen4 SSDs; Q-Flash Plus. CMOS reset uses pins; an NVMe SSD in M2M_SB disables SATA 2/3.

4-DIMM / 2SPC: E-ATX FLAGSHIPS FOR CAPACITY AND FEATURES

Motherboard	DIMMs / max., GB	Official rating	What matters for memory
ASUS Z690 Extreme	4 / 256*	6400+	Dual BIOS, Safe Boot/ReTry, ProbeIt and 10GbE for tuning. An M.2_1 SSD switches the GPU to x8.
MSI Z690 Godlike	4 / 192	6666+ 1DPC1R	10GbE, two Thunderbolt 4 ports, six M.2; dual BIOS and POST codes. An M2_3 SSD switches the GPU to x8.
ASUS Z790 Extreme	4 / 256*	7800+	Tuning and I/O: dual BIOS, Safe Boot/ReTry, ProbeIt, 10GbE. An M.2_1 SSD switches the GPU to x8.
MSI Z790 Godlike	4 / 256	7800+ 1DPC1R	Seven M.2, 10GbE, two Thunderbolt 4 ports; dual BIOS and POST codes. An M2_4 SSD switches the GPU to x8.
MSI Z790 Godlike MAX	4 / 256	7800+ 1DPC1R	Wi-Fi 7; rated 6000+ at 2DPC2R. Seven M.2, 10GbE, dual BIOS. An M2_4 SSD switches the GPU to x8.

> I do not recommend the listed flagship 4-DIMM / 2SPC boards for overclocking: a 2-DIMM / 1SPC board or a more affordable 4-DIMM board is more rational.

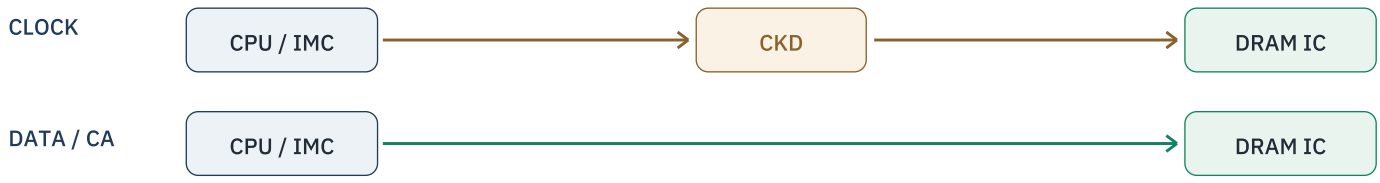
OC speed and capacity maxima are separate; the operating point depends on the CPU, BIOS and kit. GAMING X AX lists 7600 for 13th/14th-gen Core i7/i9. All three MSI QVLs for 14 Gen K list Kingston KF556C40BWAK4-128: 4 × 32 GB at 5600. * The five ASUS boards above support 256 GB with updated BIOS; their specifications still list 192 GB.

DOCUMENTATION REVIEWED: Z690/Z790 boards: exact-model specifications, manuals, QVLs and BIOS notes. ASUS Extreme: 256 GB from BIOS 3302 (Z690) / 1904 (Z790). Original reviews: 3DNews, Hardwareluxx, Igor'sLAB and Tom's Hardware; test conditions are retained in the research report. Strix E II: BIOS TUF Pro: BIOS ProArt: BIOS MSI: QVL Z690 Extreme: BIOS Z790 Extreme: BIOS

2.15 CHOOSING AN LGA1851, Z890 MOTHERBOARD

The main memory-related change in LGA1851 is official CUDIMM support. A Clocked Unbuffered DIMM remains a conventional unbuffered module for data and commands, but adds a separate Clock Driver, or CKD. It receives the clock signal, cleans it up, and reshapes it before sending it to the DRAM ICs.

WHAT EXACTLY THE CKD DOES



Data and commands are not buffered: the path remains direct

UDIMM AND CUDIMM ON CORE ULTRA 200S

Scenario	UDIMM POR	CUDIMM POR	What this means
true-1SPC / 1DPC, Core Ultra 200S	DDR5-5600	DDR5-6400	CKD enables a higher standard operating mode.
true-1SPC / 1DPC, 200S Plus	DDR5-5600	DDR5-7200	The updated IMC raises CUDIMM POR.
2SPC board, 1DPC: A2/B2 only	DDR5-5600	DDR5-5600	Even an empty second branch changes the official mode.

PRACTICAL Z890 SELECTION: OC, STANDARD 4-DIMM, AND FLAGSHIPS

Motherboard	DIMM / max., GB	Official MT/s	Practical significance
ASUS Z890 Apex	2 / 128	9600+	DIMM Fit Pro and bundled memory cooling aid tuning; Safe Boot/ReTry and Dual BIOS help recover from failed OC settings.
MSI Z890 Unify-X	2 / 128	9600+ / 7200+ 2R	An external Tuning Controller offers Safe Boot/Retry; Memory Force in BIOS and switchable Dual BIOS assist tuning.
Gigabyte Z890 Tachyon ICE	2 / 128	10400 OC	A bench/LN2 platform with a 10-layer PCB, hardware OC Kit, LIMP Mode, and DualBIOS for recovery after failed tuning.
ASRock Z890 Taichi OCF	2 / 128	12735+ 1R / 6800+ 2R (OC)	ATX for enthusiasts and bench overclocking: Retry/Safe Boot, POST codes, two selectable BIOS chips and rear Clear CMOS/Flashback make tuning and recovery from a failed profile easier.
ASRock Z890I Nova WiFi	2 / 128	9866+ 1R / 6800+ 2R (OC)	Mini-ITX for a compact two-DIMM system: 10-layer PCB and Memory OC Shield; PSC diagnostic LEDs and BIOS Flashback, with CMOS reset via onboard pins.
ASUS TUF Z890-Plus WiFi	4 / 256	9066+	Daily-use ATX: DIMM Fit, BIOS FlashBack and Q-LED diagnostics; clearing CMOS requires the onboard header.
MSI MAG Z890 Tomahawk WiFi	4 / 256	9200+ 1DPC1R	ATX for tuning: POST codes, rear Clear CMOS and Flash BIOS buttons, 5GbE networking and two Thunderbolt 4 ports.
Gigabyte Z890 Aorus Elite WiFi7	4 / 256	9200 OC	ATX with POST codes, Multi-key Safe Mode and Q-Flash Plus; its four M.2 slots do not take lanes from the GPU.
ASUS Z890 Extreme	4 / 256	9200+	E-ATX with NitroPath, Safe Boot/ReTry and dual BIOS; 10GbE, TB5 and six M.2 slots, with GPU lane sharing.
MSI Z890 Godlike	4 / 256	9200+ 1DPC1R	E-ATX: dual BIOS, diagnostic LCD, 10GbE + 5GbE; six onboard M.2 plus two on a card that shares GPU lanes.

HOW TO COMPARE ADVERTISED MAXIMUM MEMORY SPEEDS

The 10400 Tachyon ICE, 9600+ Apex/Unify-X, and 9200+ 4-DIMM results used different CPUs, modules, BIOS versions, and slot populations. Maximum capacity and maximum data rate in MT/s are separate specification targets; each has its own configuration requirements.

ASRock currently rates the OCF at 12735+ and the Nova at 9866+ for 1DPC 1R overclocking; both boards list 6800+ for 1DPC 2R. These figures do not specify a stable daily profile. Check the exact kit's QVL entry and stability with your own CPU/BIOS.

CKD BYPASS AND INTEL 200S BOOST

Both UDIMM and CUDIMM work on Z890. On some LGA1700 motherboards, CUDIMM is possible only through a BIOS-supported CKD bypass mode: the signal passes through the CKD with its PLL bypassed. Mode support and operating speed depend on the CPU, motherboard, BIOS and module. Buying CUDIMM to accelerate LGA1700 is pointless. Intel 200S Boost is a separate official OC profile, while 200S Plus refers to updated CPU models. Boost specifies memory up to DDR5-8000, NGU/D2D up to 3.2 GHz, VccSA/VDD2 up to 1.20/1.40 V, and DRAM VDD/VDDQ up to 1.40 V with one DIMM installed per channel.

MAIN TAKEAWAY FOR LGA1851

CKD expands the practical DDR5 range, but a record rated frequency still does not guarantee stable daily operation. If maximum frequency is the goal, look first at Apex, Unify-X, Taichi OCF or Tachyon ICE. Nova suits a compact two-DIMM Mini-ITX system; for high capacity, choose among the 4-DIMM models. If your tastes are unusual and you have a couple of hundred bucks to spare, choose Extreme or Godlike.

DOCUMENTATION REVIEWED: Intel EDC 832586 and 200S Boost; Z890 boards: specifications, manuals, BIOS and original tests; checked 15 Oct 2026. ASRock, checked 1 Nov 2026: OCF specifications · OC Toolkit · Nova specifications · Nova manual

2.16 MAXSUN Z690–Z890 1SPC BOARDS

Maxsun appeals to enthusiasts as a relatively budget-friendly overclocking option: two memory slots and decent features for the money. The BIOS still leaves room for improvement, especially with manual timings, as the reviews below show.

Maxsun model (MS-)	Socket / format	PCB layers	CPU VRM	Memory: claimed / tested
iCraft Z690ITX WIFI	1700 / Mini-ITX 2×DDR5	10	8+1; ISL99390, 90 A; controller*	7200 / 7400+ OC
Challenger Z690M	1700 / microATX 2×DDR4	n/a	8+1+1; SiC654, 50 A	DDR4: incompatible with DDR5
iCraft Z790ITX WIFI	1700 / Mini-ITX 2×DDR5	n/a	9 main ISL99390 stages, 90 A**	7400+ OC / 8200+ in blog; XMP-7200 tested
iCraft Z890 VERTEX	1851 / ATX 2×DDR5	8***	20+1+1; stage part numbers and ratings n/a	9200 OC; strong potential under extreme cooling
Challenger Z890M	1851 / microATX 2×DDR5	n/a	10+1+1; 60 A SPS	7200 OC; independent limit not established
Challenger Z890M WIFI	1851 / microATX 2×DDR5	n/a	10+1+1; 60 A SPS	7200 OC; independent limit not established
Challenger Z890M WIFI ICE	1851 / microATX 2×DDR5	n/a	10+1+1; 60 A SPS	7200 OC; independent limit not established

PCB: printed circuit board; n/a: unconfirmed; OC: overclocking; data rates in MT/s. VRM layouts follow manufacturer/teardown data. An SPS current rating does not specify the current capability of the whole board.

* Z690ITX: RAA229131 in the product listing, RAA229132 in the teardown. ** Not all nine stages supply Vcore. *** Low-loss PCB material and back-drilling (removal of unused plated via stubs).

Z790ITX WIFI: a budget option for LGA1700

Tom's Hardware (2023): i9-13900K, BIOS H5.3G, TeamGroup XMP-7200 worked without issues. i2HARD (2023) reached 7200 with an i9-13900KF, H4.2G and 2×16 GB Patriot 5600, but CL rose to 58 because manual timings were applied incorrectly. H7.4G included timing optimizations. The early review does not tell us how newer firmware behaves. I would consider it for a 7200 MT/s target; the advertised 8200 MT/s requires separate verification.

Z890 VERTEX: the main candidate for high data rates

Overclocking.com (2025) used an Ultra 7 265K and 2×24 GB G.Skill with Hynix M. Results: 8800 CL36 with ambient memory cooling and extreme CPU cooling; 9400 CL36 at roughly -70 °C on the memory in y-cruncher 2.5B; 9494 CL36 in 7-Zip. 11200 was a separate bench. There is potential, but the daily-use ceiling remains unproven; the reviewer missed Safe Boot/Retry for quick recovery after a failed boot.

NEWLY SHOWN BOARDS: KEEP THESE SEPARATE FOR NOW

iCraft Z890 VERTEX PRO	Computex 2026: 2×DDR5, 20+1+1; reported as microATX. A completed 3DMark benchmark records 2×24 GB at 9066 MT/s.
iCraft Z890ITX WIFI	MAXSUN's exhibition placard lists Mini-ITX, 2×DDR5, dual-channel operation (1SPC), and an 8+1+1 power design.
Terminator Z890M WIFI GKD5	MAXSUN's launch presentation showed a microATX board with two DDR5 slots. Retail-version specifications remain unconfirmed.

Choose by test results and BIOS behavior. Two slots and good routing help overclocking; the achieved frequency also depends on the IMC and kit and requires stability testing.

i2HARD: Z790ITX Tom’s Hardware: XMP-7200 Maxsun: BIOS Z790ITX VERTEX: conditions and results VERTEX: limitations PRO: 3DMark

2.17 MOTHERBOARD CLASSIFICATION

SPC means slots per channel. Population lists the supported numbers of DIMMs per channel (DPC).

Channels A/B follow the board manual; DDR5 subchannels are not counted separately here.

Board names link to specifications; confirmed topology labels link to their sources.

> T-Topology is used for motherboard memory routing and has confirmed implementations in previous DDR generations. No reliably confirmed T-Topology implementations have been established for the production DDR5 boards examined here.

Model	Slots	SPC	Population	Topology
ASUS ProArt Z890-Creator WiFi	4	2SPC	1DPC / 2DPC	Unconfirmed
ASUS ROG Maximus Z690 Apex	2	1SPC	1DPC	Point-to-point
ASUS ROG Maximus Z690 Extreme	4	2SPC	1DPC / 2DPC	Unconfirmed
ASUS ROG Maximus Z790 Apex	2	1SPC	1DPC	Point-to-point
ASUS ROG Maximus Z790 Apex Encore	2	1SPC	1DPC	Point-to-point
ASUS ROG Maximus Z790 Extreme	4	2SPC	1DPC / 2DPC	Unconfirmed
ASUS ROG Maximus Z890 Apex	2	1SPC	1DPC	Point-to-point
ASUS ROG Maximus Z890 Extreme	4	2SPC	1DPC / 2DPC	Unconfirmed
ASUS ROG Strix Z790-E Gaming WiFi II	4	2SPC	1DPC / 2DPC	Unconfirmed
ASUS ROG Strix Z890-I Gaming WiFi	2	1SPC	1DPC	Point-to-point
ASUS TUF Gaming Z890-Plus WiFi	4	2SPC	1DPC / 2DPC	Unconfirmed

Model	Slots	SPC	Population	Topology
ASUS Z790-AYW OC WiFi	2	1SPC	1DPC	Point-to-point
MSI MAG B860 Tomahawk WiFi	4	2SPC	1DPC / 2DPC	Unconfirmed
MSI MAG Z790 Tomahawk MAX WiFi	4	2SPC	1DPC / 2DPC	Unconfirmed
MSI MAG Z890 Tomahawk WiFi	4	2SPC	1DPC / 2DPC	Unconfirmed
MSI MEG Z690 Godlike	4	2SPC	1DPC / 2DPC	Unconfirmed
MSI MEG Z690 Unify-X	2	1SPC	1DPC	Point-to-point
MSI MEG Z690I Unify	2	1SPC	1DPC	Point-to-point
MSI MEG Z790 Godlike	4	2SPC	1DPC / 2DPC	Unconfirmed
MSI MEG Z790 Godlike MAX	4	2SPC	1DPC / 2DPC	Unconfirmed
MSI MEG Z890 Godlike	4	2SPC	1DPC / 2DPC	Unconfirmed
MSI MEG Z890 Unify-X	2	1SPC	1DPC	Point-to-point
MSI MPG Z790I Edge WiFi	2	1SPC	1DPC	Point-to-point
MSI Z790MPOWER	2	1SPC	1DPC	Point-to-point
GIGABYTE Z690 AORUS TACHYON	2	1SPC	1DPC	Point-to-point*
GIGABYTE Z790 AORUS MASTER X	4	2SPC	1DPC / 2DPC	Daisy Chain
GIGABYTE Z790 AORUS PRO X	4	2SPC	1DPC / 2DPC	Daisy Chain
GIGABYTE Z790 AORUS TACHYON	2	1SPC	1DPC	Point-to-point*
GIGABYTE Z890 AORUS ELITE WIFI7	4	2SPC	1DPC / 2DPC	Daisy Chain
GIGABYTE Z890 AORUS MASTER	4	2SPC	1DPC / 2DPC	Daisy Chain
GIGABYTE Z890 AORUS TACHYON ICE	2	1SPC	1DPC	Point-to-point
ASRock Z790 Taichi Lite	4	2SPC	1DPC / 2DPC	Unconfirmed
ASRock Z790I Lightning WiFi	2	1SPC	1DPC	Point-to-point
ASRock Z890 Taichi OCF	2	1SPC	1DPC	Point-to-point
ASRock Z890I Nova WiFi	2	1SPC	1DPC	Point-to-point
EVGA Z690 DARK K|NGP|N	2	1SPC	1DPC	Point-to-point
EVGA Z790 DARK K|NGP|N	2	1SPC	1DPC	Point-to-point
Maxsun Challenger Z690M · DDR4	2	1SPC	1DPC	Point-to-point
Maxsun Challenger Z890M	2	1SPC	1DPC	Point-to-point
Maxsun Challenger Z890M WIFI	2	1SPC	1DPC	Point-to-point
Maxsun Challenger Z890M WIFI ICE	2	1SPC	1DPC	Point-to-point
Maxsun iCraft Z690ITX WIFI	2	1SPC	1DPC	Point-to-point
Maxsun iCraft Z790ITX WIFI	2	1SPC	1DPC	Point-to-point

Model	Slots	SPC	Population	Topology
Maxsun iCraft Z890 VERTEX	2	1SPC	1DPC	Point-to-point
Maxsun iCraft Z890 VERTEX PRO (announced)	2	n/a	n/a	Unconfirmed
Maxsun iCraft Z890ITX WIFI (announced)	2	1SPC	1DPC	Point-to-point
Maxsun Terminator Z890-A WIFI	4	2SPC	1DPC / 2DPC	Daisy Chain
Maxsun Terminator Z890M WIFI GKD5 (announced)	2	n/a	n/a	Unconfirmed

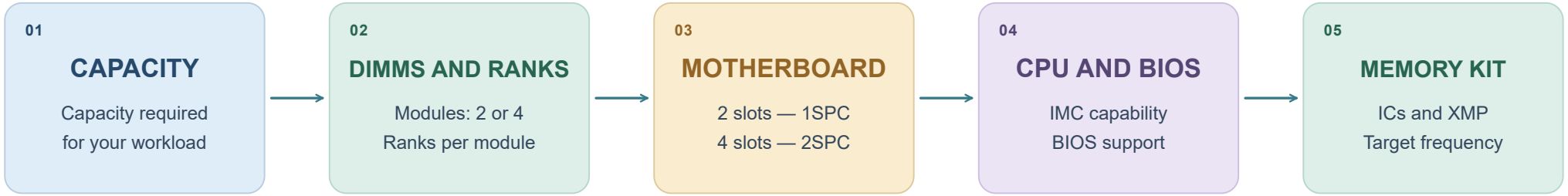
Point-to-point means the controller connects to the sole socket in a channel: a structural classification based on board documentation.

* GIGABYTE calls the Z690/Z790 Tachyon layout “2-DIMM daisy chain”; this table classifies them as Point-to-point by the number of sockets in each channel.

2.18 PRACTICAL PLATFORM AND KIT SELECTION

Start with the required capacity. Capacity determines module and rank count, which in turn determines the appropriate motherboard topology. Only then does it make sense to choose a CPU, specific IC, and realistic frequency target.

DECISION ORDER



TYPICAL SCENARIOS

Goal	Kit	Motherboard	Realistic approach
Maximum frequency	2×16 / 2×24	2-DIMM true-1SPC	Best chance of high MT/s; capacity is fixed in advance.
Balanced profile	2×16 / 2×24 / 2×32	High-quality 2- or 4-DIMM board	On a 4-DIMM board, use A2/B2 and do not chase records.
96–128 GB	2×48 / 2×64	QVL + current BIOS	Density, rank, and training matter more than an impressive XMP profile.
Four modules	one matched 4-DIMM kit	4-DIMM motherboard	Expect lower MT/s from the outset; for four modules, choose a single K4 kit.
Future upgrade	final capacity now	according to task priority	Buying a second kit later does not guarantee that both kits will work together without additional tuning.

PROCESSOR

For full manual control, choose an unlocked K/KF processor and a Z-series motherboard. The individual IMC sample remains a lottery: a more expensive CPU model does not promise a stronger controller. On LGA1851, Intel 200S Boost also requires a suitable K/KF processor, motherboard, and BIOS.

MOTHERBOARD

For maximum frequency with two modules, choose a true 1SPC OC motherboard. For high capacity and flexibility, choose four slots while accepting a lower ceiling when fully populated. The Z790 Apex Encore is officially limited to 96 GB. Yet BIOS 0904, dated February 16, 2024, promises “Enhanced compatibility with 256GB memory.” The devs must have been smoking some good stuff when they rolled out this BIOS. So 128–192 GB on LGA1700 requires another motherboard. Check the QVL for the exact model, the current BIOS, CUDIMM support and available features

MEMORY KIT

Buy one matched kit with the final capacity you need. Check the part number, number of DIMMs, rank, die density, XMP voltage, and presence of a temperature sensor. Intel does not officially specify more than 192 GB for LGA1700 even if an individual motherboard lists 256 GB support; for LGA1851, the current Core Ultra 200S ARK already specifies up to 256 GB. In practice, the final limit is determined by the combination of CPU, motherboard, BIOS version, and specific memory kit.

> ### FORMULA FOR A RATIONAL PURCHASE
>
> Capacity → number of DIMMs and ranks → motherboard topology → CPU and BIOS → IC and XMP. Changing this order makes it easy to buy an impressive profile that does not match the actual load or platform capabilities.

DOCUMENTATION REVIEWED: Current Intel ARK and memory support matrices; ASUS/MSI specifications and QVLs; Kingston guidance on matched kits.

03 / Timings

2.2 / Gear Mode and Command Rate →

3.1 Reading timings

A timing specifies the duration of an operation or the interval between memory events. Most timings specify a minimum interval. tREFI has a different role: it limits the maximum average interval between refresh commands.

BIOS values usually use memory clock cycles, CK: tCL = 36 means 36 cycles. Their duration depends on the data rate.

Converting to nanoseconds

DDR transfers data twice per clock cycle. Use these formulas:

tCK (ns) = 2000 / R

t (ns) = N × 2000 / R

R is the data rate in MT/s; N is the timing value in clock cycles.

Data rate	One clock cycle, tCK	Time at tCL = 36
DDR5-6000	0.333 ns	12.00 ns
DDR5-8000	0.250 ns	9.00 ns
DDR5-8200	0.244 ns	8.78 ns
DDR5-9000	0.222 ns	8.00 ns

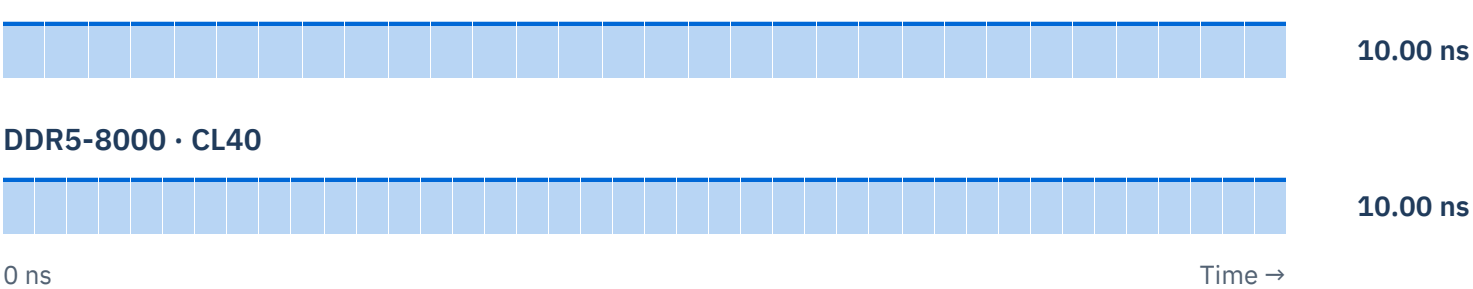
For the same cycle count, a higher data rate gives a shorter duration in nanoseconds.

Comparing values

Different CL values can represent the same amount of time:

Different CL, equal time

One segment = one CK cycle



This equality applies only to the CAS component of latency. Total access latency also depends on other timings and the controller. Compare the duration of a particular timing in nanoseconds, and compare complete memory profiles using measurements on the full system.

The following sections group timings into primary, secondary, and tertiary parameters. Section 3.2 explains where each part of the delay occurs.

DOCUMENTATION: Kingston — MT/s vs MHz; Kingston — CAS Latency Explained; SK hynix DDR5 32Gb M-die · §4.13

3.2 The command path: where latency comes from

To access data, the required row must be open in its bank. ACT starts opening the row; READ and WRITE access its data; PRE closes the row and prepares the bank for another activation. While the required row stays open, ACT does not need to be repeated before every access.

READING: ONE TARGET, THREE PATHS

All three scenarios read row B in the same bank. Only the initial state changes: row B is already open, the bank is closed, or row A is open.

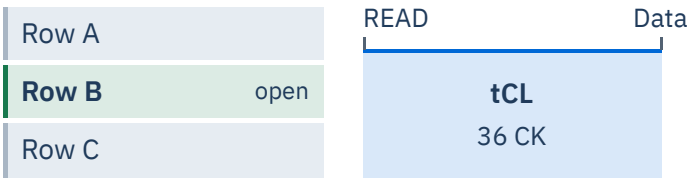
Reading row B in one bank

DDR5-8200 · tCL 36 · tRCDRD 49 · tRP 49

PRE · close A **ACT** · open B **READ** · read B

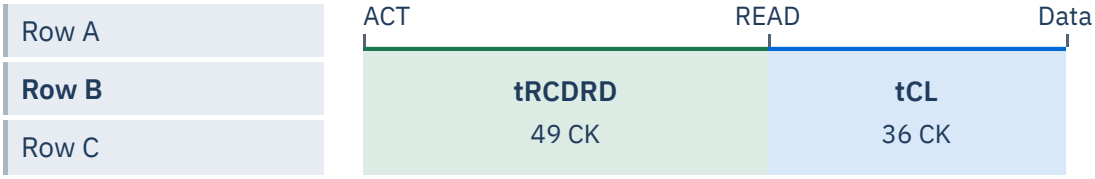
Target row already open 36 CK · 8.78 ns

Bank 0 · before READ



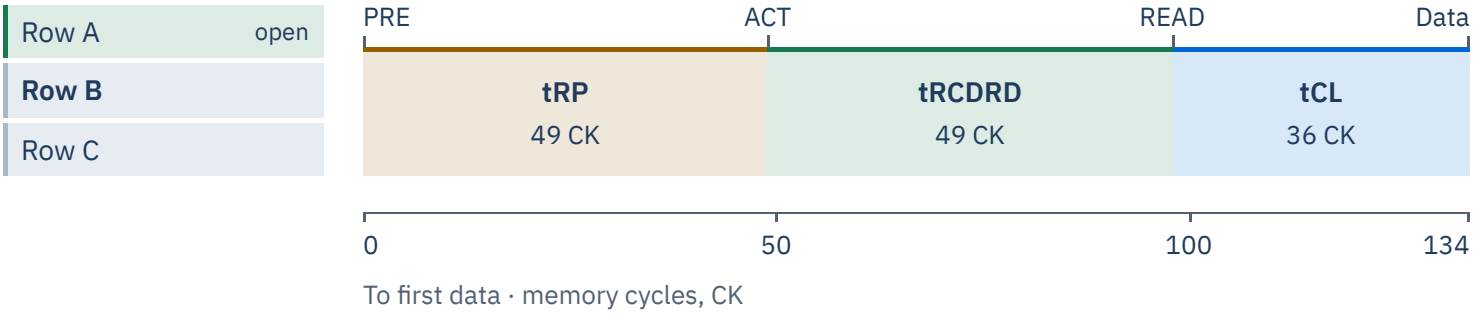
Bank closed 85 CK · 20.73 ns

Bank 0 · before ACT



Another row is open 134 CK · 32.68 ns

Bank 0 · before PRE



To first data · memory cycles, CK

The tCL segment is identical in all three cases. Opening a row adds tRCDRD; replacing an already open row adds tRP as well. The total path therefore depends on the operations required before READ.

Each bar ends at the first data. Time is measured from the first command that is already permitted: READ, ACT, or PRE. Any preceding wait and the controller's request queue are excluded from these illustrative totals.

WRITING: FIRST DATA AND END OF BURST

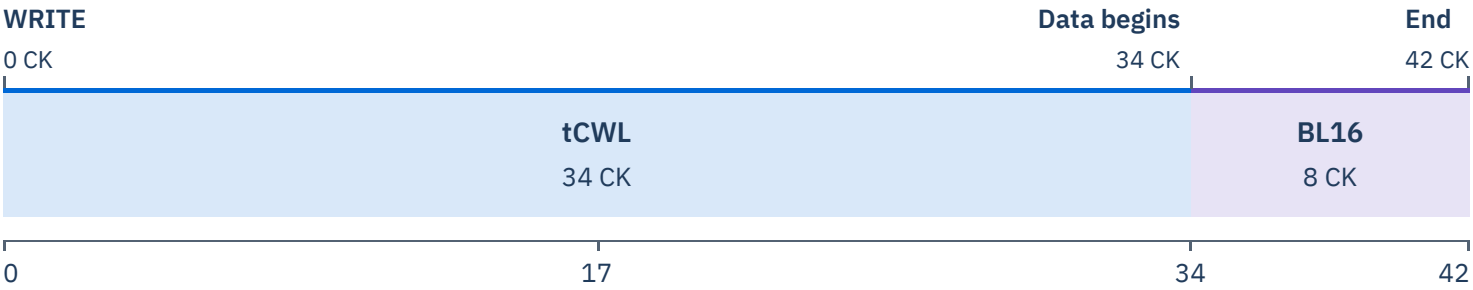
For a closed bank that is ready for ACT, first open the row and issue WRITE:

ACT → tRCDWR → WRITE

After WRITE, tCWL elapses before write data begins. A BL16 burst transfers 16 data beats over 8 CK. The following diagram starts at the WRITE command.

After the WRITE command

Example: tCWL 34 · BL16, CRC off



From WRITE · memory cycles, CK

BL16 enlarged: two data beats per cycle



Cycle within the BL16 burst

The end of the burst is a separate reference point for write recovery. Before PRE can be issued, both tWR and the tRAS requirement must be satisfied. These conditions are explained in section 3.6.

WHAT EACH SETTING CHANGES

- Lowering tCL reduces the wait after READ in all three read paths.
- Lowering tRCDRD reduces the interval between ACT and READ when a row must be opened.
- Lowering tRP reduces the preparation time between PRE and the next ACT when switching rows.
- Lowering tCWL reduces the interval between WRITE and the start of write data.

Total system latency also includes CPU and controller processing and the wait for a request to be serviced. These sequences show which part of an access each timing changes.

3.3 Primary timings

Primary timings determine when a row can be opened, its data accessed, and the bank prepared for another activation. Each value applies to a specific part of that sequence.

PURPOSE AND ADJUSTMENT

Timing	Interval	Tuning practice
tCL	**READ → first data.** In nanoseconds: tCL × 2000 / MT/s.	Reduce it in steps of **2 CK**: the ASUS BIOS versions considered here round odd values up. For H16A, use 32 as a starting point, with a more aggressive reduction to 30; for H24M, start at 36 or higher.
tRCDRD	**ACT → READ:** preparing the newly opened row for reading.	Tune separately after tCL; at high data rates it often reaches its limit sooner.
tRCDWR*	**ACT → WRITE.** From ACT to the first write data: tRCDWR + tCWL.	Start with the tRCDRD value; independent adjustment depends on the platform.
tRP	**PRE → next ACT:** closing the row and preparing the bank.	Reduce separately; frequent row changes can expose errors. Start with 12 or 14 for high data rates above 8200 MT/s.
tRAS	**ACT → permitted PRE:** the minimum time a row must remain open.	For an early READ, use tRCDRD + tRTP as a starting point; see below.
tRC	**ACT → next ACT in the same bank.**	The calculated baseline for this platform is tRAS + tRP. The actual interval can be longer.
CR	The command transmission mode on the command bus.	**1N** is not available in every configuration: support and actual use depend on the platform and BIOS. For the high data rates considered here, **2N** is the working baseline.

* The controller and BIOS/MRC may couple or normalize tRCDRD and tRCDWR in a particular mode. A universal requirement for equality across all platforms has not been established; separate BIOS fields alone do not guarantee independent control.

THE RELATIONSHIP BETWEEN tCL, tRCD, AND tRP

The primary timing order is tCL–tRCD–tRP–tRAS; three-value notation omits tRAS.

Example	Primary timings	tRCD / tRP minus tCL
DDR4 B-die	**14-14-14-34**	0 / 0
DDR5-5600 JEDEC	**46-45-45**	−1 / −1
DDR5-8000 XMP	**38-48-48**	+10 / +10
DDR5-8400 XMP	**40-52-52**	+12 / +12
Author's 8200 baseline	**36-49-49-61**	+13 / +13

DDR4 B-die is known for equal first three timings; tRAS was tuned separately. With DDR5, the difference varies between profiles. For example, in standard DDR5-5600 JEDEC, tCL is one cycle higher than tRCD and tRP.

On high-speed DDR5 with selected ICs, a gap of around 8–13 CK occurs in XMP profiles and overclocking. Lowering tCL reduces the wait after READ; tRCDRD determines the time needed to prepare a row for reading. On Hynix DDR5 above roughly 7600 MT/s, tCL is also difficult to reduce below 36: doing so requires a very large VDD increase. tRCD/tRP also reach their own limits. My baseline primary timings are 36-49-49-61. In the relationship “tRCD = tCL + X”, X depends on the profile.

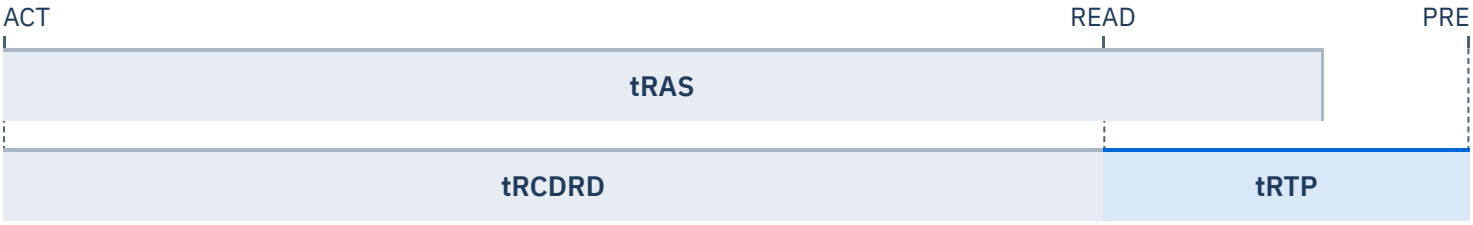
CLOSING A ROW AND CYCLING A BANK: tRAS, tRTP, AND tRC

Before PRE, both intervals must have elapsed: tRAS from ACT and tRTP from READ. If READ is issued as soon as tRCDRD allows, these constraints give the following lower bound for the bank cycle:

$$T_{ACT \to ACT} \geq \max(tRAS, tRCDRD + tRTP) + tRP$$

Two waits before PRE

tRAS ends first · schematic scale



PRE waits for tRTP

For the 8200 36-49-49-61 baseline with tRTP = 12 CK:

- Reading from a closed bank: tRCDRD + tCL = 49 + 36 = 85 CK.
- Switching rows before a read: tRP + tRCDRD + tCL = 49 + 49 + 36 = 134 CK.
- tRAS baseline: 49 + 12 = 61 CK.
- Calculated tRC: 61 + 49 = 110 CK.

Lowering tRAS below 61 does not shorten this particular path: PRE still waits for tRTP. A later READ or other constraints can lengthen the cycle, and the tRC requirement must also be met. The formula describes command intervals; the stability of the chosen values must be tested separately.

The 85 and 134 CK totals start at an already permitted ACT/PRE and end at the first data. They exclude waiting in the controller's request queue.

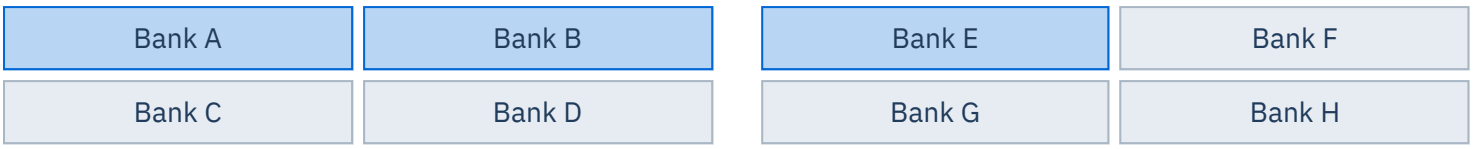
DOCUMENTATION: Samsung DDR4 8Gb B-die: datasheet; SK hynix DDR5: READ/PRE and bank cycle; ASUS: BIOS manual; Intel: ACT/PRE registers; Kingston, G.SKILL, TeamGroup: XMP specifications.

3.4 Secondary timings: activation and bank groups

DDR5 banks are arranged in groups. Commands to different groups usually require shorter gaps because fewer internal resources conflict.

For tRRD, S (Short) applies to different bank groups and L (Long) to different banks in the same group. In Intel tertiary timings, dg (Different Group) and sg (Same Group) describe the corresponding transition topology. For tCCD, the applicable constraints also depend on the speed grade and DRAM organization.

Same group and different groups



A → B · sg

Same group

A → E · dg

Different groups

Row activation: tRRD and tFAW

Timing	Constraint	Specification and tuning
tRRD_S	ACT → ACT across different groups.	For x8 devices with a 1 KB page, at least **8 CK**. I use **8** for all kits in this manual.
tRRD_L	ACT → ACT to different banks in the same group.	At least **8 CK** and the time minimum for the speed grade. Tune after S; L is usually no lower than S. Use +2–4 from tRRD_S as a starting point: tRRD_L = tRRD_S + 2|4.
tFAW*	Interval from the first to the fifth command in any five consecutive ACTs to one rank.	For x8, at least **32 CK** and the time minimum for the speed grade. My profile uses **32** as a working OC setting.

* See 3.5 for details.

With tRRD_S = 8 and tFAW = 32 on x8, ACT commands can occur at 0, 8, 16, 24, and 32 CK, provided the bank/group sequence and all other timing requirements permit it. tFAW above 32 further limits the activation rate.

For x16 with a 2 KB page, the tFAW cycle limit is 40 CK; the time minimum depends on the datasheet and speed grade. Server 3DS memory has additional constraints.

Read and write intervals: tCCD

For BL16 with CRC disabled:

Timing	Constraint	Specification and BIOS relationship
tCCD_S / tCCD_S_WR	READ → READ / WRITE → WRITE across different bank groups.	**BL16 / 2 = 8 CK**. The basis for **tRDRD_dg / tWRWR_dg**.
tCCD_L	READ → READ on the long path within a group; when tCCD_M is defined, L applies to the same bank.	At least **8 CK and 5 ns**. Related to **tRDRD_sg**; ASUS Z890 also exposes a separate field.
tCCD_L_WR	WRITE → WRITE on the long path within a group; when tCCD_M_WR is defined, L applies to the same bank. **The second WRITE requires RMW**.	At least **32 CK and 20 ns**. ASUS Z890 exposes a separate field.
tCCD_L_WR2	WRITE → WRITE within a group when **the second WRITE does not require RMW**.	At least **16 CK and 10 ns**. A separate device requirement; the BIOS may not expose a separate field.

The SK hynix table for DDR5-8000–8800 also specifies tCCD_M, tCCD_M_WR, and tCCD_M_WTR for different banks in the same group. Controller sg must therefore not be treated as a universal synonym for one DRAM L parameter. The L minimums above apply to the path specified by the datasheet; check the particular DRAM datasheet to determine whether M applies.

DOCUMENTATION: Samsung, SK hynix, Micron DDR5 x8/x16: timing tables; Intel: ACT registers; ASUS ROG Z890: BIOS manual.

3.5 tFAW: WHY 32/40 IS THE BASELINE

tFAW specifies the minimum time from the first to the fifth ACT command within one rank. The check repeats for every new command: ACT5 is compared with ACT1, ACT6 with ACT2, and so on. tRRD must also be met between adjacent ACT commands.

tFAW DEPENDENCE ON SPEED BIN

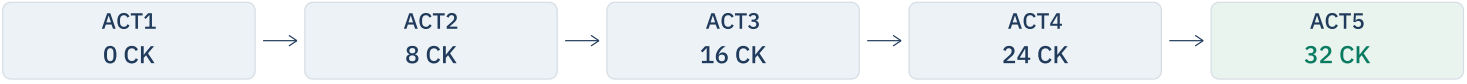
The tFAW minimum is specified simultaneously in CK cycles and nanoseconds. Both limits come from the table for the required DRAM organization and speed bin. One limit cannot be applied to all DDR5: the time component changes between bins, while the cycle component also depends on device organization.

The table contains selected speed bins for SK hynix 32 Gbit M-die, x8, with a 1 KB page. Minimums come from the datasheet. The green 8200 row is my OC profile: it lists the 32 CK setting and its time calculated from frequency.

Data rate, MT/s	tFAW, CK	Time, ns
5600	32 - minimum	11.428 - minimum
6000	32 - minimum	10.666 - minimum
6400	32 - minimum	10 - minimum
8000	32 - minimum	8 - minimum
8200 (my OC)	32 - setting	≈ 7.805 - calculated
8400	32 - minimum	7.619 - minimum
8800	32 - minimum	7.272 - minimum

WHY THE PRACTICAL MINIMUM FOR x8 IS 32 CK

tFAW (Four Activate Window) permits no more than four ACTIVATE commands within one rank in its window. tRRD_S specifies the interval between adjacent ACT commands to different bank groups. For standard DDR5 x8 with a **1 KB** page, the minimum limit considered here is **tRRD_S = 8 CK**.



There are four intervals between ACT1 and ACT5: **4 x tRRD_S = 4 x 8 = 32 CK**. tRRD_S prevents ACT5 from being issued earlier; the figure shows the densest possible ACT sequence while meeting the other constraints.

> tFAW_effective(min) ≈ 4 x tRRD_S; with tRRD_S = **8 CK**:
>
> tFAW_effective(min) = **32 CK**

Estimated ACT-command density at the specified tRRD_S.

PAGE SIZE: WHY THE LIMIT FOR x16 IS 40 CK

DDR5 x4/x8 uses a **1 KB** page; x16 uses **2 KB**. For x16, the cycle-based tFAW minimum is **40 CK** even though tRRD_S may also be **8 CK**: 4 x 8 = 32 CK. The value 40 is not derived from 4 x tRRD_S: the larger activated page requires a stricter window for a series of ACT commands and a tighter peak-load limit. tFAW is the constraint here: ACT5 can occur no earlier than **40 CK**, not 32 CK.

For details on x4/x8/x16 device organization, see Chapter 2.7

JEDEC: BOTH CK AND NANOSECONDS COUNT

> **tFAW: 1 KB - the greater of 32 CK and the ns minimum; 2 KB - 40 CK and the ns minimum.**

Here nCK is the duration of the stated number of cycles: times are compared. **32/40 CK** are cycle limits; the minimum in ns comes from the specific IC and speed bin, so the final value is not always equal to 32/40 CK.

> **PRACTICAL TAKEAWAY**
>
> For standard DDR5 x8 with tRRD_S = **8 CK**, tFAW = **32 CK** is the effective lower limit. This follows from tFAW and tRRD_S working together: lowering tFAW alone below 32 CK does not increase ACT command density.

DOCUMENTATION REVIEWED: SK hynix DDR5 SDRAM 32Gb M-die, Rev. 1.2 (07.2025), AC timing tables; Micron DDR5 SDRAM Core, Rev. E (11.2024), AC timing tables. **SK hynix 32Gb M-die · Rev. 1.2 · July 2025**, **Micron · DDR5 SDRAM Core**

3.6 Secondary timings: reads, writes, and recovery

My profile: ASUS ROG Maximus Z790 Apex Encore, DDR5-8200, Gear 2. All values below are in memory clock cycles.

tCL and tRTP — reading and closing a row

tCL sets the delay from the READ command to the first data; tRTP is the minimum interval from READ to the start of row closure with PRE.

In my overclocking profile, tRTP = 12; at high data rates, I use 14. I do not go below 12.

tCWL — write latency

tCWL sets the delay from the WRITE command to the start of write data transfer. At the DRAM level:

tCWL = tCL − 2

With tCL = 36, we use tCWL = 34.

tWR — recovery after writing

tWR sets the recovery time that must elapse after write data transfer ends before the row can begin to close.

In this manual's overclocking profile, we set tWR = 48 and do not reduce it further.

tWTR_S and tWTR_L — switching from writing to reading

tWTR sets the wait from the end of write data transfer to a subsequent READ command. tWTR_S applies across different bank groups and is linked to tWRRD_dg; tWTR_L applies within the same bank group and is linked to tWRRD_sg.

The base calculation relationships for this Intel DDR5 platform are:

tWTR_L = tWRRD_sg – tCWL – 10

tWTR_S = tWRRD_dg – tCWL – 10

Base calculation:

tWTR_L: 62 – 34 – 10 = 18; tWTR_S: 52 – 34 – 10 = 8.

The profile shown uses tWRRD_sg = 62 and tWRRD_dg = 52. With tCWL and all other settings fixed, changing the corresponding tWRRD by one cycle changes the calculated tWTR by one cycle in the same direction. After changing tCWL, recheck the linked tWRRD pair.

> Note. ATC 4.1.7 displays this profile as tWTR_L = 22 and tWTR_S = 12. To reproduce the settings, use the specified tWRRD pair; the displayed tWTR values depend on the calculation used.

After changing the settings, test memory using this manual's methodology.

Definitions, practical tertiary timing adjustments, and the relationship between tWRRD_sg/dg and tWTR_L/S are explained in section 3.8. For the compact formulas, see chapter 11.

DOCUMENTATION REVIEWED: Intel Core 13th Gen, Vol. 2; ADATA DDR5 U-DIMM; pyhwinfo: memory.py

3.7 Secondary timings: refreshing data

DRAM cells gradually lose electrical charge. To retain their data, the memory periodically performs refresh.

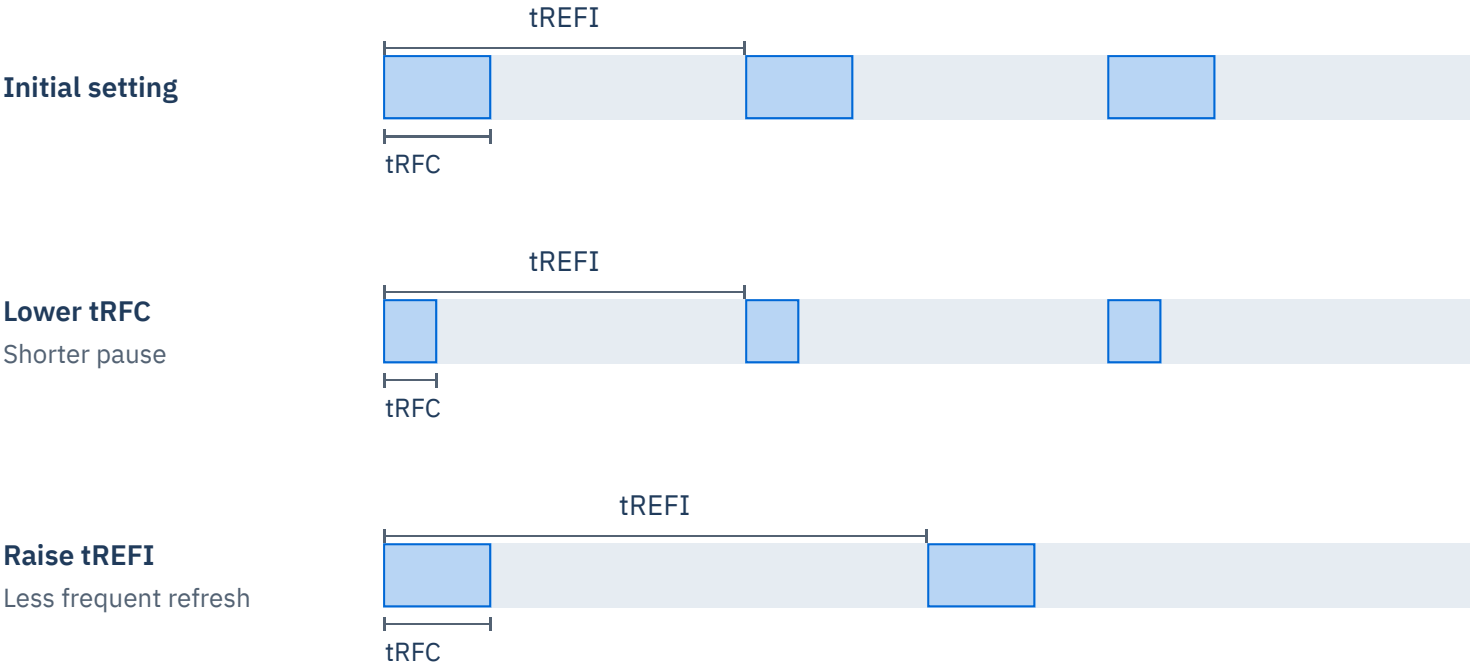
Two quantities must be distinguished:

- tRFC is the pause after a refresh command. The affected banks are busy refreshing during this interval.
- tREFI is the maximum average interval between refresh commands for the selected mode. It determines how often refresh is required.

Lowering tRFC shortens the pause enforced by the controller. Raising tREFI makes refresh less frequent. Both changes can reduce time spent servicing refresh, but require stability testing, especially after the memory has warmed up.

What tRFC and tREFI change

Schematic scale · REFab



Refresh commands are evenly spaced in this illustration. In practice, the controller may move individual commands within the permitted scheduling limits: tREFI specifies an average interval, not a mandatory spacing between every adjacent pair. The illustrated pause applies to the banks affected by refresh.

Refresh timings and modes

DDR5 has two refresh commands: REFab and REFsb. REFab affects all banks in a device. REFsb affects the selected bank number in every bank group and is used in Fine Granularity Refresh (FGR) mode.

Timing	Meaning	What to keep in mind
tRFC1	Pause after REFab in Normal Refresh mode.	The all-bank refresh requirement in Normal mode.
tRFC2	Pause after REFab in FGR mode.	Refresh occurs more often, with a shorter individual pause. tRFC2 has its own requirement; it cannot be obtained by simply halving tRFC1.
tRFCsb	Refresh pause for the selected banks after REFsb.	The same bank number is refreshed in every group. Other banks may serve accesses subject to the command-spacing requirements.
tREFI	Maximum average interval between refresh commands.	The allowed interval depends on mode and temperature. A higher value makes refresh less frequent.

DDR5 device documentation defines these timings and their relationship to the refresh mode.

Which banks are refreshing

Example device: 8 groups of 4 banks

REFab · all banks

Normal or FGR

BG0	BG1	BG2	BG3	BG4	BG5	BG6	BG7
0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1
2	2	2	2	2	2	2	2
3	3	3	3	3	3	3	3

REFsb · bank 1 in every group

FGR only

BG0	BG1	BG2	BG3	BG4	BG5	BG6	BG7
0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1
2	2	2	2	2	2	2	2
3	3	3	3	3	3	3	3

Affected by refresh Other banks

The REFsb example selects bank 1 in every group. Subsequent refresh commands may select other bank numbers. A single refresh command refreshes the portion of rows selected by the device's internal refresh mechanism; it does not refresh the entire memory contents at once.

Specification names and BIOS fields can differ. The presence of a tRFC2 field alone does not establish that FGR is enabled. Consider the active mode and the values actually applied; the mapping between tRFCsb and controller fields also depends on the platform.

Reference tRFC values

The specified refresh duration depends on the density of each DRAM die. The table uses gigabits per die, not gigabytes per module.

Minimum values from manufacturer tables:

Die density	tRFC1 — Normal	tRFC2 — FGR	tRFCsb — REFsb
8 Gbit	195 ns	130 ns	115 ns
16 Gbit	295 ns	160 ns	130 ns
24 / 32 Gbit	410 ns	220 ns	190 ns

These are reference requirements for the corresponding modes. Lower tRFC overclocking settings must be tested on the particular kit. For non-binary M-die modules at 8200 MT/s and above, the working range is 688–720 CK; A-die can run substantially lower.

Different rounding directions apply when converting time to cycles:

Parameter	Conversion to cycles	Rounding
tRFC	tRFC (ns) × R / 2000	Up, so the pause is not shorter than the chosen time.
tREFI	tREFI (µs) × R / 2	Down, so the interval does not exceed the chosen time.

R is the data rate in MT/s: use 8200 for DDR5-8200. See Formulas for the conversions.

How temperature changes the refresh interval

At higher temperatures, memory requires more frequent refresh, so the maximum average interval decreases.

The following requirements apply to REFab. TCASE is the case temperature of the DRAM device itself.

DRAM case temperature, TCASE	Normal mode — tREFI1	FGR mode — tREFI2
0 ≤ TCASE ≤ 85 °C	3.9 µs	1.95 µs
85 < TCASE ≤ 95 °C	1.95 µs	0.975 µs

At DDR5-8200, 3.9 µs corresponds to 15990 cycles, and 1.95 µs to 7995 cycles.

REFsb has its own maximum average interval:

tREFIsb = tREFI2 / n, where n is the number of banks in one bank group.

This relationship describes the spacing of REFsb commands. It is not an instruction to divide the BIOS tREFI setting manually; the mapping to BIOS fields depends on the controller.

What temperature HWiNFO reports

SPD Hub Temperature in HWiNFO is measured by the sensor in the module's SPD Hub. It is useful for tracking warm-up, but it is not a direct measurement of DRAM TCASE or of the hottest IC.

The specification's 85 °C threshold is therefore not a target operating temperature for overclocked memory. It describes the conditions for the specified refresh rate. A profile with a greatly increased tREFI can become unstable at a much lower module sensor reading.

Practical tREFI reference points

Times are calculated for DDR5-8200 and DDR5-8400. The first row gives a separate BIOS value for each data rate; the remaining rows use the same value for both.

BIOS value	@ 8200	@ 8400	Interpretation
15 990 / 16 380	3.900 µs	3.900 µs	Normal, REFab, TCASE ≤ 85 °C: 3.9 µs. FGR at the same temperature uses 1.95 µs: 7995 / 8190 CK. At 85 < TCASE ≤ 95 °C, halve each interval.
16 383	3.996 µs	3.901 µs	16K: the first binary reference point, almost 3.9 µs at 8400.
32 767	7.992 µs	7.802 µs	A convenient illustrative step.
65 535	15.984 µs	15.604 µs	About one quarter of the 18-bit range.
131 071	31.969 µs	31.207 µs	Half of the range; a popular OC setting.
262 143	63.937 µs	62.415 µs	Maximum of Intel's 18-bit field; a working option with water cooling.

Intermediate values are illustrative tuning reference points. Above roughly tREFI = 30000, this manual's method calls for directed airflow and temperature monitoring during testing. The last row shows the controller field's encoding limit; it does not establish a stable setting for a particular system.

On my TeamGroup Xtreem 2×24 GB kit at tREFI = 131071, errors began at approximately 47 °C on the module sensor. That result applies to the particular kit, voltages, and test. It is not a general temperature limit for DDR5. The ASUS Z790 configuration described here exposes values up to 262143, but the setting must be chosen through stability testing.

Tuning sequence

1. Prepare the test conditions. Data rate and voltages should already be validated. Record the applied timings and provide the cooling that will be used every day.
2. Tune tRFC with tREFI held constant. Change one refresh timing that is actually used at a time, then test stability on warmed-up memory.
3. Raise tREFI separately. Once a suitable tRFC is found, hold it constant and increase the refresh interval with repeated testing. Changing both at once makes it harder to identify the cause of errors.
4. Leave temperature headroom. A test on cold memory does not establish stability after prolonged warm-up. If stability depends on directed airflow, provide the same airflow in daily use.

With more ICs and ranks, check module warm-up separately: cooling requirements may increase.

What to do with tREFIx9

tREFIx9 is a controller parameter limiting the maximum interval between refreshes to one rank. Intel defines it in units of 1024 DCLK and gives this calculation:

tREFIx9 field value = 8 × tREFI / 1024.

The field has a limited range. At high overclocked tREFI values, the direct calculation may exceed that range; the applied value depends on BIOS/MRC. Do not confuse these scaled field units with an ordinary DRAM cycle count.

The practical recommendation here is to leave tREFIx9 on Auto.

DOCUMENTATION: SK hynix 32Gb M-die · §4.13, tables 66–67; SK hynix 16Gb A-die · §4.13.3; Micron DDR5 Core · tables 182–183; Intel Core 13th Gen, Vol. 2 · TC_RFTP, TC_RFP; HWiNFO · SPD Hub temperature

3.8 Tertiary timings: transitions between commands

Intel tertiary timings describe transitions between commands. They set the minimum intervals between successive reads and writes; reducing them allows the controller to schedule the corresponding operations more closely. All values below use memory clock cycles. The practical settings apply to DDR5 with BL16 and CRC disabled.

READING THE NAMES

The order of RD and WR identifies the current and next commands. The suffix specifies which memory regions the transition crosses:

Suffix	Meaning
sg — Same Group	Within one bank group of one rank.
dg — Different Group	Between bank groups of one rank.
dr — Different Rank	Between ranks on one DIMM.
dd — Different DIMM	Between DIMMs in one memory channel.

With 1R/1DPC, the dr and dd paths are not used. This also includes two single-rank DIMMs installed one per memory channel. Dual-rank DIMMs use dr; two DIMMs per channel use dd.

TIMINGS AND PRACTICAL ADJUSTMENT

Timings	Interval	Tuning
tRDRD_sg, tRDRD_dg, tRDRD_dr, tRDRD_dd	**Read → read**.	**tRDRD_dg = 8**. For **tRDRD_sg**, start with the trained value and measure the effect of reducing it.
tWRWR_sg, tWRWR_dg, tWRWR_dr, tWRWR_dd	**Write → write**.	**tWRWR_dg = 8**. In my tests, **16** was the lowest effective **tWRWR_sg** setting; reducing it further produced no benefit.
tRDWR_sg, tRDWR_dg, tRDWR_dr, tRDWR_dd	**Read → write**, including the change in data direction.	Start with **Auto**, then test lower values separately for the paths in use.
tWRRD_sg, tWRRD_dg, tWRRD_dr, tWRRD_dd	**Write → read**.	**sg** is related to **tWTR_L**; **dg** to **tWTR_S**. See the formulas below.

A BL16 burst takes 16 / 2 = 8 clock cycles; this is the basis for 8 in tRDRD_dg and tWRWR_dg. The tWRWR_sg = 16 value is reported as a result of my practical tests.

Initially leave any dr/dd paths in use on Auto, and tune them separately after validating the main transitions.

tWRRD_sg AND tWRRD_dg: THEIR RELATIONSHIP TO tWTR

tWRRD is the scheduler interval between WRITE and READ commands. tWTR describes the wait after write data ends. The values are related, but their reference events differ.

Parameter	Base DDR5 calculation*	Older calculation using a DDR4 burst
tWTR_L	tWRRD_sg – tCWL – 10	tWRRD_sg – tCWL – 6
tWTR_S	tWRRD_dg – tCWL – 10	tWRRD_dg – tCWL – 6

Reverse base calculation:

- tWRRD_sg = tCWL + 10 + tWTR_L
- tWRRD_dg = tCWL + 10 + tWTR_S

Here, 10 = 8 burst cycles + a 2-cycle calculation adjustment. Read tCWL from the controller. In pyhwinfo's main calculation for Raptor Lake DDR5 at 5200 MT/s and above, a long write postamble reduces the calculated tWTR by one additional cycle; the reverse calculation therefore adds one cycle to tWRRD. These are details of that particular readout calculation.

With tCWL and the other adjustments unchanged, lowering tWRRD_sg by one lowers the calculated tWTR_L by one; lowering tWRRD_dg similarly changes tWTR_S.

Leave tWTR on Auto and adjust it by lowering tWRRD. Change one parameter at a time. After training, check the values actually applied, stability under load, cold starts, and the repeatability of performance measurements.

DOCUMENTATION: Intel: RDRD/RDWR/WRRD/WRWR registers; SK hynix: DDR5 device formulas; ASUS Apex Encore BIOS 2202.; pyhwinfo: memory.py, pinned revision

3.9 Maintenance and power-saving timings

These parameters define waits during power transitions, self-refresh, and memory interface maintenance. Shortening them rarely improves performance noticeably, while errors may appear at cold boot, during idle, or on wake-up. Auto is the practical starting point.

PURPOSE OF MAINTENANCE TIMINGS

Parameter	Purpose	Relationship or practical note
tCKE	A controller timing for Power Down transitions.	DDR5 has no separate CKE pin; interpret the field in the context of the platform.
tPD	Minimum time spent in Power Down, from entry to exit.	At least **8 CK and 7.5 ns**.
tCPDED	Delay after Power Down entry before normal command decoding is disabled.	At least **8 CK and 5 ns**; it is not added sequentially to tPD.
tXP	Power Down exit → next ordinary command.	At least **8 CK and 7.5 ns**.
tXS	Self Refresh exit → permitted commands.	**tXS(min) = tRFC1***; commands requiring a locked DLL use **tXS_DLL(min) = tDLLK**.
tRDPDEN	READ → Power Down entry.	Baseline: **tCL + 8 + 1**.
tWRPDEN	WRITE → Power Down entry.	Baseline: **tCWL + 8 + tWR + 1**; do not reduce independently of tCWL/tWR.
tMRD / tMOD	Intervals when programming mode registers.	Distinct maintenance parameters; leave on **Auto**.
tZQCSPeriod	The period for interface impedance calibration maintenance.	**Auto**; do not disable it for a single benchmark. Calibration helps maintain signal margin as temperature changes.
tOSCO / tMRR	Wait after stopping the DQS oscillator / after a mode register read.	May be exposed on Z890; manual adjustment is usually unnecessary.

* For monolithic DDR5, with one DRAM die per package. The relationship with tRFC1 refers to the device specification; it does not mean that tXS should be recalculated automatically from an overclocked BIOS tRFC value.

The Power Down entry formulas assume BL16 with CRC disabled: the burst takes 8 CK. tWR is expressed in cycles here; verify the applied controller fields separately.

POWER DOWN AND SELF REFRESH

Power Down reduces memory power consumption during idle.

Mode	Practical approach
Power Down Disabled — PD = 0	If Power Down is actually disabled, tCKE, tXP, and the PD-entry delays do not participate in this path. **tCKE = 8 is a neutral setting; it does not improve performance.** Auto is also suitable.
Power Down Enabled — PD = 1	Leave maintenance intervals on **Auto** and test extended idle followed by a return to work.

For tXP, both the cycle and nanosecond requirements must be met. At DDR5-8200:

tXP(min) = max(8, ⌈7.5 × 8200 / 2000⌉) = 31 CK.

This is the DRAM lower bound; the controller may apply a longer interval.

Disabling Power Down does not by itself disable Self Refresh, in which memory refreshes its data autonomously. tCKSRX specifies the stable-clock interval before exit; tXS/tXS_DLL specify the wait after exit, depending on the command. Leave these settings on Auto. tREFI specifies the interval for normal externally scheduled refresh.

OREF_RI: REFRESH WHEN A RANK IS IDLE

OREF_RI sets the rank-idle threshold that defines an opportunity for refresh. Auto is the default choice. A value of 0 removes that threshold; refresh remains enabled, and Power Down is controlled separately. A universal benefit from 0 has not been established: compare it with Auto on your own system. In practice, there is little reason to use anything other than Auto.

CHECKING TRANSITIONS AND TRAINING

Auto does not mean zero: check the applied values and training repeatability after a cold boot.

Test the profile under load, at cold boot, through several restarts, after extended idle, and through sleep and wake-up. If a failure occurs after sleep, restore maintenance timings and power policies to Auto and repeat the same scenario. This comparison helps separate a power-transition issue from instability under continuous load.

DOCUMENTATION: SK hynix/Micron DDR5: Power Down and Self Refresh; Intel Raptor/Arrow Lake: TC_PWRDN, TC_MR, TC_RETRAINING_OSCL, TC_RFP; ASUS ROG Z790/Z890: BIOS; CKD: datasheet.

3.10 Correlations by IC, rank, and capacity

The same capacity does not mean the same behavior. Limits are affected by IC density and revision, rank count, modules per channel, and screening quality. Determine the kit's physical organization first; only then transfer timing logic.

Characteristic	What it changes	Which timings it affects	What to check
IC revision	Internal ranges and voltage response	tCL, tRCD, tRP, tRFC, tCWL	Marking/part number; XMP tells you nothing about the revision.
Die density	Number of cells on the die	tRFC1/2/sb specifications and practical tRFC	Compare time in ns with data for the same density.
1R / 2R	Load and rank switching	2R activates tertiary dr timings and changes ODT	With 2R, return dr and training settings to Auto.
1DPC / 2DPC	Number of modules and signal-path length	2DPC activates dd, more often requires looser CR	Find frequency again, then timings.
XMP screening	Starting frequency, CL, and voltage	Does not define a universal minimum	Compare the entire profile, not just MT/s.

TYPICAL KITS AND TUNING PRIORITIES

Kit	Common organization	Typical characteristic	Tuning logic
2 x 16 GB	16-Gbit x8, 1R	Older Hynix A-die often scales down tCL well	Find frequency/tRCD first, then tCL and VDD response.
2 x 24 GB	24-Gbit x8, 1R	Non-binary Hynix M-die	Lowering below CL36 often requires a lot of VDD for next to no gain.
2 x 32 GB	Depends on the specific SKU	May be 2R 16-Gbit or denser 1R	Do not draw conclusions from capacity: check SPD, rank, and density first.
2 x 48 GB	Often 24-Gbit x8, 2R	Rank-to-rank transitions are active	Find frequency, dr, and refresh settings again.

tCL AND VDD: CALCULATE THE ACTUAL GAIN

At DDR5-8200, reducing tCL from 38 to 36 cuts pure CAS latency by approximately 0.49 ns. If this requires 50-100 mV more VDD, makes the memory run hotter, and leaves tRCD/tRP unchanged, a CL38 daily profile may be the more rational choice.

CAPACITY MATTERS THROUGH ORGANIZATION

A 24 GB module built with 24-Gbit ICs remains single-rank, while a 48 GB module using the same ICs usually requires two ranks. In the latter case, the controller gains more parallelism but must also switch ranks and train additional dr paths.

When moving from 48 GB to 96 GB, retest frequency, tertiary transitions and refresh, even with the same IC revision.

CUDIMM improves the clock path through CKD, but does not change the meaning of tCL, tRCD, tRFC, or tertiary transitions. When transferring a profile, preserve relationships and time in ns—not the old timing values. Recalculate the cycle counts for the new data rate and validate them on the new configuration.

DOCUMENTATION REVIEWED: SK hynix module/component datasheets; Intel memory support; TeamGroup DDR5-8200/6800 kits; practical A/B methodology.

3.11 ASUS Z790 APEX ENCORE BIOS 2202

In this chapter, I use the ASUS ROG Maximus Z790 Apex Encore with BIOS 2202 as the reference. The official manual confirms the overall structure, but the individual entries depend on firmware, processor, and modules. Setting names are given exactly as ASUS labels them.

> **AUTO ON APEX IS A VALID STARTING POINT**
>
> On the Apex BIOS versions I tested, secondary and tertiary timings train correctly on Auto. After a boot after idle, save the values actually applied, including Runtime, and begin reducing them one at a time from that baseline.

MAP OF THE DRAM TIMING CONTROL SECTION

ASUS group	What it contains	How to use it
Primary Timings	tCL, tRCD Read/Write, tRP, tRAS, Command Rate	Main timing string; Read and Write are shown as separate fields.
Secondary Timings	tRRD, tFAW, tRFC, tREFI, tWR, tRTP, tWTR, tCWL	Activation, recovery, and refresh.
Third Timings	tRDRD, tWRWR, tRDWR, tWRRD with sg/dg/dr/dd	Controller transitions; use trained values as the reference.
Misc. Timings	Power Down, Self Refresh, ZQ, and service intervals	PD=0, everything else on Auto unless addressing a specific diagnostic problem
Memory Training Algorithms	Interface training and matching algorithms	Covered in detail in Chapter 05; do not confuse with a timing.

EXACT FIELDS MOST OFTEN SET MANUALLY

ASUS name	In brief	Relationship	BIOS 2202 nuance
DRAM CAS# Latency	tCL	READ -> data	For DDR5, an odd value is rounded up.
RAS# to CAS# Delay Read / Write	tRCDRD/ WR	ACT -> RD/WR	Two fields; equal values can be used as a starting point, but this is not a universal requirement.
DRAM RAS# PRE Time	tRP	PRE -> ACT	Tested during row changes.
DRAM RAS# ACT Time	tRAS	ACT -> PRE	Compare with tRCDRD+tRTP.
DRAM REF Cycle Time 2	tRFC	Refresh	This manual refers to the field neutrally as tRFC; the ASUS name alone does not prove active 2x FGR.
REF Cycle Time Same Bank	tRFCsb	One bank in each group	The other banks remain available during the cycle.
WRITE to READ Delay L / S	tWTR_L/ S	End of WR data -> RD	Related to tWRRD_sg/dg.
DRAM Write Latency	tCWL	WRITE -> data	The CL36 baseline uses CWL34 according to the formula tCWL = tCL − 2 = 34
tRDRD_sg/dg Training / Runtime	RDRD	RD -> RD	Runtime is the actual operating interval; this is the value to record.

> **TRAINING AND RUNTIME**
>
> Training refers to finding an operating range during memory training; Runtime refers to the interval actually used by the scheduler after boot. Auto is not an empty value: before manual tuning, save the actual numbers after a boot after idle.

WHAT TO RECORD BEFORE MANUAL ENTRY

After full training, save the frequency, Gear, Command Rate, all primary and secondary timings, the tRDRD/tWRWR/tRDWR/tWRRD groups, module temperature, and BIOS version. For fields with Training/Runtime, record Runtime specifically.

After boot, the MRC may round an entered value to a valid code or apply an internal constraint. Use the actual post-boot value as your reference.

DOCUMENTATION REVIEWED: ASUS ROG Z790 Series BIOS Manual; ROG Maximus Z790 Apex Encore BIOS 2202 menu; Intel timing registers.

3.12 ASUS Z890 Apex: what changed

The meaning of the main DDR5 timings has not changed on Z890, but ASUS reorganized the menu for Core Ultra 200S, CUDIMM, and the new MRC. Transfer the logic and relationships from Z790, not every number or field name. The table is based on the public ROG Z890 manual; the specific entries depend on BIOS, CPU, and DIMM.

Area	Z790 Apex Encore 2202	Z890 Apex	Practical takeaway
Profiles	Maximus Tweak	Memory Presets; DIMM Fit / Fit Store	DIMM Fit is a new training tool, not a renamed Tweak.
Command Rate	1N, 2N, 3N, N:1	1N / 2N in the public menu	2N remains the baseline for high-frequency DDR5.
tCCD	Separate fields are not shown	tCCD_L and tCCD_L_WR added	Long read and write paths are easier to see.
Refresh*	tRFC1, tRFC2, tRFCsb, tREFI, and extended fields	Publicly: tRFC, tRFCsb, tREFI; tRFM added	RFM is a refresh-management mechanism for frequent activations; tRFM is the duration of an RFM cycle. Neither replaces tRFC.
tRDRD	Training and Runtime separate	One final entry in the public menu	Training itself remains; manual separation of the fields is gone.
Power	Scattered Power Down fields	Explicit modes, thresholds, and counters by subchannel	Configuration is more detailed, but leave it on Auto for timing overclocking.
Divide DRAM timings	No separate entry in the public manual	Single Divide DRAM timings entry	This encodes field ranges; it is neither Gear 4 nor a way to reduce latency.
Training	Baseline algorithms and Round Trip	Training Consistency; Rank-to-Rank; more PHY settings	Test repeatability after a boot after idle.

NEW AND HIDDEN FIELDS

Group	What is visible on Z890	How to interpret it
Added	tCKCKEH, tCA2CS, tOSCO, tMRR, tRPab, tccdByteCasDelta, tRFM, tSR, tZQCSPeriod, tMRD	Some service parameters and mechanisms became visible; this is not a mandatory manual-overclocking list.
Not shown	tRFC2, tREFIX9, Ref Interval, tXPDLL, tMOD, tZQOPER, and low-level refresh debt/PBR fields	The absence of an entry from the public menu does not prove that the mechanism disappeared from the MRC.
Not renamed	tRPab ext ≠ tRPab; tMOD ≠ tMRD; tZQOPER ≠ tZQCSPeriod	Similar names cannot be carried over as direct equivalents.

CUDIMM AND CKD

CKD restores the clock signal on the module, but does not change the meaning of tCL, tRCD, or tRFC. CUDIMM adds CKD settings: CKD Skew Control, PLL Bypass, and PLL modes. Dual PLL was added in BIOS 1203. PLL Bypass disables the primary advantage of CKD; it is used for compatibility and diagnostics.

WHAT TO TRANSFER FROM Z790 AND WHAT TO FIND AGAIN

You can transfer the meaning of settings, the tRC=tRAS+tRP formula, the tRRD/tFAW and tWTR/tWRRD relationships, and the approach of converting cycles to nanoseconds from Z790. Frequency, voltages, training results, and PHY-dependent values must still be found again. Do not search for Z890 entries absent from the public manual under similar names and fill them with Z790 numbers. Start with Auto and the actual value, then confirm the function for the specific BIOS version. Leave Divide DRAM timings on Auto until a field-range limitation appears. It has no universal 9600 MT/s threshold: the BIOS/MRC decides according to frequency and the encoding of the specific timing.

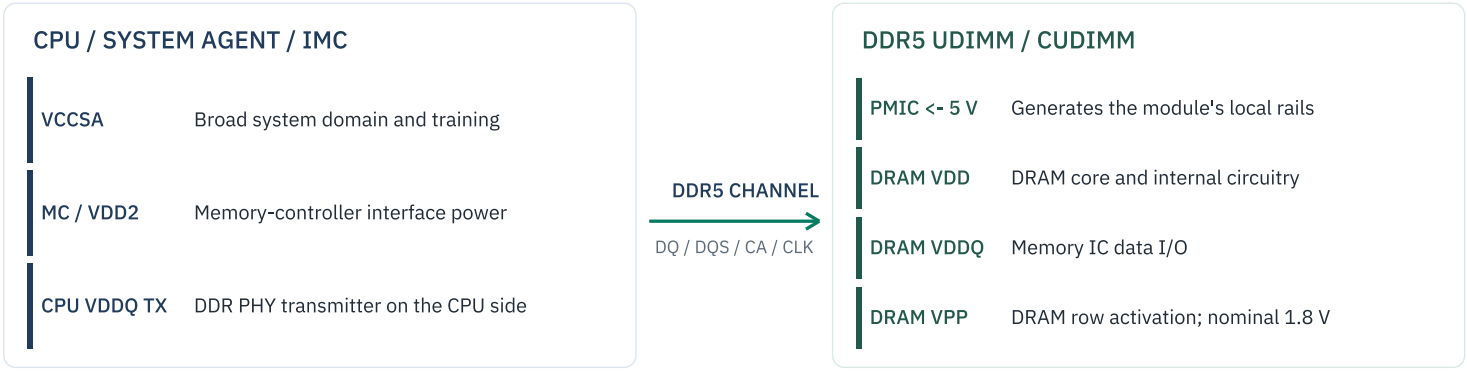
***** For Raptor Lake-S, public Intel documentation states that DDR5 RFM is not enabled. The presence of a similar BIOS entry alone does not prove that the mechanism is active on a specific platform.

DOCUMENTATION REVIEWED: ASUS ROG Z790/Z890 BIOS Manuals; ASUS CKD/CUDIMM/Memory Gear note; Z890 Apex BIOS changelog; Intel Core Ultra 200S registers.

04 / Voltages

4.1 Power domains: CPU, IMC/PHY, DIMM

DDR5 overclocking involves adjusting voltages for several independent domains. Some are inside the processor, some belong to the channel's electrical interface, while VDD, VDDQ, and VPP are generated by the PMIC on the module itself. First separate these areas physically; only then look for a relationship with the error.



CPU-SIDE AND DIMM-SIDE VDDQ: SEPARATE POWER RAILS

DRAM VDDQ powers data I/O on the DIMM's memory ICs. On Z790, IVR Transmitter VDDQ applies to the CPU transmitter. On Z890, Vddq Voltage Override is in the CPU-side Advanced Memory Voltages block. In both cases, VDDQ identifies an I/O-domain voltage in the DQ/DQS data path, but on opposite sides of the CPU-DIMM interface; they are functionally related but electrically independent power rails.

HOW TO READ THE NUMBER SHOWN BY THE BIOS

Value type	Example	What it means
Setpoint	SA, TX, MC, DRAM VDD/VDDQ	The requested value. Voltage at the measurement point may differ from it.
Auto / training	MRC selects Vref, ODT, and delays	In Auto mode, the firmware algorithm selects the value. Full retraining is required after changing one voltage.
Calculation base	MC/VDD Calculation Voltage Base	A calculated value that firmware uses when setting the voltage of an existing rail.
Telemetry	IVR VCCSA, VDDQ TX, IMC VDD, PMIC	Compare readings from the same sensor under the same load.

4.2 CPU System Agent Voltage: SA

VCCSA powers the System Agent, a domain that includes more than the memory controller alone. SA affects the memory and uncore operating point and MRC repeatability. VDD2 supplies the controller interface, while the module’s power rails supply the DRAM chips. On Z890, SA also contributes to uncore/NGU tuning; D2D has its own power domains and ratios.

Insufficient SA may appear as POST loops, problems with boots after idle, or inconsistent training results. Too much can cause the same symptoms: noise, reference levels, and the PHY range found by training all change. Use small steps to find a range that gives repeatable results.

> **BIOS INPUT RANGE AND DAILY-USE PROFILE LIMITS**
>
> The voltage range available in ASUS BIOS is wider than needed for everyday DDR5 overclocking and tuning. The upper values in this range are unsafe.

DOCUMENTATION REVIEWED: Intel Raptor Lake / Core Ultra 200S power-rail specifications; ASUS ROG Z790 — E21402 / Z890 — E25061: BIOS Manuals; Micron DDR5 client-module architecture.

4.3 CPU VDDQ TX

On ASUS Z790, the IVR Transmitter VDDQ Voltage entry literally sets the internal transmitter voltage of the memory controller. This is part of the CPU-side channel: it participates in shaping DQ/DQS edges, write training, Vref/ODT, and electrical margin at high speed.

TX state	What we usually observe	How to interpret it
Insufficient	Unstable write training, early data-path errors, dependence on MT/s	TX VDDQ is the first suspect. MC, DRAM VDDQ, ODT, and PHY may also contribute to the same symptoms.
Operating range	Boots after idle are repeatable; Vref and trained intervals do not vary	Choose a voltage with some margin within the verified range of stable boots.
Excessive	Increasing it no longer helps or immediately worsens training	The stable operating range may narrow because of edge overshoot, crosstalk, and incorrect balance with the other side of the channel.

> **TX VDDQ AND DRAM VDDQ OPERATE ON OPPOSITE SIDES OF THE CHANNEL**
>
> They do not have to be equal, and there is no universal "correct" delta between them. Hold the other side at a known-stable value, then change only one voltage in small steps with full retraining.

On Z890, the separate IVR Transmitter VDDQ name is gone. Advanced Memory Voltages adds VccDdqControl Bypass and Vddq Voltage Override, alongside VccIog and VccClk fields. The public ASUS manual confirms these low-level CPU/PHY-side settings, but does not disclose their exact electrical mapping. Vddq Override is functionally similar to the former TX domain, but cannot be treated as a 1:1 rename or assigned a copied Z790 value.

4.4 VDD2: IMC interface power

ASUS calls this rail Memory Controller Voltage on both Z790 and Z890. Its hardware name in Intel documentation is VDD2: power for the memory-controller interface and processor DDR I/O. HWiNFO usually shows it as IMC VDD. VDD2 supplies the controller interface, module VDD supplies the internal DRAM circuits, and TX VDDQ supplies the CPU-side transmitters.

Factor	Why it changes the load	Practical takeaway
MT/s and Gear	Higher MT/s shortens data-transfer intervals. Switching from Gear 2 to Gear 4 at the same memory data rate halves the memory-controller frequency and usually increases access latency.	MC often affects the frequency limit. Tune it together with a frequency that is realistic for your configuration.
2R	More ranks, receivers, and switching within the DIMM/channel	First find frequency, ODT, and training again; do not raise MC automatically.
2DPC	A second DIMM adds electrical load and line branches	Account for motherboard topology and retest frequency, ODT, and training.
Die density	Changes DRAM internal organization and refresh	Affects MC indirectly; more strongly related to VDD, tRFC, tREFI, and temperature.
Excessive MC	Power consumption, heat, and noise within the CPU increase	If a higher MC voltage does not widen the stable operating range, it only adds load.

WHAT TO LEAVE ON AUTO

MC/VDD Calculation Voltage Base entries are firmware calculation parameters. Memory Controller Boot Voltage sets the voltage of an existing rail during boot; Eventual Memory Controller Voltage sets its final operating voltage. The Boot/Eventual names belong to specific Z790 BIOS versions and may be absent from the public Z890 menu; unless a problem specifically during the transition from boot to runtime has been confirmed, leave these fields on Auto.

DOCUMENTATION REVIEWED: ASUS ROG Z790 — E21402 / Z890 — E25061: BIOS Manuals; Intel Raptor Lake / Core Ultra 200S VDD2 and memory-controller specifications.

4.5 DRAM VDD and VDDQ

DRAM VDD and DRAM VDDQ reside on the module itself and are generated by its PMIC. VDD powers the DRAM core, while VDDQ powers the IC data I/O. Nominal VDD and VDDQ are 1.10 V each; XMP profiles often use higher values.

Rail	Physical role	More commonly related to	What limits it
DRAM VDD	DRAM core, array, and internal peripheral circuitry	tCL, some internal timings, and the individual tRFC minimum	IC revision and screening, temperature, and the early tRCD/tRP plateau.
DRAM VDDQ	Data transmitters/receivers on the DIMM	Signal margin during data writes/transfers, VrefDQ, and turnarounds together with CPU TX and MC	Channel quality, ODT, and training; further increases may worsen the result.

HOW VOLTAGES RELATE TO FREQUENCY AND TIMINGS

Change	Typical response	Why you cannot increase it blindly
MT/s	Affects VDD/VDDQ, but also TX, MC, SA, and training	A frequency limit is rarely solved by one module voltage.
tCL	On Hynix, it often responds more noticeably to VDD	On 24-Gbit M-die, further reducing tCL at the selected memory data rate may require a substantial increase in VDD for little or no performance gain.
tRCD / tRP	IC architecture often becomes the limit sooner	After the plateau, excess VDD only adds heat.
tRFC / tREFI	Depend on density, revision, and temperature	Higher VDD can heat the DIMM and worsen refresh stability after warm-up.

EQUAL VDD AND VDDQ AS A STARTING POINT

Starting with equal XMP values is convenient. After verifying stability, tune VDD and VDDQ separately: hold one voltage constant, change the other in small steps, and test the result.

4.6 Auxiliary power settings

ASUS entry	What it does	Practice used in this manual
High DRAM Voltage Mode	Unlocks BIOS voltage settings above 1.435 V.	Does not raise anything by itself. The BIOS maximum of 2.070 V is not a safe recommendation.
DRAM VPP Voltage	Row-activation power; nominal 1.8 V	Do not change.
SPD HUB VLDO / VDDIO	SPD Hub logic power at 1.8 V and sideband at 1.0 V	Auto; problems here are more closely related to SPD, the sensor, and PMIC control.
Sync All / By per PMIC	Identical or separate module programming	Synchronized adjustment is convenient for modules in one kit; adjust separately only after confirming a difference. Even a matched kit does not guarantee equal temperature and telemetry.
Switching Frequency / Current	Converter mode and PMIC current limit	Leave on Auto until measurable voltage droop or a PMIC error is identified. These fields control the converters for existing power rails.

CUDIMM: DRAM POWER AND CKD MODES

CKD restores the clock signal and can operate in Single PLL, Dual PLL, or Bypass mode.

DOCUMENTATION REVIEWED: Micron DDR5 SDRAM and client modules; ASUS ROG Z790 — E21402 / Z890 — E25061: BIOS Manuals; Renesas P8911 PMIC and RG5C172 CKD short-form datasheets.

4.7 Voltage tuning

Every voltage has an operating range. Below it, electrical margin is insufficient; above it, edge rate, Vref, ODT, noise, and heat change, and after full retraining the operating range may narrow again. The dynamic component of power scales roughly as Pdyn ~ C x V^2 x f, so a small increase in V at high frequency noticeably affects heat.

Problem type	First suspects	What to check before increasing	Suitable test
No POST / training loop	MC/VDD2, CPU VDDQ, SA, frequency	Gear, 1DPC/2DPC, ODT, several boots after idle	POST codes and retraining
Early write/data errors	DRAM VDDQ, CPU TX, MC	tWR/tWTR/turnaround and trained Vref	Karhu/TM5 with emphasis on writes
VT3 fails	MC, TX, SA, and interaction with CPU/ring	Separate a memory error from heavy CPU load	y-cruncher VT3
Errors only after warm-up	VDD, tREFI/tRFC, cooling	DIMM temperature and lowering tREFI	Karhu/TM5 after warm-up with monitoring
Boot after idle / sleep only	Training, startup setpoints, power state	MRC Fast Boot, saved training results, and auxiliary settings on Auto.	Boots after idle, sleep/wake

CHOOSING A VOLTAGE FOR DAILY USE

Keep the frequency, Gear, and configured timings at their current values. Change one voltage, perform full retraining and several boots after idle. Record the training results and compare them at similar temperatures. Find the lower boundary in small steps, and move upward only within a predefined reasonable range, stopping if there is no improvement or temperature rises. There is no need to deliberately raise voltage until errors appear. Leave the final value inside the repeatable range with a small margin; no error code identifies a specific rail unambiguously.

My Z790 Apex Encore / BIOS 2202 / 2 × 24 GB / DDR5-8200 profile uses SA 1.22; TX 1.35; MC 1.40; VDD 1.49; VDDQ 1.44 V. Telemetry shows similar but unequal numbers. This example shows the difference between setpoints and sensor readings on my configuration. Voltages for another system must be selected separately; the safety of these values has not been established here.

4.8 Voltage names in ASUS BIOS

Function	Z790 Apex Encore 2202	Z890 Apex	How to transfer it
System Agent	CPU System Agent Voltage	CPU System agent Voltage	Name retained; do not copy the numbers because of the new NGU/D2D architecture.
CPU-side VDDQ	IVR Transmitter VDDQ Voltage	VccDdqControl Bypass + Vddq Voltage Override	Functionally similar, but not a confirmed 1:1 rename.
IMC / VDD2	Memory Controller Voltage	Memory Controller Voltage	Main CPU-side memory rail; HWiNFO often shows IMC VDD.
DRAM core/data	DRAM VDD Voltage / DRAM VDDQ Voltage	Same exact names	DRAM VDD and DRAM VDDQ are module power rails generated by the PMIC; CPU Vddq Override refers to the processor side.
PMIC / SPD / VPP	PMIC Voltages; SPD HUB; DRAM VPP	Same groups; PMIC0-1 on Apex	Leave service settings on Auto unless asymmetry has been demonstrated.
Z890 auxiliary fields	No separate public entries	VccIogControl Bypass; VccIog Voltage Override; VccClkControl Bypass; VccClk Voltage Override	Low-level CPU/PHY fields; exact electrical role is not publicly disclosed. Leave on Auto without specific diagnostics.
D2D / always-on	No	VNNAON 0.77v Voltage; NGU Ratio; CPU D2D Ratio	Settings for D2D and the CPU's always-on domain; leave on Auto/stock values for ordinary memory tuning.

INTEL 200S BOOST: PROFILE CONDITIONS AND SCOPE

Intel 200S Boost requires a compatible Core Ultra 200S K/KF or 200S Plus processor, a Z890 motherboard with BIOS support for the profile, and one installed XMP DIMM per channel (1DPC). The profile supports data rates up to DDR5-8000 with VDD2 ≤ 1.40 V, VCCSA ≤ 1.20 V, and module VDD/VDDQ ≤ 1.40 V.

DOCUMENTATION REVIEWED: ASUS ROG Z790 — E21402 / Z890 — E25061: BIOS Manuals; Z790 Apex Encore / Z890 Apex BIOS changelogs; Intel Core Ultra 200S power rails and 200S Boost; my BIOS/HWiNFO baseline.

4.9 Voltage guidelines

The ranges below are very approximate guidelines based on my personal opinion. There is no single official safe range for manual overclocking: platform, IC type and density, rank count, number of modules, and other factors all matter.

VOLTAGE RANGES, V

Rail / platform	Working OC (V)	Not recommended (V)
DRAM VDD[1]	1.45–<1.52[2]; 1.45–<1.55[3]	>1.55
Z690 · VCCSA	**4** 1.20–1.30	>1.35
Z690 · IVR TX VDDQ	1.20–1.35	>1.35
Z690 · MC / VDD2	1.25–1.40	>1.40
Z790 · VCCSA	1.10–1.30	>1.40
Z790 · IVR TX VDDQ	1.20–1.40	**5** >1.45
Z790 · MC / VDD2	1.25–1.45	>1.50
Z890 · VCCSA	1.00–1.20	>1.35
Z890 · MC / VDD2	1.20–1.40	>1.50

Official Z890 reference: Intel 200S Boost — SA ≤ 1.20 V.

1 A-die, non-binary M-die; **2** air; **3** water; **4** reduce only while retaining stability, down to 1.10–1.15 V; **5** in my observations within the community, sustained TX VDDQ >1.45 V coincided with cases of failed 13900K and 14900K processors. These are observations, not a confirmed failure threshold.

DRAM VDD AND VDDQ: TUNED SEPARATELY

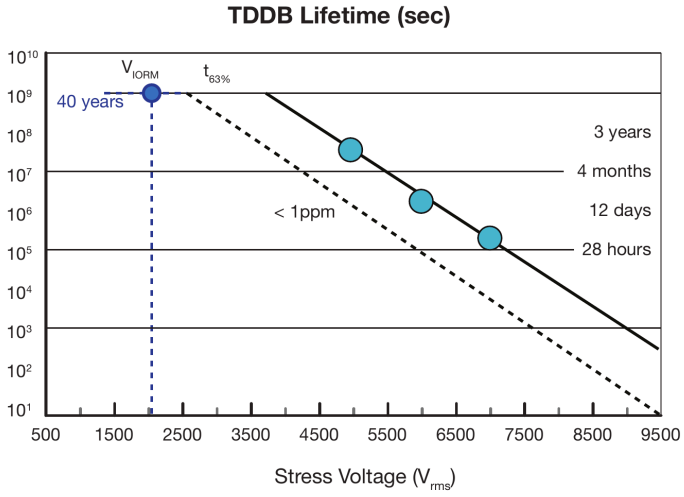
VDD powers DRAM circuitry; VDDQ powers I/O. The rail-to-rail voltage difference is limited by IC/PMIC specifications; maximum ratings are not operating conditions. No safe OC delta has been established. Fix VDD, frequency, and timings, then lower VDDQ in 10–20 mV steps. After warm-up and several complete training cycles, find the lower passing boundary, then select a value with a small margin inside the repeatable range. Passing tests does not prove that an overclock is safe.

A MEMORY WATER BLOCK: GOOD THERMAL HEADROOM

With good contact and cool liquid, a water block reduces DIMM temperature and provides headroom for timings, frequency, or lower voltage. If the limit is already the IMC or signal quality, there may be no gain.

Comparison of the same 2 × 24 GB M-die pair: for 8200 CL34, a 140 mm fan at 800 rpm required 1.56 V at 49.2/48.5 °C; the water block required 1.50 V at 31.2/31.0 °C. This was AM5, voltages were tuned separately, and validation was 1 hour of Karhu plus about 25 minutes of TM5. Temperature was read from the SPD Hub; I did not study service life. The example is provided for comparison.

ELECTRICAL STRESS REMAINS EVEN WITH COOLING



TI, SSZY028 (2017), Fig. 5. High-voltage insulators. The voltages and service lives shown do not apply to DDR5. The figure illustrates the principle.

Higher voltage increases the electric field in the dielectric. Prolonged exposure gradually degrades its insulating properties and may end in breakdown: TDDB. Heat accelerates several aging mechanisms.

A water block reduces temperature while leaving the electric field from the configured VDD/VDDQ unchanged. A cold module can therefore pass tests while still losing service life. Lower temperature reduces the thermal component of risk; it does not make high voltage safe.

In the TI graph, the X-axis is voltage and the Y-axis is time to breakdown on a logarithmic scale. The higher the test voltage, the shorter the time. The points represent failure of 63% of samples; the dashed line predicts a 1 ppm failure rate.

DOCUMENTATION REVIEWED: Intel 200S Boost; PhoenixMDA: voltage and cooling measurements; Texas Instruments SSZY028, Fig. 5. Intel 200S Boost, Comparison of one 2 x 24 GB M-die pair, TI, SSZY028 (2017), Fig. 5.

05 / Memory tuning and training

5.1 System preparation

Before trying someone else's timings, establish a repeatable baseline on your own system. First prove that the system works correctly on clean JEDEC/Auto, then establish a separate XMP baseline. Old manual voltages, trained values, or hidden profile settings must not be carried between these modes.

TWO BASELINES FOR TWO DIFFERENT TASKS

Mode	What to apply	What it is for
JEDEC / Auto	Load Optimized Defaults, XMP disabled; perform full training	Verify assembly, slots, SPD, boot, and baseline operation without overclocking.
XMP II	The complete set of parameters in the DIMM's XMP profile; BIOS/MRC determines parameters absent from the profile.	The original XMP baseline for comparison; loading XMP II does not exclude BIOS/MRC involvement.
XMP I	Main DIMM XMP fields with the remaining parameters optimized by ASUS	A separate comparison branch; do not mix its results with XMP II.
XMP Tweaked	XMP plus additional ASUS settings for compatible kits	Enhanced ASUS profile: test only after establishing a stable baseline.

RECORD FOR EACH SESSION

Record	Exact information	Record	Exact information
Platform	CPU, motherboard, BIOS version, and ME	Kit	Part number, total capacity, 1R/2R, die density
Installation	A2/B2 on a 4-DIMM board or both Apex slots; record DIMMs per channel separately	Module type	UDIMM/CUDIMM, XMP profile, CKD mode if present
Conditions	DIMM airflow, room temperature	Readings	BIOS setpoints and HWiNFO sensor readings
Result	Boot type, Q-Code (diagnostic POST code), training time	Validation	Test, duration, temperature, and exact symptom

5.2 Choosing initial settings



WHAT INVALIDATES THE ESTABLISHED BASELINE

Changing the CPU, DIMM count or rank, occupied slots, UDIMM/CUDIMM type, BIOS version, or making a major change to frequency/Gear (the controller divider) requires retesting the corresponding earlier stage.

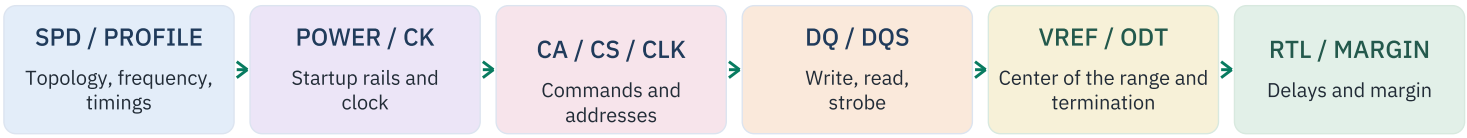
WHY WE CHOOSE MEMORY CAPACITY BEFORE DATA RATE IN MT/s

Capacity determines the available module organization and electrical load before a target frequency is chosen. A 2 × 48 GB kit usually requires a different strategy from 2 × 24 GB, even with the same IC manufacturer: rank count, training, ODT, temperature, and the controller's realistic ceiling all change. Gear (the controller divider) and Command Rate (the command interval) are selected after the target load. Only then does it make sense to find useful SA, TX, MC, VDD, and VDDQ ranges. This helps identify the causes of failures and reduces the risk that excess voltage masks an incorrectly chosen baseline.

DOCUMENTATION REVIEWED: ASUS ROG Z790/Z890 BIOS Manuals; ASUS XMP I/II/Tweaked descriptions; Intel MRC and DDR5 platform documentation.

5.3 MRC memory training

Memory Reference Code (MRC) is part of Intel firmware that selects working delays, reference-voltage levels, termination, and signal compensation during boot. The result is a set of parameters for continuing the boot process. Optimal timings are selected when tuning the profile, and stability is tested separately under load.



5.4 Startup and restart

Scenario	What happens	What it proves
Full training	MRC reruns the required set of stages; POST takes noticeably longer	Repeatability of the range found during retraining. Stability in Windows is checked with separate stress tests.
Reboot	Normal reboot without removing power; a fast path may be used	Only the system's ability to reboot with this profile.
S5 / shutdown	The OS has shut down, but the motherboard may remain on standby power	Not a power-cycled boot and does not guarantee full retraining.
Power-cycled boot (AC Cold Start or Cold Boot)	A cold system startup after power has been completely removed	Does not guarantee a full MRC run if firmware uses saved data.
MRC Fast Boot / Fast Boot	BIOS applies a shortened MRC path	Enable it to save time after confirming that full training is repeatable.
BIOS Fast Boot	Speeds up overall POST and device initialization	BIOS Fast Boot speeds up general device initialization; MRC Fast Boot shortens memory training by reusing saved results.
Windows Fast Startup / sleep	The OS restores saved state or resumes from sleep	Tested separately, in addition to a boot, a reboot, and a power-cycled boot.

ASUS SERVICE SETTINGS

BIOS entry	Purpose	How to use it
MRC Fast Boot (Z790) / Fast Boot (Z890)	Shortened path through MRC	Disable while finding a profile; enable after a series of full training cycles.
MCH Full Check	Full MCH check; ASUS associates Enabled with stability	Auto/Enabled for a daily profile; Disabled only for a limit experiment.
Mem Over Clock Fail Count	Number of failed POST attempts before recovery	Do not set too high: a large number only prolongs a failed training loop.
Training Profile	Auto / Standard Profile / ASUS User Profile	Start with Auto; the internal difference is not publicly disclosed.
Mrc Training Loop Count	Exponential number of internal cycles	Controls internal MRC training loops; leave on Auto unless you have a specific diagnostic task. Stress tests are run separately in the OS.
Improve Training Limit (Z790 2202)	The entry exists in firmware, but its exact logic is not publicly described	Leave on Auto; do not assign it an invented frequency or voltage limit.
Memory Test on Warm Boot (Z790 2202)	A basic memory check during a reboot. Here, Warm Boot denotes the type of startup; component temperature is considered separately. The entry may be hidden.	For diagnostics only; does not replace OS testing.
Realtime Memory Timing	Allows timings to be changed after MRC_DONE	Disabled for the normal methodology; recheck the result after a full POST.

THE KEY DISTINCTION

A successful POST means only that the MRC found parameters with which the system can boot. An error may appear later after warm-up, under another load, or during the next full training cycle. Training and testing are therefore two consecutive but distinct stages.

DOCUMENTATION REVIEWED: ASUS ROG Z790/Z890 BIOS Manuals; Intel Memory Reference Code and Core Ultra 200S memory-initialization documentation.

5.5 Training Algorithms on ASUS Z790

The table combines the public ASUS Z790 BIOS manual with the actual Apex Encore BIOS 2202 menu. In Auto, MRC/ASUS selects the state of each function. The final column is my practical A/B scheme for Z790 Apex Encore / BIOS 2202 / 2 x 24 GB DDR5-8200. For another motherboard, CPU, kit, or BIOS, start with Auto.

Group	BIOS entries (similar items grouped)	What it trains	Mode
Commands / CA	Early Command Training; Command Voltage Centering; Early Command Voltage Centering; Late Command Training; CMD CTL CLK Slew Rate; CMD/CTL DS & E 2D; CMD/CTL Drive Strength Up/Dn 2D	Timing, Vref, drive strength, and edges of the command/address path	Auto.
Initial read	**SenseAmp Offset Training; Early ReadMPR Timing Centering 2D; Read MPR Training; Receive Enable Training; Receive Enable Centering 1D**	Receiver calibration, MPR, and read-gate timing; affects RTL.	**Auto; do not disable Receive Enable**
Write	**Jedec Write Leveling; Early Write Time Centering 2D; Write Timing Centering 1D; Write Voltage Centering 1D; Write Timing Centering 2D; Write Voltage Centering 2D**	DQS-to-CK alignment and write-eye centering.	**Auto / stock; do not disable JEDEC WL**
Read	**Early Read Time Centering 2D; Read Timing Centering 1D; Read Timing Centering with JR; Read Voltage Centering 1D; Read Timing Centering 2D; Read Voltage Centering 2D**	One- and two-dimensional search for the center of the read eye in time and Vref.	**Auto; Early Read Time 2D - Enabled for 8000+***
ODT / RON / drive	**Dimm ODT Training; Max RTT_WR; DIMM RON Training; Read ODT Training; DIMM CA ODT Training; Write Drive Strength/Equalization 2D; Write Slew Rate Training; Write Driver Strength Training; Write Drive Strength Up/Dn independently**	DIMM/channel termination and drive strength. Manual Ω values are covered in 5.9.	**Auto; Max RTT_WR - ODT OFF, 120 Ω for A/B only**
Equalization	Read Equalization Training; Read Amplifier Training	Correction of receiver-path loss and distortion.	Auto
Compensation	**Comp Optimization Training; TxDqTCO Comp Training; ClkTCO Comp Training; TxDqsTCO Comp Training; VccDLL Bypass Training; PanicVttDnLp Training; Read Vref Decap Training; Vddq Training**	PVT, PHY delays, DLL, and reference levels; do not transfer between CPUs/BIOS versions.	**Auto; Vddq: Auto → Disabled after voltages are fixed***
DCC	Duty Cycle Correction Training; Periodic DCC; Tx Dqs Dcc Training	Correction of CK/DQS duty cycle and its drift.	Auto
RTL / transitions	**Round Trip Latency; Turn Around Timing Training**	Round-trip delay and RD↔WR intervals; related to frequency, WTR, ranks, and topology.	**RTL - Enabled; TAT: Auto → Disabled after manual turnaround settings***
DDR5 signal	DIMM DFE Training; EARLY DIMM DFE Training; DRAM EMPHASIS Training; DRAM DCA Training; DQS OFFSET ADJUST Training	DFE/DCA; DRAM EMPHASIS and DQS OFFSET ADJUST behavior is not disclosed.	Auto
Margin / test	Rank Margin Tool Per Bit; Rank Margin Tool; Memory Test; DIMM SPD Alias Test; Post Package Repair Training; Retrain Margin Check; Margin Check Limit; Margin Limit Check L2	Service checks of signal margin. Stability in the OS is verified with stress tests.	Auto; RMT/Test - temporarily Enabled for diagnostics
Not for this manual	LPDDR DqDqs Re-Training	Applies to LPDDR, not desktop DDR5 DIMMs.	Not applicable

* For my Z790 Apex Encore / BIOS 2202 / 2 x 24 GB DDR5-8200: I enable Early Read Time 2D at 8000+, disable TAT only after manually setting turnaround/WTR values, and disable Vddq Training after setting fixed CPU TX VDDQ and DRAM VDDQ values and completing several successful training cycles after boots after idle. Start with Auto on another platform. BIOS 2202 uses the name Early Read Time Centering 2D; some manuals use Timing.

DOCUMENTATION REVIEWED: ASUS ROG Z790 Series BIOS Manual, pp. 32-34; actual Apex Encore BIOS 2202 menu; my analysis and validated profile scheme.

5.6 Training Algorithms on ASUS Z890

The Z890 menu exposes more PHY/MRC stages. The starting scheme below uses the ASUS manual and my recommendations. I leave most stages on Auto; choices for manual timing adjustments are shown in the table and Chapter 06.

Group	BIOS entries (similar items grouped)	What it trains	Mode
Commands / CA	Early Command Training; CA ODT Optimization; Command Voltage Centering; Late Command Training; CMD CTL CLK Slew Rate; CMD/CTL Drive Strength; CMD/CTL Tx Equalization; DIMM CA ODT Training	Command/address path, its termination, drive strength, and equalization.	Auto
Initial read	**SenseAmp Offset Training; Early ReadMPR Timing Centering 2D; Read MPR Training; Receive Enable Training**	Preparation of receivers and MPR data-capture boundaries.	**Auto; do not disable Receive Enable**
Write	**Jedec Write Leveling; Early Write Time Centering 2D; Unmatched Write Time Centering 1D; Write Timing Centering 1D/2D; Write Voltage Centering 1D/2D**	Write leveling/centering; Unmatched details are undisclosed.	**Auto; do not disable JEDEC WL**
Read	**Early Read Time Centering 2D; Read Timing Centering 1D/2D; Read Voltage Centering 1D/2D; RxVref Per-Bit Training**	Read-eye center in time/voltage and RxVref Per-Bit Training.	**Auto; change Early Read Time 2D only as a separate A/B test**
ODT / RON	**DDR5 ODT Timing Config; Read DQS ODT Training; Read DQ ODT Training; Dimm ODT Training; DIMM RON Training**	DQ and DQS are separate; enter manual resistances from the trained baseline.	**Auto**
EQ / DFE	**Read Equalization Training; Read CTLE Training; DIMM DFE Training; Ddr5 Rx Cross-Talk Cancellation; Write Drive Strength; Write Equalization**	Correction of frequency-dependent loss, reflections, and crosstalk.	**Auto; do not disable DFE without an A/B test**
Compensation	TxDqTCO Comp Training; ClkTCO Comp Training; Pre Training Comp Calibration; Comp Optimization; Ref PI Calibration; Rx SAL Calibration; VccClk FF Offset Correction; Data PI Linearity Calibration; Unmatched Rx Calibration; LVR Auto Trim	Phases, delays, PVT, and PHY power; do not transfer between CPUs/BIOS versions.	Auto

Group	BIOS entries (similar items grouped)	What it trains	Mode
DCC	Duty Cycle Correction Training; Downstream; QCLK; Rise/Fall; Functional DCC for DDR5 DQS, CLK and Data DQ	Extended duty-cycle correction for different DDR5 paths.	Auto
Mapping / ranks	**DQ/DQS Swizzle Training; Write Rank-to-Rank Training; Read Rank-to-Rank Training; Turn Around Timing Training; Write DQ/DQS Retrain**	Line mapping, rank-to-rank transitions, and DQ/DQS retraining.	**Auto; TAT Disabled with manual tertiary timings**
Margin / protection	Rank Margin Tool; Rank Margin Tool Per Bit; Retrain Margin Check; Margin Check Limit; Margin Limit Check L2; Row Hammering Prevention; Post Package Repair	Signal-margin checks, retraining decisions, and data protection. Stress tests in the OS are performed separately.	Auto; margin checks for diagnostics only
Service	**View Pin Calibration; Power Saving Meter Update; Read Vref Decap Training; Vddq Training; DIMM SPD Alias Test**	Service calibrations and checks; internal logic is not fully disclosed.	**Auto; disable Vddq Training only as a separate A/B test**
Not for DDR5 DIMMs	Functional DCC for LP5 WCK; Duty Cycle Correction for LP5 DCA	LPDDR5 entries in the shared menu do not apply to UDIMM/CUDIMM.	Not applicable

WHAT CANNOT BE CARRIED OVER LITERALLY FROM Z790

E25061 has no separate Round Trip Latency entry. If one appears in the BIOS, record the version and test it separately. With manual tertiary timings, I leave TAT Disabled (§6.9). Start with Vddq Training on Auto on Z890; test the Z790 disabling scheme separately. Enabled is not a universal recommendation for Early Read Time 2D on Z890.

DOCUMENTATION REVIEWED: ASUS ROG Z890 Series BIOS Manual E25061, pp. 29-32; the actual menu in the specific firmware takes precedence.

5.7 RTL/IOL training

WHAT RTL IS ON DDR5

RTL is Round-Trip Latency, the delay of the full read path. In Intel documentation for Alder Lake / Raptor Lake, it is the interval from the READ command until the first data returns to the memory controller, expressed in QCLK cycles. Training selects receiver parameters while accounting for the CPU, motherboard, modules, and settings. RTL describes the interval from READ until the first data returns to the controller; CAS describes the interval from READ until DRAM begins outputting data. AIDA64 measures access latency in its own test.

IOL is I/O Latency. On DDR4, it is a separate I/O delay setting. On DDR5, receiver parameters and their availability depend on the platform and BIOS; the old RTL/IOL pairing cannot be carried over.

Conditional conversion of RTL to time

The conversion below applies when the displayed RTL value corresponds to a number of QCLK cycles and tQCLK = Gear × tCK has been confirmed for the selected mode. Check the output format and scaling for the specific platform and utility version. This correspondence has not been confirmed for ATC 4.1.7 on Apex Encore / Raptor Lake / BIOS 2202: the examples are conditional.

tCK = 2000 / S ns • tQCLK = G x tCK • tRTL = R x tQCLK

S is the effective data rate in MT/s: for DDR5-8200, use 8200. The corresponding memory clock frequency is 4100 MHz.

G is the Gear ratio (2 or 4), and R is the RTL value in QCLK.

Conditional example: 8200, Gear 2, RTL 65: tCK = 2000/8200 ≈ 0.244 ns; tQCLK = 2 x tCK ≈ 0.488 ns; tRTL = 65 x tQCLK ≈ 31.71 ns.

WHAT TO USE AS YOUR REFERENCE

The main reference is **repeatability on your own stable profile**. Under identical conditions, a higher RTL, a new spread between corresponding entries, and boot-to-boot jumps are warning signs, especially when accompanied by repeated POST attempts, test errors, or performance loss.

1. Create comparable conditions. Save frequency, Gear, CAS, voltages, BIOS, and ME in a profile. Compare several full training cycles in the same scenario: a reboot with MRC Fast Boot may reuse a saved result.

2. Record the result of each boot. Compare the same active controller, subchannel, and rank positions. Note boot time and Karhu / y-cruncher errors; measure performance the same way each time.

3. Change one parameter. If the result varies, test a lower frequency or looser CAS, then voltages separately. Repeat training and tests to verify reproducibility.

WHY THE RESULT MAY CHANGE

Factor	What to check
Frequency and CAS	High frequency and tight timings reduce stability margin. Returning to a validated profile helps distinguish the overclocking limit from a random training result.
Voltages	An unsuitable memory or controller voltage, including too much voltage, can reduce stability. RTL cannot identify the required power rail or direction of adjustment.
BIOS and boot	BIOS / ME version, Auto rules, and reuse of training results can change the comparison conditions. After changing BIOS, first establish a new baseline series of boots.

MANUALLY LOWERING RTL IN BIOS

For **EVGA DARK**, the community reported RTL reductions of 1-2, supposedly by lowering CAS: the RTL block would then train according to the selected CAS. **ASUS Z790** documents RTL Init / Max, a signed Offset, and rank fields. I tested these blocks and concluded that they should remain on Auto. The motherboard should perform the training itself. If the result is unusable, diagnose it (see the glossary). For **Z690 Tachyon**, there are reports that manual entry does not work and recommendations to enable RTL training; no conclusion has been established for Z790.

BEHAVIORAL VALIDATION IS WHAT MATTERS

Passing POST does not prove OS stability, and errors in the OS alone do not prove an RTL training failure. There is no universal "correct" RTL or permissible spread for all DDR5.

DOCUMENTATION REVIEWED: Intel RTL; Intel Gear; ASUS MRC; ASUS RTL; EVGA DARK / OC; Tachyon / HWBOT

anta777 EMPIRICAL FORMULA

anta777 has an empirical formula for estimating RTL. Effective DDR5 data rate in MT/s and CAS in cycles are entered into it, and the result is used as an approximate reference.

X = S / 800 + tCL + 19

8200 @ tCL38: 67.25 • 8200 @ tCL36: 65.25 • 8400 @ tCL38: 67.5

A technically exact universal relationship has not been confirmed. Do not force every utility entry to 65 / 66. The rule that "RTLA rounds down and RTLB rounds up" cannot be considered universal: when the fractional part is below 0.50, the lower integer RTLB value also occurs. The observation applies to the readings in this case; these data cannot establish the BIOS rounding algorithm.

XTREEM CASE STUDY: 8200 AND 8400 MT/s

ASUS ROG Maximus Z790 Apex Encore, TEAMGROUP T-Force XTREEM 2 x 24 GB, Gear 2. We compare ATC readings for three profiles: 8200 @ tCL38, 8200 @ tCL36, and 8400 @ tCL38.

ATC entry	Controller and DDR5 path	8200 @ tCL38	8200 @ tCL36	8400 @ tCL38
MC0 C0 A1/A2	MC0, group A, subchannel C0	72/25	70/25	72/25
MC0 C1 A1/A2	MC0, group A, subchannel C1	67/25	65/25	67/25
MC1 C0 B1/B2	MC1, group B, subchannel C0	73/25	71/25	73/25
MC1 C1 B1/B2	MC1, group B, subchannel C1	67/25	65/25	67/25

How to read an entry. MC0 / MC1 are controller blocks; C0 / C1 are the two 32-bit DDR5 paths within each block. A1/A2 and B1/B2 label groups of positions in ATC. Apex Encore physically has two slots.

What 70/25 means. The slash separates two RTL readings in one entry. 70 applies to the occupied position; 25 in the second position matches Intel's reset value of 0x19. For this 1R kit, 25 is consistent with an unused position.

Relationship to the formula. At 8200, C1 matches the lower integer from the anta777 estimate: 67.25 -> 67 at tCL38, 65.25 -> 65 at tCL36. At 8400 @ tCL38, the estimate is 67.5, but C1 stays at 67; the entire RTL block matches 8200 @ tCL38. C0 is 5 / 6 above C1. The formula does not directly describe the whole block; the screenshots do not explain the offset or rounding algorithm.

The basic validation remains the same: several full training cycles, comparison with a stable profile, tests, and identical performance measurements. My 8200 @ tCL36 profile also showed RTL 64/65. One screenshot proves neither normal behavior nor an error. Under the confirmed conversion conditions in Section 5.7 (p. 82), at 8200 MT/s and Gear 2 one QCLK is approximately 0.488 ns: a difference of 5-6 conditionally corresponds

to 2.44-2.93 ns. The ATC 4.1.7 scaling on this system has not been confirmed. The calculation gives the duration of the read interval under consideration. Overall system latency and stability margin are assessed through separate measurements and tests.

I treat Apex and other prominent 2-DIMM motherboards as the benchmark for correct, fast RTL training when comparing them with other boards, especially 4-DIMM models.

WHAT TO ACCOUNT FOR ON Z890

On Z890 / Core Ultra 200S, use documentation and a utility intended for that platform: field names, units, and training procedures may differ. ASUS BIOS includes **Training Consistency**, which may improve training repeatability but does not replace testing. Z790 numbers and offsets, including the anta777 estimate, cannot automatically be treated as targets for Z890.

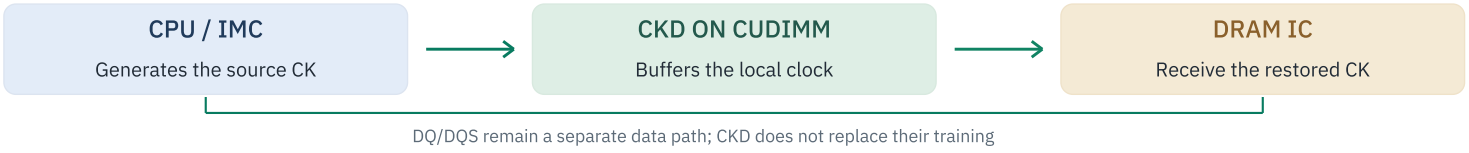
DOCUMENTATION REVIEWED: Intel RTL; ASRock Z790; anta777 / RTL; ASUS Z890

5.8 Z890 training features

The public menu separates Read DQ/DQS ODT more precisely, exposes more PHY calibrations, and adds Training Consistency and the DIMM Fit family. The absence of an old name does not prove removal of the algorithm: it may have been merged, renamed, or hidden within the MRC.

Category	Examples	How to interpret the change
Retained	MCH Full Check; Training Profile; Mrc Training Loop Count; margin tools	The principle is unchanged; margin and the result depend on the new IMC/PHY and BIOS.
Renamed / split	MRC Fast Boot -> Fast Boot; Read ODT -> Read DQS ODT + Read DQ ODT	Compare by function, but do not treat every name as a direct 1:1 mapping.
Exposed for the first time	CA ODT Optimization; CTLE; RxVref Per-Bit; crosstalk; rank-to-rank; DCC	More observation points, but you should not switch each one manually
Not visible as a separate entry	RTL, Max RTT_WR, Write Slew Rate, Read Amplifier, TxDqsTCO, Memory Test, and other Z790 entries	They are not listed in the public Z890 manual, but may still be used by the MRC.

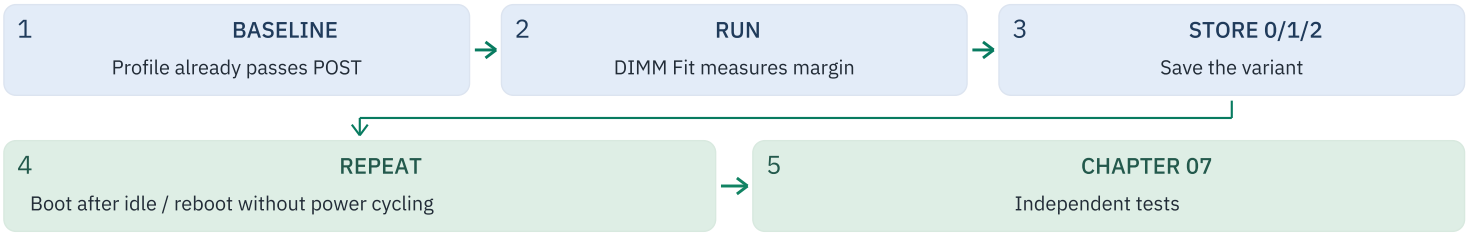
CUDIMM: CKD RESTORES THE CLOCK, MRC TRAINS THE DATA PATH



CKD MODES AND AEMP III

The public ASUS Z890 BIOS manual lists no separate CKD Training entry. Single PLL, Dual PLL, and Bypass determine how CKD handles the clock signal. Gear 2/Gear 4 set the ratio of controller frequency to memory frequency, while MRC initializes and trains the memory subsystem. AEMP III is described as a two-stage process: first the clock driver, then memory frequency.

DIMM FIT: AUTOMATIC SEARCH FROM A GIVEN STARTING POINT



Function	What is available	Practical caveat
DIMM Fit	Store0 / Store1 / Store2 and deletion of the selected Store	Run it from a bootable baseline; the result is not yet a daily profile.
DIMM Fit Pro	Up to 20 parameters with ranges; Fail to Next advances to the next parameter early.	The transition criterion follows the BIOS User Guide. ASUS recommends 2 cycles; do not turn off power.
Training Consistency	A feature intended to improve the repeatability of training results	Only when full retraining varies; start with Auto.

WHAT REMAINS VALID AFTER AUTOMATIC TUNING

DIMM Fit optimizes parameters only relative to the current starting point. After changing frequency, Gear, voltage, kit, or CKD mode, repeat training and tests for the saved Store. CKD improves clock-signal quality on CUDIMM. Reliable reads and writes also depend on Vref/ODT settings and memory temperature. Achievable Z890 frequency is assessed for the entire configuration: CPU, motherboard, BIOS, modules, CKD mode, and Gear.

DOCUMENTATION REVIEWED: ASUS ROG Z890 BIOS Manual and Z890 Apex page; ASUS DIMM Fit/DIMM Fit Pro FAQs; Renesas RG5C172C CKD datasheet.

5.9 Resistances: ODT, RTT, RON

ODT is on-die line termination. RTT sets its effective resistance; RON is the output resistance of the transmitter. A lower RTT strengthens termination; a lower RON lets the transmitter drive more current at the same voltage. Tuning these settings helps match the driver to the termination and reduce signal reflections.

> ### AUTO FOR EVERYDAY TUNING
>
> There is no single set of resistance values that is correct for every configuration. The table lists settings and observations from specific systems; applying them to another system requires testing.
>
> Start with Auto: the BIOS/MRC selects values using firmware tables and training results. For everyday memory tuning, most users should leave the resistance settings on Auto. Manual tuning can help near the overclocking limit or with training failures; 2R, 2DPC, or a weak IMC may call for it sooner.

RESISTANCE SETTINGS AND THEIR ROLES

Parameter	Role	Tuning options	Validation
RTT_WR	Termination on the target rank during a write	An adjacent resistance after testing Auto	Memory tests after several full training cycles
RTT_NOM_RD / WR	Termination on a non-target rank while another rank is being read or written, when the controller activates NT ODT	Change NOM RD and NOM WR separately; particularly useful with 2R/2DPC	Reads, writes, and rank-to-rank transitions
RTT_PARK / DQS	DQ/DQS termination on a parked rank	Change PARK and PARK DQS separately	Memory tests, boots after idle, and reboots
DRAM RON	DRAM output drive during reads	Test Pull-up and Pull-Down separately	Reads and repeatability of full training
CA / CS / CK ODT	Termination for commands, rank select, and clock	Try Group A/B settings when POST or training failures recur	Several boots after idle with full training

PUBLISHED EXAMPLES

The data rate in the table describes a specific test. The comparison also needs to account for Gear, BIOS, memory, and the test/benchmark methodology. Resistance values are in ohms.

Config and date	MT/s	Published settings	Result and limitations
Z790 APEX; BIOS 1801; CPU —; DDR —; 02.2024	8400–8600	RON PU/PD: 40/34; 34/40. RTT and Groups: Auto.	Veii: advice for comparison with Auto, with an explicit PCB dependency. The system and test protocol are only partly documented.
Z790 APEX ENCORE; CPU —; DDR —; 02.2024	8533 CL36; VDD/VDDQ 1.63/1.47 V	RON PU/PD: MC00 48/40; MC01 40/48, using the author's labels. The full RTT set needs clarification.	tibcsi0407 reported an improvement after TX tuning. These are experiments on one system; 8600 remains the next target.
Z890 APEX; BIOS 3202; 285K; 2x16 (Hynix A-Die); 30.06.2026	8800 for tuning; 8600 CL40, G2; VDD/VDDQ 1.45/1.45 V	A1: RTT NOM RD 48. B1: RTT NOM RD 60, NOM WR 40, PARK DQS 120. Other BIOS readings are listed below.	UNIKO: after ODT tuning, RunMemtestPro reached 100% coverage; VT3 failed in iteration 10. Further progress followed voltage tuning.
Z890 APEX; BIOS 1901; 285K; 2x24 (Hynix M-Die); 29.07.2025	9600 CL48, G4; DRAM 1.45 V	RTT, ODT, RComp, and training: Auto, according to the LAB501 summary dated 21.10.2026.	LAB501: Prime95 LargeFFT with memory filled. Run duration and boot repeatability need clarification. The screenshot shows 4800 MHz DRAM and a 1200 MHz controller: Gear 4.
Z890 APEX; BIOS 1401; 285K; 2x24 (Hynix M-Die); 10.02.2025	10 133 CL46, G4; DRAM 1.50 V	RTT, ODT, RComp, and training: Auto. Exact BIOS readings need clarification.	LAB501: Apex and Tachyon ICE comparison. The screenshot of the earlier Apex result shows SuperPI 1M completed in 6.718 s, with DRAM at 5066.7 MHz and the controller at 1266.7 MHz (G4). Extended stress tests and boot repeatability for this setting still need separate validation.
Z790-P WIFI; BIOS AD3; 13900KF; 2x32 (Hynix A-Die); date —	6800 CL32; VDD/VDDQ 1.40/1.40 V	DQ RTT: WR 34; NOM RD 40; NOM WR 40; PARK 34; PARK DQS 34. ODT Finetune: 2 (setting index).	vintologi24: stressapptest reported 1 error over 8567.82 s (~2 h 23 min). After further tuning, the author reported 13 h of various tests without errors. He later noted an mprime Large FFT failure with similar settings. RTT values stayed the same while voltages, timings, and training settings changed. These are stages of tuning one system.
Z790 APEX; BIOS 2002; CPU —; DDR —; 27.02.2024	8000 CL36, G2; VDD/VDDQ 1.50/1.47 V	Both exported blocks list DQ RTT: WR 40; NOM RD 40; NOM WR 34; PARK 34; PARK DQS 34. Group B CA/CS/CK: 60/40/40. RON PU/PD: 48/40; 40/48, in export order. DIMM ODT, DIMM RON, and Read ODT Training: Disabled.	zebra_hun, posts #13741 and #13751: TM5 passed, but VT3 failed after about 30 min, compared with roughly 10 min before the BIOS update. The author published the full profile. This result covers the complete setup with BIOS 2002; the comparison does not isolate the contribution of the resistances.
Z790 APEX ENCORE; 14900KS; DDR —; 27.05.2024	8600 CL36; VDD/VDDQ 1.62/1.60 V	DQ RTT NOM RD 80; NOM WR 80. "RON ODT 48–40–40–48" is the author's notation; the PU/PD mapping to channels needs clarification. VDD/VDDQ 1.62/1.60 V; MC 1.45 V; TX 1.35 V.	elmariachi: settled on 8600 CL36; memory reached 37.5 °C in TM5 with a fan. At SA 1.23 V and above, the system froze in TM5; he used 1.22 V. BIOS, kit capacity, the other RTT values, and TM5 duration and configuration need clarification.

BIOS VALUES AND LABELS

Z790 Apex / Z790 Apex Encore: the ASUS manuals list DQ RTT WR / NOM RD / NOM WR / PARK / PARK DQS values of 34/40/48/60/80/120/240 Ω; DRAM RON Pull-up/Pull-Down values of 34/40/48 Ω; and Group A/B CA/CS/CK ODT values of 40/60/80/120/240/480 Ω.

The ASUS Z890 manual lists RTT values of 34/40/48/60/80/120/240 Ω and DRAM RON Pull-up/Pull-Down values of 34/40/48 Ω. These are the available menu options. Auto leaves the choice to the firmware; Disabled turns termination off.

Group A/B are termination groups for the DRAM devices on a module; CHA/CHB are motherboard channels. Micron explains the grouping. Match PU/PD pairs to the full BIOS field names. DRAM RON applies to the memory transmitter; CPU drivers have their own controls.

On Z790, Max RTT_WR caps RTT_WR selection during Power Training. A manual resistance is entered in the separate DQ RTT WR field.

UNIKO: BIOS SCREENSHOTS

The A1 and B1 screenshots show four manual settings and numbers beside Auto fields. Each cell below gives the number to the left of the field, followed by the selected setting. Sync Basic Dimm ODT mode is Enabled.

Field	Channel 1 Slot A1: number / setting	Channel 0 Slot B1: number / setting
RTT WR	60 / Auto	60 / Auto
RTT NOM RD	48 / 48 Ω	60 / 60 Ω
RTT NOM WR	0 / Auto	40 / 40 Ω
RTT PARK	0 / Auto	0 / Auto
RTT PARK DQS	80 / Auto	120 / 120 Ω
Pull-up Output Driver Impedance	34 / Auto	34 / Auto
Pull-Down Output Driver Impedance	34 / Auto	34 / Auto

UNIKO: TUNING RESULTS

In the UNIKO test at 8600, after ODT tuning, RunMemtestPro reached 100% coverage, while VT3 failed in iteration 10 after about 20 minutes. After the next voltage-tuning stage, VT3 failed in iteration 16. After setting MC Voltage Calculation Voltage Base to 1.16 V, the author reported 30 VT3 cycles, about an hour. This result combines ODT and voltage tuning.

The system used an open bench and a fan over the memory; room temperature changed during the work. The result applies to this configuration. Repeatability of boots after idle still needs a separate check.

CUDIMM AND DIMM FIT

On a CUDIMM, the clock signal is handled by the CKD, a separate chip on the module. In Single PLL and Dual PLL modes, it restores the clock signal; in bypass mode, it passes the signal around the PLL. CK ODT applies to termination on this clock path, while DQ RTT applies to the data lines.

ASUS DIMM Fit automatically tunes memory parameters and saves the result in a Store. The Pro version lets users select parameters and search ranges, including voltage settings. Support depends on the motherboard and BIOS. ASUS explains that Completed Successfully means the tuning procedure has finished; separate test results show how stable the profile is under load.

METHOD FOR COMPARING RESULTS

Save the Auto profile and BIOS readings, change one parameter, then repeat full training and the same tests. Return to the starting profile and compare the result. Record the board, CPU, memory kit, BIOS, Gear, voltages, cooling, and temperature. For each test, note its version, settings, duration, and errors; for boots, record successful attempts out of the total. Improvements, regressions, and results matching Auto are all worth recording.

5.10 BIOS profiles and recovery

Save a working step after each completed stage. Then a failed timing or voltage change will not force you to rebuild the profile: you can quickly return to the last repeatable point and test the next hypothesis separately.

Changing frequency or Gear requires retesting voltage ranges and training repeatability. When changing the CPU, kit, capacity, occupied slots, BIOS version, or UDIMM/CUDIMM type, it is safer to start from the baseline profile.

PROFILE LADDER: ROLLBACK SHOULD TAKE SECONDS



RECOVERY ORDER AFTER A FAILED POST

Step	Recovery	What to do	What is preserved
1	Wait	DDR5 training can take noticeable time; assess Q-Code and repeatability	Entire profile
2	ReTry	Retry POST with the same settings	Entire profile
3	Safe Boot	Safe boot: temporarily load conservative parameters and correct the OC	Manual fields
4	Working step	Load the previous profile	Validated baseline
5	Clear CMOS	Clear settings if BIOS is inaccessible; use FlashBack (BIOS recovery) only for a firmware problem	Previously exported copy

SAVE INTERMEDIATE PROFILES

Saved steps help isolate a change and roll back quickly. The criteria for a completed daily profile, checks of boots after idle and reboots, and the test suite are covered in Section 7.9.

KEEP A COPY OUTSIDE CMOS

Export the profile to a USB drive and save screenshots of changed pages, the BIOS version, and a brief configuration description alongside it. A profile file may become incompatible after a firmware update, while the screenshots remain readable.

DOCUMENTATION REVIEWED: Methodology of this revision; ASUS Apex Encore User Manual and Z790/Z890 BIOS Manuals. The detailed test suite is in Chapter 07.

06 / Training algorithms

> **FOR EVERYDAY MEMORY TUNING**
>
> The purpose of this chapter is to explain how the TRAINING ALGORITHMS controls work. For the average user, the practical rule is simple: leave 98% of these settings on **AUTO**. Changing them makes sense when you have a specific training problem and understand what you are testing.

This section covers Z790 Apex, Z790 Apex Encore, Z890 Apex, and other ASUS motherboards. Setting names were checked against the ASUS manuals, and the corresponding software values against Intel FSP.

The following settings provide a starting point and options to test when training causes problems. **AUTO does not always leave the setting ENABLED:** the BIOS decides, and an option appearing in the menu does not necessarily mean it is used for DDR5. **DISABLED does not lock in the previous training result:** other algorithms may change the same parameters.

6.1 Command/address path

These algorithms align the CMD/CTL command and control signals with the CLK clock signal, select command detection thresholds, and tune the electrical characteristics of the output drivers.

Early Command Training — ECT

What it does. Finds an initial working alignment of the command and control signals relative to CLK for the subsequent stages.

Practical choice. **AUTO**. Test ENABLED separately if full training fails with a new profile.

Key detail. The older implementation handles LPDDR. The specific CA/CS passes for DDR5 on Z790/Z890 have not been publicly confirmed.

Command Voltage Centering — CMDVC

What it does. Centers command Vref, the threshold for detecting commands.

Practical choice. **AUTO**; test ENABLED with automatic command Vref and inconsistent training results. DISABLED if centering repeatedly produces poor results or when manually tuning the same Vref.

Key detail. DDR5 has VrefCA and VrefCS; the exact scope of this BIOS stage has not been disclosed.

Early Command Voltage Centering

What it does. The name suggests early command Vref tuning; the exact implementation and how it differs from CMDVC have not been established.

Practical choice. **AUTO**.

Key detail. The option is listed for Z790; it is not listed in the Z890 manual reviewed.

Late Command Training — LCT

What it does. Performs late centering of CMD/CTL relative to CLK; the older code uses complex command patterns.

Practical choice. **AUTO**; ENABLED when selecting training stages manually while leaving command delays on automatic. Test DISABLED if this late adjustment reproducibly makes the result worse.

Key detail. Early and Late complement each other.

CMD CTL CLK Slew Rate — CMDSR

What it does. Tunes Slew Rate (the rate of voltage change at signal edges) for the command, control, and clock lines based on the operating window.

Practical choice. **AUTO** with automatic electrical settings. Test DISABLED when manually tuning the corresponding Slew Rate settings, or if the automatic stage reproducibly makes the result worse.

CMD/CTL DS & E 2D — CMDDSEQ

What it does. Jointly tunes command driver strength and transmitter equalization: Drive Strength × Tx Equalization.

Practical choice. **AUTO**; test DISABLED when manually tuning these parameters if the stage prevents the combination from being retained.

Key detail. Z890 lists separate CMD/CTL Drive Strength — CMDDS and CMD/CTL Tx Equalization — CMDTXEQ controls.

CMD/CTL Drive Strength Up/Dn 2D — CMDDRUD

What it does. Separately tunes the pull-up and pull-down strengths of the command drivers: pull-up × pull-down.

Practical choice. **AUTO**; test DISABLED when manually tuning the command Up/Dn settings specifically, or when automatic training repeatedly produces a poor result.

Key detail. The corresponding option/flag was not found in the Z890 manual reviewed or in the Arrow Lake-S interface.

6.2 Initial read setup

These stages calibrate the integrated memory controller (IMC) receivers, find an initial region of valid reads, and determine when to open the receive window. The BIOS retains the MPR name. In DDR5, training patterns are configured through dedicated MR registers: serial, clock, and LFSR (Linear Feedback Shift Register) patterns are provided.

SenseAmp Offset Training — SOT

What it does. Calibrates the inherent electrical offset of the CPU's DQ/DQS input receivers, compensating for variation in their detection thresholds.

Practical choice. **AUTO**. At the overclocking limit, if results differ between training runs, test DISABLED separately; keep it only if boot behavior and test results improve repeatably.

Early ReadMPR Timing Centering 2D — ERDMPRTC2D

What it does. Searches for an initial read region across DQ/DQS timing and RxVref. The older algorithm centers timing at different RxVref values using a known pattern, without requiring functional writes to normal memory.

Practical choice. **AUTO**. Test ENABLED separately if full training fails or produces inconsistent results.

Key detail. Early Read Time Centering 2D uses normal test traffic.

Read MPR Training — RDMPRT

What it does. Aligns DQ reads relative to DQS using a known pattern: finds the timing boundaries of the operating window and selects a position within it.

Practical choice. **AUTO**; ENABLED when manually enabling the basic training stages.

Receive Enable Training — RCVET

What it does. Locates the arrival of the DQS preamble and sets when the receive window opens — DQS gating.

Practical choice. **AUTO**; ENABLED when manually enabling the basic training stages. Disable it only to diagnose a specific, reproducible failure.

Receive Enable Centering 1D — RCVENC1D

What it does. Further centers Receive Enable along the timing axis.

Practical choice. On Z790 Apex / Encore — **AUTO**.

Key detail. The older Coffee Lake description includes LPDDR Only. The option/flag was not found in the Z890 manual or the Arrow Lake-S IoT FSP reviewed.

> **HOW TO COMPARE THE SETTINGS**
>
> I start with AUTO wherever it is available. For the comparison, I disable MRC Fast Boot (Fast Boot within the memory settings on Z890). I change one switch at a time, perform several boots after idle with full training, and check the frequency, full memory capacity, and stability after different training runs.

6.3 Write training

These algorithms align the write strobe DQS with the CK clock signal, then center the data relative to DQS and tune the VrefDQ threshold on the DRAM side.

Jedec Write Leveling — JWRL

What it does. Aligns DQS relative to CK on the memory side, compensating for the difference in their delays. The controller uses feedback from DRAM to position the write strobe.

Practical choice. **AUTO**; ENABLED when controlling the basic training stages manually.

Key detail. DDR5 also provides compensation for mismatched internal DQ/DQS paths.

Early Write Time Centering 2D — EWRTC2D

What it does. Performs a preliminary search for a working write region: centers DQ/DQS timing at several DRAM VrefDQ values and selects a suitable starting point.

Practical choice. **AUTO**. Test ENABLED or DISABLED separately when troubleshooting full training.

Key detail. In the older MRC code reviewed, this stage is allowed only for DDR4. The field in current FSP does not disclose the conditions under which it runs for DDR5. The Z790 manual uses Timing instead of Time in the name.

Write Timing Centering 1D — WRTC1D

What it does. Finds the write window and centers DQ timing relative to DQS at the current VrefDQ.

Practical choice. **AUTO** where available; in menus with only ENABLED / DISABLED, start with ENABLED. Keep the selected basic centering mode when enabling the late 2D pass.

Key detail. E21287 and E22758 for Z790 offer only ENABLED / DISABLED; E25061 for Z890 also offers AUTO.

Write Voltage Centering 1D — WRVC1D

What it does. Centers VrefDQ, the internal threshold for detecting write data in DRAM, at the current DQ/DQS timing position.

Practical choice. **AUTO**; ENABLED when manually enabling the basic training stages. Test DISABLED if centering repeatedly produces poor results or when manually tuning this same DRAM VrefDQ.

Key detail. Even with manual VDD/VDDQ settings, the DRAM VrefDQ threshold is tuned separately.

Write Timing Centering 2D — WRTC2D

What it does. Refines the DQ/DQS timing position, accounting for changes in the operating window at different VrefDQ values.

Practical choice. **AUTO**. At a borderline overclock, test ENABLED separately if stability varies after repeated training. Keep DISABLED only if it produces a repeatable improvement over the initial mode.

Key detail. The reference stage may include per-bit deskew: individual compensation for timing variation between bits.

Write Voltage Centering 2D — WRVC2D

What it does. Measures the voltage boundaries of the operating window at several DQ/DQS timing offsets and uses the combined results to refine VrefDQ.

Practical choice. **AUTO**. Test ENABLED separately if stability after training is borderline. DISABLED if centering is demonstrably poor or when manually tuning the same VrefDQ.

> Z890: Unmatched Write Time Centering 1D is a separate option with the UNMATCHEDWRTC1D flag; see §6.12.

6.4 Read training

These algorithms tune the DQ sampling time relative to DQS and the RxVref threshold in the memory controller's receive path. Unlike write training, they tune the CPU side.

Early Read Time Centering 2D — ERDTC2D

What it does. Performs a preliminary search for a read operating point across DQ/DQS timing and RxVref; the reference code checks it using normal test traffic.

Practical choice. **AUTO**. Compare ENABLED / DISABLED separately when troubleshooting full training.

Key detail. In the older MRC code reviewed, ERDTC2D is restricted to DDR4; the conditions used by the current DDR5 implementation have not been disclosed. The Z790 manual spells the name Early Read Timing Centering 2D.

Read Timing Centering 1D — RDTC1D

What it does. Finds the timing boundaries for receiving data and centers the DQ sampling time relative to DQS on the controller side at the current RxVref.

Practical choice. **AUTO**; ENABLED when controlling the basic training stages manually. When enabling RDTC2D, keep the selected RDTC1D mode: basic and subsequent centering may run one after the other.

Read Timing Centering with JR

What it does. A separate read timing centering variant in the Z790 menu. How it differs from RDTC1D has not been established.

Practical choice. **AUTO**.

Key detail. The meaning of JR has not been confirmed. This option is not listed in the Z890 manual reviewed.

Read Voltage Centering 1D — RDVC1D

What it does. Centers RxVref, the memory controller's data detection threshold, at the current DQ/DQS timing position.

Practical choice. **AUTO**; ENABLED with automatic RxVref when controlling the basic training stages manually. Test DISABLED for poor results or manual RxVref tuning, provided a comparison confirms that this pass is interfering.

Key detail. Even with manual VDDQ or SA settings, the RxVref threshold is tuned separately.

Read Timing Centering 2D — RDTC2D

What it does. Refines the data sampling time based on the shape of the operating window at different RxVref values.

Practical choice. **AUTO**. At a borderline overclock, test ENABLED separately if stability varies after repeated training. Keep DISABLED only if it produces a repeatable improvement.

Key detail. The reference stage may perform per-bit deskew: individual compensation for timing variation between bits.

Read Voltage Centering 2D — RDVC2D

What it does. Refines RxVref using the voltage boundaries of the operating window, measured at several DQ/DQS timing offsets.

Practical choice. **AUTO**. Test ENABLED separately with inconsistent training results and automatic RxVref. DISABLED if centering is confirmed to be poor or when manually tuning the same threshold.

> Z890: RxVref Per-Bit Training is a separate option with the RXVREFPERBIT flag; see §6.12.

6.5 Termination and transmitters

ODT provides termination for impedance matching; RON and Drive Strength set transmitter output resistance and drive strength. Slew Rate (the rate of voltage change at signal edges) and equalization change the signal shape.

Dimm ODT Training — DIMMODTT

What it does. Tunes DRAM termination based on read and write margins. The full set of DDR5 RTT settings searched by a particular BIOS has not been disclosed. DISABLED skips this tuning stage; termination itself continues to operate.

Practical choice. **AUTO** with automatic RTT settings. Test ENABLED if training results are inconsistent; DISABLED if the stage overrides manually tuned RTT settings or makes the result worse.

Max RTT_WR

What it does. Sets the upper limit for automatic RTT_WR tuning in power training. Options: ODT OFF and 120 Ohms. The final RTT_WR is selected during training within this limit.

Practical choice. **BIOS DEFAULT VALUE**. Test 120 Ω separately. ODT OFF sets the RTT_WR search limit here; DIMM termination as a whole remains active.

DIMM RON Training — DIMMRONT

What it does. Tunes the DRAM driver's output resistance during reads: memory → CPU. RON applies to the transmitter, RTT to termination.

Practical choice. **AUTO**. Test DISABLED with manual DRAM Output Driver Impedance if training interferes with it. If only RTT or CPU Write Drive Strength is being changed, the DIMM RON Training mode can remain as it was.

Read ODT Training — RDODTT

What it does. Tunes the CPU receiver's termination during reads. DIMM RTT_NOM_RD sets termination on the memory side and is tuned separately. On Z890, CPU receiver termination training is split into Read DQ ODT Training and Read DQS ODT Training.

Practical choice. **AUTO**. Test DISABLED for manually tuned CPU Read ODT if the stage changes the result, or if automatic tuning repeatedly produces poor results. On Z890, compare DQ and DQS separately.

DIMM CA ODT Training — DIMMODTCA

What it does. Tunes command/address line termination on the DRAM side. The older code handles LPDDR4; the scope for DDR5 CA/CS/CK has not been disclosed. CA ODT Optimization is listed separately on Z890.

Practical choice. **AUTO**. Test DISABLED with manual CA ODT if this stage interferes with it.

Write Drive Strength/Equalization 2D — WRDSEQT

What it does. Jointly tunes CPU driver strength and write equalization: CPU → DRAM. The two dimensions are Drive Strength × Tx Equalization.

Practical choice. **AUTO**; test ENABLED if training results are inconsistent. DISABLED when manually tuning these parameters if the stage interferes with them. Write Drive Strength and Write Equalization are listed separately on Z890.

Write Slew Rate Training — WRSRT

What it does. Tunes the slew rate of CPU write signals.

Practical choice. **AUTO**. Test DISABLED with manual Write Slew Rate or if the pass makes the result worse.

Write Driver Strength Training — WRDS

What it does. Trains CPU write driver strength separately. The order and interaction of WRDS and WRDSEQT in the BIOS have not been disclosed.

Practical choice. **AUTO**. Test DISABLED if training overrides manual CPU Write Drive Strength. On Z890, the field with the corresponding name is Write Drive Strength.

Write Drive Strength Up/Dn independently — WRDSUDT

What it does. Separately tunes the pull-up and pull-down sides of the CPU write driver. DIMM Pull-up / Pull-down Output Driver Impedance applies to the driver on the memory module.

Practical choice. **AUTO**. Test DISABLED with manual CPU Drive Up/Dn settings or if training produces a poor result.

> Max RTT_WR, Write Slew Rate Training, and Write Drive Strength Up/Dn independently are not listed in the Z890 manual reviewed.

6.6 Receiver equalization

These algorithms tune the CPU receiver when reading from DRAM. The equalizer compensates for distortion in the incoming signal; amplifier training selects the operating mode of the analog circuitry.

Read Equalization Training — RDEQT

What it does. Tunes the CPU receiver's equalizer based on read timing and voltage margins. In the older MRC, the available settings depend on the receiver mode; the code includes CTLE and DFE.

Practical choice. **AUTO**. At a borderline overclock, test ENABLED separately if results differ between training runs. DISABLED if automatic tuning produces a poor result or when manually tuning the corresponding equalization.

Key detail. On Z890, Read CTLE Training is listed separately from Read Equalization Training.

Read Amplifier Training — RDAPT

What it does. In the older code, tunes the bias current or load of the CPU receiver's analog circuitry, depending on the mode. It considers read margin and, in the relevant mode, power consumption.

Practical choice. **AUTO**. At the overclocking limit, test DISABLED separately if there are repeatable signs of poor receiver-mode tuning. ENABLED allows tuning of the already active amplifier's operating mode.

Key detail. This option is not listed in the Z890 manual reviewed.

6.7 PHY calibration

These algorithms tune compensation codes, internal transmitter delays, power supplies, and reference circuits in the CPU memory PHY.

Comp Optimization Training

What it does. In the older MRC, moves the shared portion of byte-group corrections into global compensation, reducing local offsets while aiming to preserve the overall result. Handles Write Drive Strength, Read ODT, and, in some branches, Slew Rate.

Practical choice. **AUTO**. Test DISABLED if this stage causes problems or when investigating manual compensation offsets. This stage can remain enabled with manual RTT or Drive Strength settings. Hardware compensation also works when training is disabled.

Key detail. Z890 lists Comp Optimization and Pre Training Comp Calibration separately.

TxDqTCO Comp Training — TXTCO

What it does. Tunes delay compensation for the DQ output path during writes: CPU → DRAM. The older MRC evaluates the write window.

Practical choice. **AUTO**; test ENABLED separately when training results are inconsistent, and DISABLED when this stage reproducibly makes them worse.

ClkTCO Comp Training — CLKTCO

What it does. Tunes delay compensation for the CLK output path. The older code evaluates the command window and also updates the CMD/CTL TCO codes; the exact scope of the current stage has not been disclosed.

Practical choice. **AUTO**. ENABLED can be tested when training is marginal.

TxDqsTCO Comp Training — TXTCODQS

What it does. Tunes delay compensation for the CPU-side write DQS output strobe.

Practical choice. **AUTO**, if available. Test DISABLED only when this stage causes a specific deterioration. No separate entry is listed in the Z890 manual reviewed.

VccDLL Bypass Training — VCCDLLBP

What it does. ENABLED allows testing the VccDLL power-supply bypass mode from VccIOG. Whether Bypass is entered depends on the test result; the DLL continues to operate.

Practical choice. **AUTO**. DISABLED is a diagnostic option if this stage causes problems. The setting is not listed in the Z890 manual reviewed.

PanicVttDnLp Training — PVTTDNLP

What it does. In the older MRC, tunes VttPanicCompDnLPMult for the pull-down branch of fast VTT correction, only for LPDDR with VTT termination.

Practical choice. **AUTO**. The setting is not listed in the Z890 manual reviewed.

Read Vref Decap Training — RDVREFDC

What it does. Tunes the programmable RxVref decoupling capacitances in the CPU receiver. The older code then provides for RxVref recentering.

Practical choice. **AUTO**; test ENABLED when read training results are inconsistent, and DISABLED when this pass makes them worse.

Vddq Training — VDDQT

What it does. The older, partly unfinished MRC describes tuning CPU TX VDDQ through FIVR based on command and write margins, only for LPDDR4/5. The role of this stage in controlling DRAM VDDQ through the PMIC remains unknown.

Practical choice. **AUTO**. With manual CPU TX VDDQ, test DISABLED separately if you suspect interference from this pass. If only DRAM VDDQ is set manually, you can retain the initial mode for this stage. My example in §5.5 applies only to the specified configuration.

6.8 Duty cycle correction (DCC)

Duty cycle is the fraction of a period for which a signal is high. DCC equalizes the high and low durations, usually toward 50/50.

Duty Cycle Correction Training — DCC

What it does. Calibrates the correction of high and low durations in the CPU memory interface.

Practical choice. **AUTO**. When explicitly controlling training stages, start with ENABLED; test DISABLED if a training problem is reproducible.

Key detail. The exact scope of the general Apex switch has not been disclosed. Z890 separately lists Downstream, QCLK Calibration, Rise/Fall, and Functional DCC for DDR5 DQS, DDR5 CLK, and Data DQ.

Periodic DCC

What it does. Allows periodic updates to duty cycle correction after the initial calibration. The interval and conditions for running it on DDR5 Apex have not been published.

Practical choice. **AUTO**. When selecting a mode explicitly, use DISABLED as the baseline for comparison; test ENABLED separately, including extended operation and transitions between idle and load.

Key detail. The setting appears in the Z790 E22758 manual; it is not listed in the earlier E21287 or in the Z890 E25061 manual.

Tx Dqs Dcc Training — TXDQSDCC

What it does. Tunes duty cycle correction for the CPU-side write DQS output strobe, for CPU → DRAM transfers.

Practical choice. **AUTO**; when selecting a mode explicitly, start with ENABLED. Test DISABLED if this stage reproducibly makes the result worse.

Key detail. No separate entry is listed in E25061; a connection to Functional DCC for DDR5 DQS has not been confirmed.

6.9 Read and turnaround latency

RTL determines when read data returns to the controller; TAT sets the intervals between bus operations.

Round Trip Latency — RTL

What it does. Optimizes the latency of data returning after a read command. In the older Ice Lake MRC, RTL is tuned together with receive FIFO delays, with read-window checks and a margin.

Practical choice. **ENABLED**. I always leave this stage enabled when tuning memory manually.

Key detail. Initial RTL values are already calculated during Receive Enable Training; a separate pass optimizes them. RTL is not listed in E25061. It is unknown whether the Read/Write Rank-to-Rank Training settings replace RTL.

Turn Around Timing Training — TAT

What it does. Tunes the intervals for read → read, read → write, write → read, and write → write, including rank changes. The older MRC optimizes the corresponding variants of tRDRD, tRDWR, tWRRD, and tWRWR, as well as CPU receiver ODT turn-on timing and duration.

Practical choice. **DISABLED**. I tune memory and tertiary timings manually, so I disable automatic tuning.

Key detail. The older MRC also tunes ODT with a single rank. TAT is retained on Z890.

6.10 DRAM-side signal tuning

DFE tunes data reception inside DRAM during writes; DCA adjusts the output waveforms during reads.

DIMM DFE Training — DIMMDFE

What it does. Trains Decision Feedback Equalization in the DRAM receiver during writes: CPU → memory. DFE accounts for previous bits and compensates for their effect on detecting the current bit.

Practical choice. **AUTO**. When explicitly controlling training stages, start with ENABLED; test DISABLED if training reproducibly produces poor results or when tuning DIMM DFE manually.

Key detail. Hardware DFE may also operate when training is disabled.

EARLY DIMM DFE Training — EARLYDIMMDFE

What it does. A separate early pass for tuning DRAM DFE. The exact search sequence and interaction with the main DIMM DFE stage in Apex BIOS have not been disclosed. It is unknown whether one pass can replace the other.

Practical choice. **AUTO**. Compare ENABLED and DISABLED separately for a specific training problem.

DRAM EMPHASIS Training — DRAMEMPHASIS

What it does. The purpose of this switch for DDR5 in Apex BIOS has not been disclosed.

Practical choice. **AUTO**.

DRAM DCA Training — DRAMDCA

What it does. Trains the Duty Cycle Adjuster inside DRAM: adjusts the high and low durations of the DQ/DQS outputs during reads, memory → CPU. The goal is to reduce duty cycle distortion, bringing the durations closer to 50/50.

Practical choice. **AUTO**. When explicitly controlling training stages, start with ENABLED; test DISABLED if training reproducibly gets worse.

DQS OFFSET ADJUST Training — DQSOFFSETADJUST

What it does. The implementation of this pass in Apex BIOS has not been disclosed. DDR5 provides Read DQS Offset Timing through MR40: the DQS strobe starts transmitting earlier relative to DQ. A connection between this switch and MR40 has not been confirmed.

Practical choice. **AUTO**. Compare ENABLED/DISABLED separately for a specific training problem.

Key detail. According to the DRAM documentation, changing MR40 leaves data transmission timing and Read Latency unchanged.

> Z890: E25061 lists DIMM DFE Training separately; the other four settings in this block are not listed. Duty Cycle Correction for LP5 DCA is intended for LPDDR5. There is no confirmation that it can replace DRAM DCA when tuning DDR5.

6.11 DRAM checks and repair

Margin is the distance from the operating point to the error boundary in timing or Vref. These settings control measurements, training and addressing checks, retraining, and DRAM repair. Validate the profile under load separately.

Rank Margin Tool Per Bit — RMTBIT

What it does. Measures timing and receiver-threshold margins for individual DQ bits. In the older MRC, a separate flag starts it without checking the RMT flag; the dependency in current ASUS BIOS implementations has not been disclosed.

Practical choice. **AUTO** or DISABLED if the results are not used; ENABLED for diagnostics when the data is accessible.

Rank Margin Tool — RMT

What it does. Evaluates timing and Vref margins for reads, writes, and commands. Allows comparison of trained states.

Practical choice. **AUTO** or DISABLED for normal operation; ENABLED if you have a way to read the results. BDAT export is enabled separately. The report may still be unavailable in the BIOS interface.

Memory Test — MEMTST

What it does. Tests memory during initialization; ASUS has not disclosed the coverage or patterns.

Practical choice. **AUTO**; ENABLED for boot diagnostics. No separate entry is listed in E25061 for Z890.

DIMM SPD Alias Test — ALIASCHK

What it does. Intended to detect DRAM address aliasing when the module organization is described incorrectly. The older code checks geometry and capacity against SPD; the physical address test is unfinished.

Practical choice. **AUTO** or ENABLED. DISABLED makes sense only for a confirmed false positive.

Post Package Repair Training — PPR

What it does. Allows defective DRAM rows to be replaced with spare rows: Soft PPR is a temporary repair; Hard PPR is permanent and survives power loss.

Practical choice. Do not force it on for normal overclocking; when controlling it manually, start with **DISABLED**. Do not move to Hard PPR because of errors that occur only when overclocked.

Key detail. The repair type and trigger conditions may be set separately. The repair type used by ASUS has not been established; the Z890 menu name omits Training.

Retrain Margin Check — RMC

What it does. In the older MRC, checks read, write, and command margins; if margin is insufficient, raises the optimization thresholds and requests retraining during the current initialization. Execution also depends on the power training mode.

Practical choice. **AUTO**. ENABLED for investigating inconsistent training results; DISABLED if the check itself causes a problem.

Margin Check Limit

What it does. Selects the margin check used to decide whether to retrain on the next boot: DISABLED, L1, L2, BOTH.

Practical choice. **DEFAULT VALUE**. For diagnostics, start with L1; test L2 and BOTH with the L2 threshold scaling factor in mind.

Margin Limit Check L2

What it does. Sets the threshold: L2 = L1 × value / 100. Available when L2 or BOTH is selected.

Practical choice. **DEFAULT VALUE**; use 100 for comparison.

Key detail. A higher value sets a stricter check threshold. A range of 1–300 is specified for Z790; the Z890 manual does not give the limits.

6.12 Additional Z890 Apex algorithms

The Z890 menu adds training stages and separate controls for some existing functions. This section covers the differences from Z790 documented in the ASUS Apex manuals. Start with AUTO; the procedure for comparing settings is in §6.2.

CA ODT Optimization

What it does. Separate optimization of command/address line termination. DIMM CA ODT Training is also retained in the menu; ASUS does not describe how the tasks are divided between these two stages.

Practical choice. **AUTO**. When tuning manually, change these two settings separately.

Unmatched Write Time Centering 1D — UNMATCHEDWRTC1D

What it does. A separate one-dimensional write alignment stage for the Unmatched path. The public Intel interface does not disclose how it differs from regular Write Timing Centering 1D.

Practical choice. **AUTO**.

RxVref Per-Bit Training — RXVREFPERBIT

What it does. Tunes the input detection threshold separately for each data bit on the CPU receiver side.

Practical choice. **AUTO**.

DDR5 ODT Timing Config — DDR5ODTTIMING

What it does. A separate stage for tuning DDR5 ODT timing: when termination turns on and off relative to data transfers.

Practical choice. **AUTO**. Compare ENABLED and DISABLED separately for a reproducible problem during full training.

Read CTLE Training — RDCTLET

What it does. Tunes the CPU receiver linear equalizer. CTLE adjusts the frequency response of the input path, reducing signal distortion during reads.

Practical choice. **AUTO**.

Ddr5 Rx Cross-Talk Cancellation — DDR5XTALK

What it does. Controls crosstalk compensation in the DDR5 receive path: adjacent lines can induce interference in the received signal.

Practical choice. **AUTO**.

Unmatched Rx Calibration — RXUNMATCHEDCAL

What it does. Calibrates the Unmatched receive path. Its architecture and adjustable quantities have not been disclosed in the ASUS manuals or the public FSP interface.

Practical choice. **AUTO**.

DQ/DQS Swizzle Training — DQDQSSWZ

What it does. Configures the mapping of logical DQ/DQS lines to their physical routing, accounting for line swaps.

Practical choice. **AUTO**.

Write DQ/DQS Retrain — WRTRETRAIN

What it does. Controls a separate stage that retunes the relative alignment of DQ and DQS during writes. The older MRC describes such a mechanism for LPDDR; its DDR5 implementation on Z890 has not been disclosed.

Practical choice. **AUTO**.

These stages calibrate internal memory-PHY circuitry: compensation, phase interpolators, receivers, and linear voltage regulators.

Pre Training Comp Calibration — DDRPRECOMP

What it does. Performs preliminary compensation calibration before the main training stages. Z890 separates it from the subsequent Comp Optimization stage.

Practical choice. **AUTO**.

Ref PI Calibration — REFPI

What it does. Calibrates the phase interpolator reference circuitry. PI positions the edge where required between the available clock phases.

Practical choice. **AUTO**.

Data PI Linearity Calibration — DATAPILIN

What it does. Calibrates the linearity of the data-path phase interpolators: equal control-code steps should produce uniform phase shifts.

Practical choice. **AUTO**.

Rx SAL Calibration — RXSALCAL

What it does. A separate receiver calibration. The purpose of the SAL circuitry and the adjustable quantities are not described in the ASUS manuals or public FSP.

Practical choice. **AUTO**.

VccClk FF Offset Correction — VCCCLKFF

What it does. Corrects the offset of the internal VccClk FF circuitry. What FF stands for and its relationship to a specific BIOS voltage field have not been established from the sources reviewed.

Practical choice. **AUTO**.

LVR Auto Trim — LVRAUTOTRIM

What it does. Automatically trims the internal PHY linear voltage regulators. In the Meteor Lake/Arrow Lake architecture, LVRs supply internal CPU memory-interface circuitry.

Practical choice. **AUTO**.

View Pin Calibration — VIEWPINCAL

What it does. An internal calibration for View Pin. Public manuals do not explain the purpose of this circuitry or its relationship to DDR5 tuning.

Practical choice. **AUTO**.

Power Saving Meter Update — PWRMETER

What it does. Updates an internal estimate of energy savings. In the older MRC, the calculation compares the states before and after optimization and passes the result to the power controller.

Practical choice. **AUTO**.

On Z890, DCC is split by circuit and signal. Separate settings handle read and write training across different ranks and protection against Rowhammer.

Duty Cycle Correction Downstream Training — DCCDOWNSTREAM

What it does. Corrects duty cycle in downstream clock-path circuitry. Intel specifies the PI Serializer/LUT area—the phase interpolator serializer and its settings table.

Practical choice. **AUTO**.

Duty Cycle Correction QCLK Calibration — DCCQCLK

What it does. Calibrates the duty cycle of the internal QCLK signal.

Practical choice. **AUTO**.

Duty Cycle Correction Rise/Fall Training — DCCRISEFALL

What it does. Performs separate rising- and falling-edge correction, equalizing the signal high and low durations.

Practical choice. **AUTO**.

Functional Duty Cycle Correction for DDR5 DQS — FUNCDCCDQS

What it does. Performs functional duty cycle correction for the DDR5 DQS strobe. A connection to the earlier Tx Dqs Dcc Training has not been confirmed.

Practical choice. **AUTO**.

Functional Duty Cycle Correction for DDR5 CLK — FUNCDCCCLK

What it does. Performs functional duty cycle correction for the DDR5 CLK signal.

Practical choice. **AUTO**.

Functional Duty Cycle Correction for Data DQ — FUNCDCCDQ

What it does. Performs functional duty cycle correction for the DQ data lines.

Practical choice. **AUTO**.

Write Rank-to-Rank Training — TXRK2RK

What it does. Separate write training for operation across different ranks. The delays it tunes are not listed in public FSP; Turn Around Timing Training is retained as a separate setting.

Practical choice. **AUTO**.

Read Rank-to-Rank Training — RXRK2RK

What it does. Separate read training for operation across different ranks. The delays it tunes are not listed in public FSP.

Practical choice. **AUTO**. Do not carry over the Z790 RTL recommendations to this setting: a connection between the stages has not been confirmed.

Row Hammering Prevention — ROWHAMMER

What it does. Controls protection against errors in adjacent DRAM rows caused by repeatedly activating the same rows. This is a separate entry in the Z890 training menu; the protection itself also existed on earlier platforms.

Practical choice. **AUTO**. I do not recommend disabling it for overclocking: it affects data protection. The specific mechanism selected by ASUS has not been disclosed.

> **FOR EVERYDAY MEMORY TUNING**
>
> The purpose of this chapter is to explain how the TRAINING ALGORITHMS controls work. For the average user, the practical rule is simple: leave 98% of these settings on **AUTO**. Changing them makes sense when you have a specific training problem and understand what you are testing.

Chapter sources

1. ASUS Z790 2023
2. ASUS Z890
3. FSP Raptor Lake-S
4. FSP ARL-S IoT
5. MRC: Commands
6. MRC: Drivers
7. MRC: Receivers
8. MRC: Read training
9. CFL: LPDDR Only
10. Micron DDR5
11. MRC: Write training
12. MRC: Common
13. MRC: Receive Enable
14. MRC: WL
15. MRC: Startup
16. ASUS Z790 2022

07 / Stability testing

7.1 Stability testing principles

Use different workloads to check a DDR5 profile. Data storage and transfer, the memory controller, heavy computational workloads, training repeatability, and margin at real operating temperatures must be tested separately.

FIVE DIFFERENT TEST TARGETS

Target	What may be unstable	How we test it	What a single test does not prove
DRAM and data	Cells, rows, refresh, writes, and reads	Karhu, TM5, MemTest86, OCCT Memory	IMC stability under AVX load
IMC / PHY	CPU-to-DIMM link, VDD2/MC, TX, SA, Vref, and signal integrity	y-cruncher VT3/FFTv4, OCCT CPU + RAM	Absence of a rare retention error
CPU and cache	Cores, ring/cache, voltage, and CPU temperature	y-cruncher SVT and small in-cache tests	Stability of the modules alone
Training	Variation in trained values, boots after idle, reboots, and the saved fast path	Several complete training cycles and boots	Stability of an already-booted system
Temperature	tREFI, tRFC, DRAM voltage, and different thermal behavior of 1R/2R	Karhu/TM5 with HWiNFO and real airflow	Behavior of a cold memory kit

ANY CONFIRMED ERROR MEANS INSTABILITY

There is no acceptable number of errors. However, where an error appears does not by itself identify the culprit: Karhu can catch a CPU/cache issue, y-cruncher can catch memory or IMC instability, and MemTest86 can catch a firmware-dependent error. First reproduce the symptom, then change one parameter.

PROFILE TESTING SEQUENCE

Step	Stage	Practical action	Proceed when
1	Quick screening	10–30 minutes of a targeted workload after one change	No errors or hangs
2	Isolate the cause	Compare SVT with VT3/FFTv4 and an independent RAM test	The conditions that reproduce the failure are understood
3	Pre-boot	MemTest86: four passes after cold training	No address or bit errors
4	Thermal conditions	Bring the DIMMs to their daily-use temperature plateau	The profile remains stable at the selected tREFI
5	Repeatability	Boot after idle, reboot, sleep, and normal workloads	The result does not depend on one lucky POST

THE CORE PRINCIPLE OF THIS CHAPTER

A combination of two or three different algorithms provides more information than running one test all day. For a final profile, we use y-cruncher, Karhu, MemTest86, and RAM Test Pro by Svetlana; for testing quality, I would even rank it first. Boot checks remain mandatory; I treat TM5 as an alternative targeted tool.

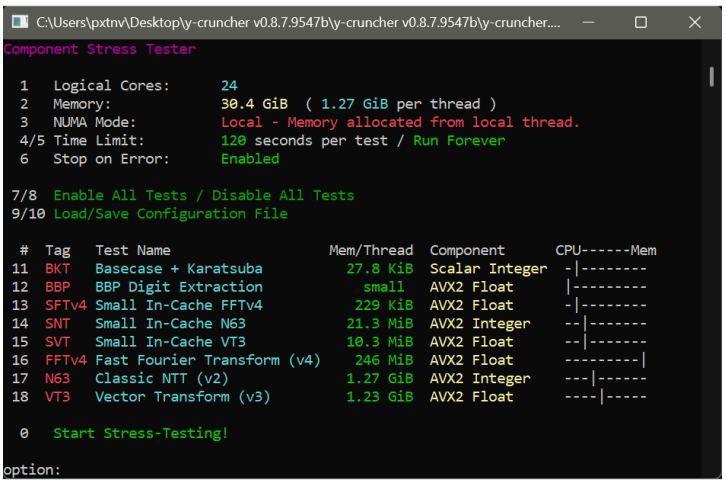
Test duration

Running one test on the principle that “longer is better” is a foolish waste of time. A profile needs a mix of checks: memory, the controller, heat, retraining, and boots. Even relatively short checks in combination can reveal more than blindly looping one algorithm. Every test needs a purpose. Without one, you are just wasting your time running hours of tests for the sake of testing. Ignore that advice — the people giving it have a very superficial understanding of the hardware.

DOCUMENTATION REVIEWED: The methodology of this revision; Numberworld y-cruncher FAQ; Karhu RAM Test FAQ; PassMark MemTest86 User Guide; official OCCT test descriptions.

7.2 y-cruncher

Use only Component Stress Tester. The official Windows build is v0.8.7.9547b; Linux is v0.8.7.9547. My screenshot shows the Windows binary 0.8.7.9547b.



PRACTICAL STARTING POINT

Memory: for large tests, 80–90% of free RAM with room for the OS, without paging. NUMA: Local on a typical LGA1700/LGA1851 system. Time Limit: a separate 60–120 s limit for each component in the session. Stop on Error: Enabled.

The instruction set depends on the binary. AVX2 in the screenshot describes that run. Record the version, binary, threads, and memory allocation when comparing results. Mem/Thread shows memory use per thread, which varies by component.

WHAT EACH COMPONENT DOES

Tag	Algorithm	Primary workload	Role in DDR5 diagnostics
BKT	Basecase + Karatsuba*	Scalar integer multiplication; small working set	CPU arithmetic; little dependence on RAM
BBP	BBP Digit Extraction	Vector floating-point arithmetic; small working set	CPU computation with a small working set; RAM coverage is limited to the size of that set.
SFTv4	Small In-Cache FFTv4	Small FFTv4: floating-point Fourier transform in cache	CPU/cache; complements large FFTv4
SNT	Small In-Cache N63	Small N63: integer NTT in cache	CPU/cache with a different type of arithmetic
SVT	Small In-Cache VT3	Small VT3: vector computation with an in-cache working set	CPU/cache; I compare it with large VT3
FFTv4	Fast Fourier Transform v4	Floating-point FFT; large working set, strongly dependent on RAM bandwidth	CPU/cache/IMC/RAM with heavy memory traffic
N63	Classic 64-bit NTT v2	64-bit integer NTT; large working set	Another algorithm for combined CPU and RAM testing
VT3	Vector-Scalable Transform v3	Vector transform; large working set, CPU + IMC + RAM	Mixed workload across the DDR5 path; successor to VST

* Command Lines.txt expands BKT to include Toom-Cook; the developer's internals guide says Toom-3 was removed.

HOW I COMPARE THE RESULTS

SVT is the small, in-cache variant of VT3; VT3 succeeds the old VST. If SVT passes but VT3 fails, I check the profile with a large working set: CPU/cache, IMC, and RAM. If both fail, I start with the same components. I revert the last change, repeat the check, and add an independent RAM test. FFTv4 exercises the CPU and memory together.

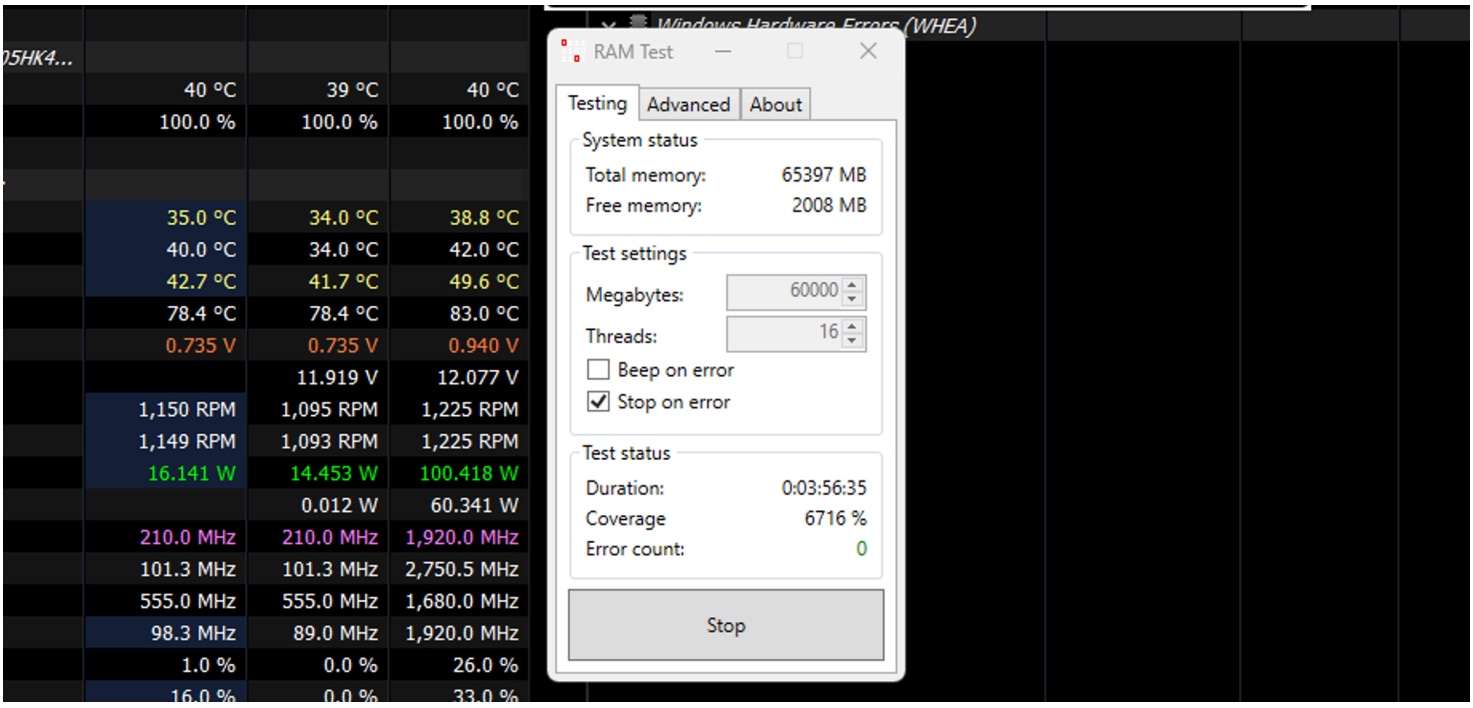
TYPICAL PRACTICAL DURATION

Quick SVT + VT3 screening: 20–30 minutes. Final candidate: 45–60 minutes; up to 60–90 minutes when needed to reach the temperature plateau. These are guidelines from my methodology. After reaching the temperature plateau, I check the profile with other algorithms and repeat boot checks.

DOCUMENTATION REVIEWED: Alexander J. Yee: y-cruncher v0.8.7, Version History, Multiplication Internals, Memory Allocation Guide, and FAQ; official package 0.8.7.9547b.

7.3 Karhu RAM Test

Assess RAM Test's suitability for DDR5 from test results. Claims about its limitations need specific instability scenarios that Karhu misses and comparative tests that demonstrate them. RAM Test was developed and is published by the Finnish company Karhu Software Oy; the stable version is 1.1.0.0, **while the 2.0 branch is in development**.



HOW LONG TO TEST: CURRENT DEVELOPER STATISTICS

Time to error	Errors found	How to use it
10 minutes	74.89%	Quickly exposes a badly chosen setting
30 minutes	87.62%	Intermediate check after a timing or voltage change
1 hour	92.97%	Minimum for finding some intermittent errors
3 hours	97.84%	Reasonable test for a finished candidate
6 hours	99.30%	Strong final run; returns diminish sharply after this
12 / 24 hours	99.91 / 99.99%	Occasional search for an intermittent failure

10,000% IS A USEFUL REFERENCE, BUT NO LONGER THE DEVELOPER'S CURRENT RECOMMENDATION

The current FAQ advises looking primarily at duration. Coverage measures the accumulated work performed by the test relative to the allocated memory region. It does not provide the percentage of physical cells tested or a probability of stability. Its rate of increase depends on memory size, CPU, thread count, and cache.

SETTINGS AND THERMAL CONDITIONS

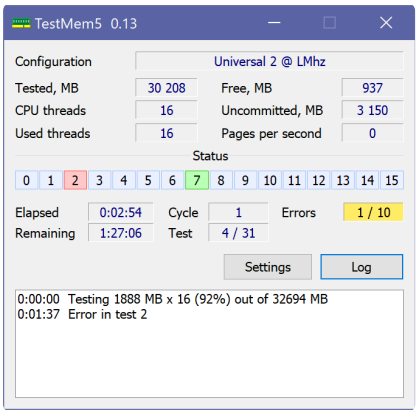
Field	Practical value	Why
Megabytes	About 85% of physical RAM; leave roughly 15% for the system	Do not select all memory: Windows and background processes need some headroom, without paging
Threads	Number of physical cores; 24 for the 14900K/KS	As recommended by the Karhu README
CPU cache / RNG	Default / Default	Set CPU cache to Enabled only for a combined CPU/cache test; XORWOW is primarily needed for Windows 7
Stop on error	Enable	The first error means the profile has failed the check

AIRFLOW AND MEMORY OPERATING TEMPERATURE

With elevated VDD/VDDQ and tREFI above roughly 30,000, I use directed airflow even during tuning and monitor the SPD Hub temperature in HWiNFO. The profile must then be tested with its daily-use cooling. On my TeamGroup Xtreem kit at tREFI 131K, errors begin at about 47 °C; another kit may have a different limit, and 2R is generally more sensitive.

DOCUMENTATION REVIEWED: Karhu Software Oy RAM Test 1.1.0.0: official page, README, current FAQ, and archived 2021 FAQ; HWiNFO monitoring. Screenshot: my test run.

7.4 TestMem5 (TM5)



MY POSITION

I do not use TM5 myself: in my methodology, it did not provide any additional diagnostic information beyond what I already got from Karhu and y-cruncher. TM5 remains a popular free tool. In the screenshot, Universal 2 has already detected an error.

The original TestMem5 0.12 was written by Serj; CoolCmd continued its development. The current version, 0.13.1, fixes premature completion, an incorrect tested-memory size, and silent allocation errors. Run it as administrator and verify the TM5.exe/TM5.dll version.

THE CONFIG DETERMINES THE NATURE OF THE TEST

Config	Creator	Purpose	Role for Intel DDR5
DDR5 Intel / OptimalforIntelDDR5	anta777	Profile specifically for Intel DDR5	The most logical starting point
Universal 2	LMHz	General-purpose profile; default in 0.13.1	Quick general check
Absolut	anta777	Profile focused on testing the memory array	Final independent check
Extreme	anta777	Older, long-running general-purpose profile	Usable, but not DDR5-specific
1usmus v3	1usmus	Short diagnostic profile	Historical; do not treat it as the DDR5 standard
Default	Serj	Original baseline sequence	Not the best choice for modern overclocking

KARHU AND TM5 APPROACH A SIMILAR TASK DIFFERENTLY

Characteristic	Karhu RAM Test	TestMem5 0.13.1
Model	Single closed algorithm	Engine with user-defined configs
Progress	Time and coverage	Specified duration, sequences, and tests
Configuration	Cache, RNG, FPU, memory size, and threads	Patterns, blocks, duration, and order
Repeatability	Easier to compare identical runs	The result depends more heavily on the config
License	Paid	Free

HOW TO USE AN ERROR NUMBER IN DIAGNOSIS

Tables that map ‘error N’ to a specific timing are based on community observations and depend on the config. Use them only as weak hints. For A/B comparisons, 10–30 minutes is enough; you can test a candidate profile for 1–2 hours with DDR5 Intel or Universal 2, then confirm it with another algorithm.

DO NOT USE RANDOM REPACKS

The official 0.13.1 binaries are unsigned and may trigger antivirus heuristics. Do not use archives with unknown TM5.dll, MT0.dll, or EXE files: the required popular configurations are already included in CoolCmd’s release.

DOCUMENTATION REVIEWED: CoolCmd/TestMem5 v0.13.1 release and documentation; bundled configs by Serj, LMHz, anta777 and 1usmus; 02.09.2026.

7.5 MemTest86

PassMark MemTest86 v11.7 Build 1000 is a standalone UEFI application. Write the image to a USB drive, select the drive in the Boot Menu, and MemTest86 then runs without Windows or Linux. It is used for basic and service diagnostics of memory kits in UEFI mode.



CONFIGURATION FOR DDR5

Setting	Practical choice	Meaning
CPU Mode	Parallel	Fastest standard mode; Single/Round Robin/Sequential are only for diagnosing UEFI or CPU cores
Passes	4 passes	Free: maximum of 4; the first is shortened, the next 3 are full. Four full passes are available only in Pro/Site through PASS1FULL=1
Tests	Free: 0–10, 13; Pro/Site: 0–13	Tests 11/12 are 64/128-bit tests available only in Pro/Site; Test 13 Row Hammer is available in Free
Test 14 DMA	Disabled by default	Additional DMA/USB diagnostics. Other tests are used for routine memory-overclocking validation.

FOUR PASSES BEFORE BOOTING THE OS

In PassMark's official example, one pass takes about 15 minutes and four take 120 minutes. Estimate the time separately for your system: RAM capacity, CPU, selected tests, and cache mode can change it substantially. In Free, four passes consist of one shortened pass and three full passes. PASS1FULL=1 makes the first pass full, but it is available through mt86.cfg only in Pro/Site. Even four error-free passes do not replace Karhu/y-cruncher under an operating system.

FREE, PRO, AND SYSTEM ECC

Feature	Free	Pro
Core tests	Up to 4 passes; up to 16 logical CPUs; without Tests 11/12	Up to 999 passes; more CPUs; Tests 11/12 available
Automation	Manual launch and standard report	mt86.cfg, profiles, advanced reports, and cache policy
System ECC	Detection of system ECC support and error reporting	Error injection to verify system ECC on compatible CPU/IMC combinations

HOW on-die ECC AND SYSTEM ECC WORK

on-die ECC corrects a single-bit error in an internal data block of a DRAM IC. ECS (Error Check and Scrub) counters describe array checks using on-die ECC; reading them requires platform support. System ECC requires compatible CPUs/IMCs, motherboards and memory modules. Corrected ECC errors are errors corrected by system ECC and logged by the platform. An increasing count warrants attention. Error injection in MemTest86 Pro verifies system ECC operation on a supported platform.

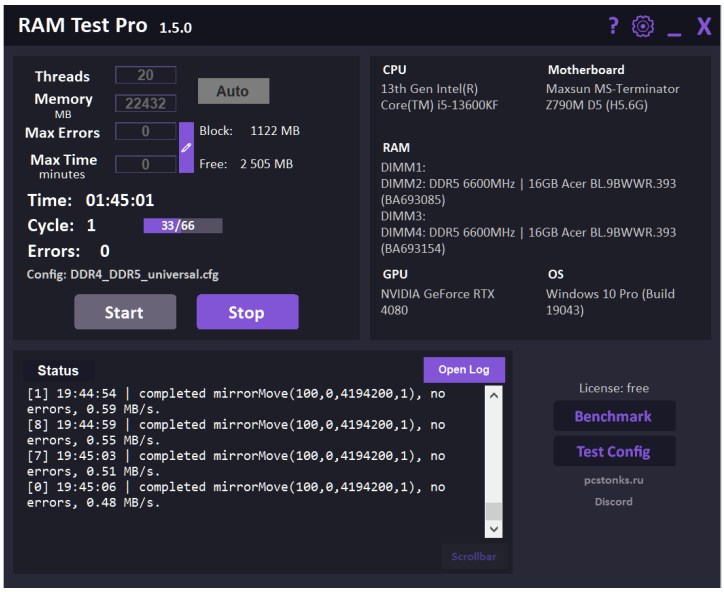
TEST 13 HAMMER AND TEST 14 DMA

Leave Hammer enabled: it searches for row-disturbance bit flips in adjacent rows caused by frequent activations and tests a distinct class of risks associated with refresh (periodic restoration of cell charge). DMA—direct device access to memory without normal CPU handling—is experimental and disabled: its error may involve the USB drive or UEFI driver, so repeat the test with another flash drive.

DOCUMENTATION REVIEWED: PassMark MemTest86 v11.7: User Guide, editions, execution time, ECC, Test 13/14. SK hynix DDR5 32Gb M-die Rev.1.2, §4.37. Photo: my v11 Pro run.

7.6 RAM Test Pro

RAM Test Pro 1.5.0 is a free 64-bit memory-testing utility for Windows 10/11 by **Svetlana (PCSTONKS)**. It combines configurable test sequences, error logging, WHEA monitoring, NUMA/Large Pages support, and a separate DDR2–DDR5 benchmark.



PCSTONKS RECOMMENDATIONS

FROM THE CURRENT RAM TEST PRO GUIDE

- Close unnecessary programs, free as much RAM as possible, and do not use the system during the run.
- Manual mode: at least 800 MB per block; more is better. Leave 300–500 MB of available free memory for the system.
- Test DDR5 for at least 6 hours; DDR4 for 3–4 hours.
- Monitor memory and CPU cooling; use only safe voltages.

MY INTERMEDIATE A/B STAGE

20–30 minutes is a short intermediate run. The final PCSTONKS check is at least 6 hours for DDR5.

WHAT SETS RAM TEST PRO APART

Component	What is implemented	Practical meaning
Engine	Its own x64 core and cfg format, according to Svetlana's description	Flexible configuration of test sequences and parameters
Algorithms	Inverse, mirror move, refresh, pseudorandom, and I/O/AVX	The sequence and parameters can be changed through a config
Diagnostics	Error location, log, WHEA, and stopping at a limit	More context than a single Errors counter
Platforms	Multicore CPUs, NUMA, and experimental Large Pages	Useful beyond a typical gaming system
Benchmark	Read/Write/Copy, latency, and random access	Complements AIDA64/MLC when assessing memory performance.

ADDITIONALLY:

Confirm RAM Test Pro results with y-cruncher, MemTest86 or another independent workload. Repeat the checks after booting following an idle period and after rebooting.

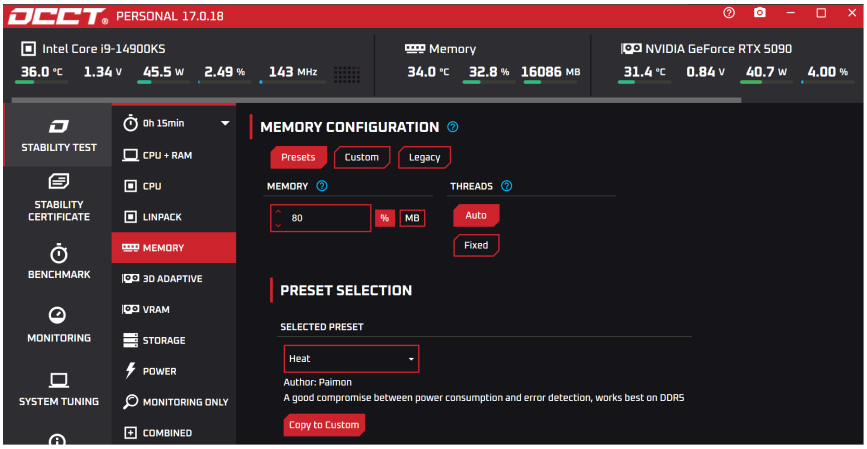
DOCUMENTATION REVIEWED: Svetlana / PCSTONKS: RAM Test Pro 1.5.0 official page, guide and release notes.

7.7 Additional tests

These programs can be used to quickly test a specific hypothesis and obtain additional diagnostic data. Karhu + y-cruncher remain the foundation of my methodology; Svetlana's (PCSTONKS) RAM Test Pro is covered in 7.6 as a free alternative for an additional check. Always save the version, settings, duration, temperature, and first error together with the screenshot.

Additional tools and test modes





Tool	When useful	Limitation	Practical duration
OCCT Memory	Tests memory in Windows and detects errors at the selected frequency and timings	Cannot test memory occupied by the operating system	15–30 minutes
OCCT CPU + RAM	Tests the overall CPU and memory path; monitors WHEA	More difficult to isolate the cause	20–45 minutes
HCI MemTest 7.0	Simple alternative Windows RAM test	More manual setup; slower than Karhu. Pro makes thread allocation easier	400%+ as a basic reference point
Real-world workload	Game, archiver, compilation, rendering, and system sleep	Does not provide controlled coverage	Normal work cycle

7.8 Test plan

Stage	Primary combination	What we test	Guideline
One timing	Karhu	Quick feedback on the latest change	10–30 minutes
Frequency / power	y-cruncher SVT + VT3, then FFTv4	CPU/cache and the CPU/IMC/RAM path with different working-set sizes	20–30 minutes
Candidate profile	y-cruncher + Karhu; TM5/RTP are additional checks	Different algorithms under Windows	45–60 minutes + 1–3 hours of Karhu
Pre-boot	MemTest86 4 passes	Gross address, bit, and Hammer errors	Until completion
Final daily profile	MemTest86 + y-cruncher + Karhu + boots after idle and reboots	Data, IMC, temperature, and repeatability	4 passes + 45–60 min + 3–6 hr of Karhu

CHOOSE TEST DURATION TO SUIT THE TASK

The smaller the change, the shorter the intermediate test. A long final run begins only after the profile has survived several short A/B checks. If an error appears within a minute, there is no reason to wait out the remaining hours; if it appears only after warm-up, first establish the temperature threshold.

RECOMMENDED FOUNDATION OF THIS MANUAL

The foundation of my methodology is Karhu + y-cruncher; MemTest86 adds an independent UEFI check. The 1–3 and 3–6 hour ranges apply specifically to Karhu and were not borrowed from PCSTONKS. TM5 or RTP can serve as additional independent checks. Even after an error-free run, the baseline Karhu criterion must still be met. Use OCCT and HCI only for a specific diagnostic task.

DOCUMENTATION REVIEWED: OCCT official test descriptions; HCI MemTest 7.0 official page; PCSTONKS RAM Test Pro documentation; consolidated methodology of this manual.

7.9 Error diagnosis

After an error, first establish the conditions under which it appears. Examine the test, time, temperature, WHEA, boot or reboot type, and latest change; then revert only one parameter.

SYMPTOM -> FIRST HYPOTHESIS -> NEXT TEST

Symptom	First hypothesis	What to do next
The data-error counter rises immediately	Latest OC change; CPU/cache, memory, IMC, or signal integrity	Revert the step; repeat from a known-good baseline; save the error text and conditions
The test cannot allocate memory	Requested allocation, program limitations, or available RAM	Reduce the allocation; check program settings and messages
The test runs unusually slowly	Paging (page transfers between RAM and disk), background load, or test mode	Check RAM/page-file use and repeat under comparable conditions
Error only after warm-up	tREFI/tRFC, DRAM VDD, cooling, or 2R	Record the SPD Hub temperature; lower tREFI or improve daily-use airflow
SVT and VT3 fail	CPU/cache, ring, CPU power, or an overall CPU/IMC, thermal, or power limit	Back off the CPU OC; compare SFTv4/SVT and OCCT CPU
SVT passes, but VT3/FFTv4 fail	IMC, VDD2/MC, TX/SA, memory, or signal integrity	Compare with Karhu; restore Auto ODT; check the voltage ranges
MemTest86 reports errors before the operating system loads	Gross memory/IMC instability, addressing, or UEFI/BIOS	JEDEC, another DIMM/slot, then repeat after Clear CMOS and cold training
Error following a boot after idle	Non-repeatable training result or accelerated boot path	Disable MRC Fast Boot; perform three boots after idle and compare runtime readback
WHEA without a RAM error	Possible sources include the CPU, IMC, interconnects, and DRAM; use the WHEA record to narrow them down.	OCCT CPU + RAM and a separate CPU test; check the WHEA log

Data errors and memory-allocation errors are counted separately. Paging (transferring memory pages between RAM and disk) can dramatically slow the test; it is not a sufficient explanation for a rising RAM-error counter.

> **DO NOT TREAT AN ERROR BY RANDOMLY RAISING VOLTAGE**
>
> SA, TX, MC/VDD2, and DRAM VDD/VDDQ each have useful ranges: excess voltage can degrade the signal and training and increase heat. Return to the last verified value and adjust the voltage of one power rail in small steps, checking values above and below that value.

COMPLETION CRITERIA FOR A DAILY PROFILE

Step	Requirement	What to save
1	Four error-free MemTest86 passes	HTML/photo of the report and the 11.x version
2	45–60 minutes of y-cruncher SVT + VT3 + FFTv4	Version, memory allocation, limit, and initial/final temperature
3	Karhu for 3–6 hours; TM5/RTP only as an additional run	Duration, coverage, memory size, threads, and 0 errors
4	Three boots after idle and three reboots; sleep if used	POST behavior, Q-Code, and trained values
5	Final thermal run with daily-use cooling	Maximum SPD Hub temperature, WHEA events, and ambient temperature
6	Normal workloads show no regressions	Archiver/game/rendering and a backup of the profile

STOPPING POINT

The profile is ready when it passes different algorithms, remains reproducible after complete power removal, and retains margin at daily-use temperatures.

DOCUMENTATION REVIEWED: Consolidated methodology of chapters 03-07; official y-cruncher, Karhu RAM Test, PassMark MemTest86, OCCT and HWiNFO documentation.

08 / Performance and monitoring

8.1 Performance metrics

For DDR5, evaluate bandwidth, latency, cache effects and performance in real workloads. Check stability using the method in Chapter 7.

A comparison is meaningful only within the same program and version, with identical CPU/Ring frequencies, Windows background load, cooling, and operating-system security-feature state.

FOUR DIFFERENT TYPES OF RESULTS

Metric	What it shows	What affects it most
Read	Speed of reading data from memory	Frequency, IMC, Gear, channels, threads, and test implementation
Write	Speed of writing data to memory	CPU/IMC architecture, frequency, timings, and algorithm
Copy	Data copy: reading followed by writing	Entire memory path, cache, and working-set size
Latency	End-to-end access latency in nanoseconds	All timings, frequency, Gear, Ring/Uncore, and OS background activity

THREE LEVELS OF RESULT VALIDATION

1 SYNTHETIC

AIDA64, MLC, or OCCT shows the limit of a particular algorithm.

2 REAL-WORLD TEST

7-Zip, Cinebench, or a CPU-limited game checks whether the gain reaches the actual workload.

3 STABILITY

Chapter 07 searches for errors separately. A high score does not mean the profile is stable.

CHECK THE GAIN IN YOUR OWN WORKLOADS

Higher bandwidth does not guarantee better 1% lows, and lower AIDA64 latency will not ensure lower latency in a game. First evaluate the median across runs, then confirm the effect with a separate real-world workload.

RULE FOR THIS CHAPTER

Change one profile, keep the environment identical, and do not cherry-pick the best run. Do not count a difference smaller than the natural run-to-run variation as an improvement.

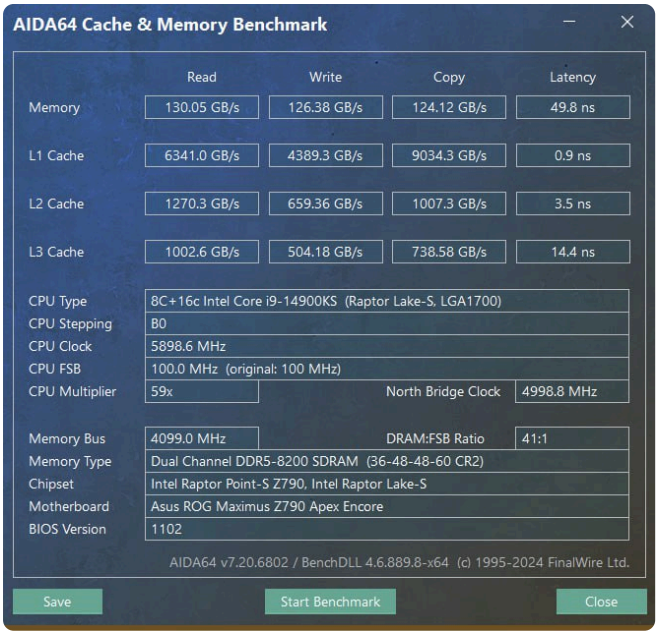
DOCUMENTATION REVIEWED: FinalWire AIDA64 benchmark methodology; consolidated measurement methodology of chapters 03-07.

8.2 AIDA64 Extreme



AIDA64 Cache & Memory Benchmark is a quick synthetic test for comparing profiles on the same system. According to the developer's published description, Read/Write use a 64 MB block, while Copy transfers 32 MB and counts traffic in both directions. Latency uses random addresses within blocks.

HOW CACHE & MEMORY BENCHMARK WORKS



READ / WRITE

Multithreaded reads and writes. Higher is better.

COPY

Read + write through the CPU. Shows the entire path well.

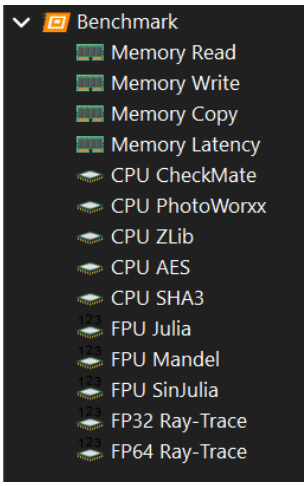
LATENCY

Random-access latency in ns. Lower is better; the result reflects the entire memory path, including tCL.

MY REFERENCE 8200 BENCHMARK

130.05 / 126.38 / 124.12 GB/s and 49.8 ns on a 14900KS.

USEFUL TESTS FROM THE GENERAL BENCHMARK SECTION



CORE SET

Memory Read, Write, Copy, and Latency directly compare the DDR5 profile.

CPU + MEMORY

CPU PhotoWorxx is especially sensitive to cache and latency; CPU ZLib has moderate memory sensitivity.

PRIMARILY CPU

AES, SHA3, Julia, Mandel, SinJulia, and Ray-Trace serve as CPU-performance checks in this method.

Hardware Prefetcher on ASUS Z790 controls the MLC Streamer: it detects sequential accesses and fetches upcoming data into L2 ahead of demand. It is separate from Adjacent Cache Line Prefetch; the effect depends on the workload.

> Disabling Hardware Prefetcher in BIOS reduces Read/Write/Copy. I don't remember exactly which one it fucks up, but I think Copy takes the biggest hit.

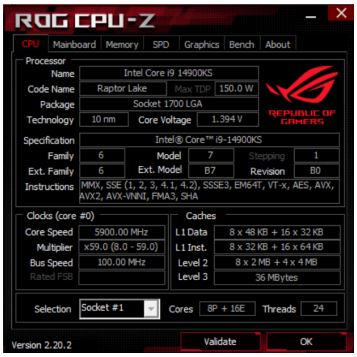
DOCUMENTATION REVIEWED: FinalWire AIDA64 8.40.5000: Cache & Memory, CPU/FPU and developer explanations. Screenshots: my measurements. Hardware Prefetcher: ASUS ROG Z790 BIOS, p. 67; Intel Hardware Prefetch Controls, § 1.3.1.

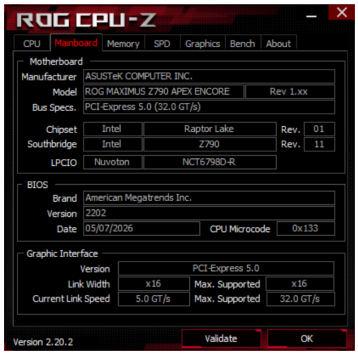
8.3 CPU-Z

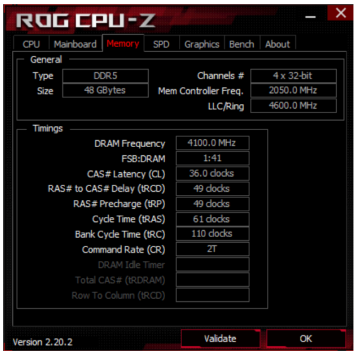
CPU-Z records the system configuration: CPU model and stepping (revision), motherboard model, BIOS version, actual memory clock, active primary timings and each module's SPD contents.

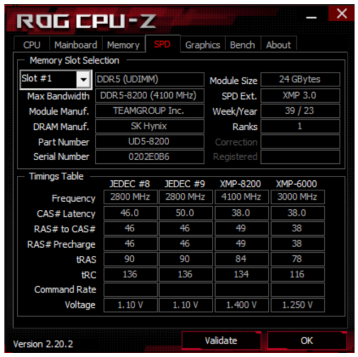
MY CPU-Z TABS: WHAT TO SAVE WITH THE RESULT

1. CPU 2. MAINBOARD 3. MEMORY 4. SPD / SLOT 1

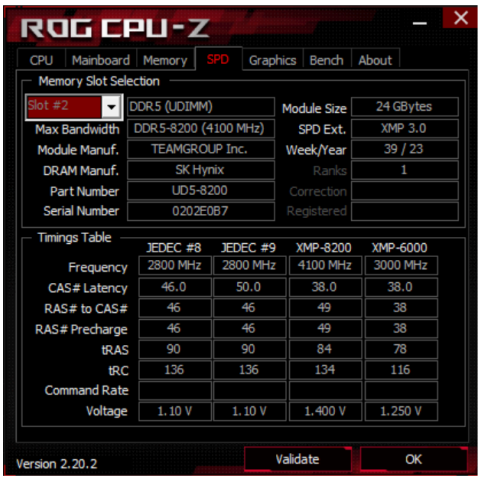


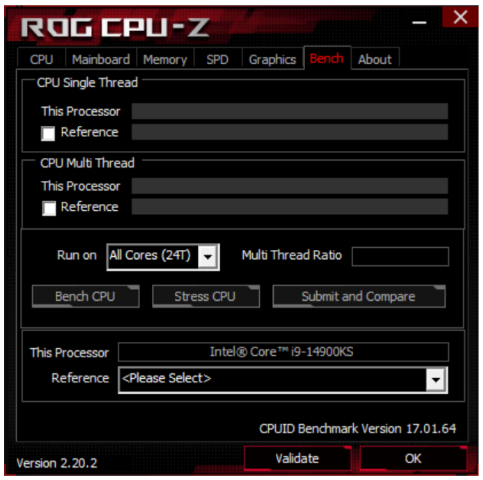


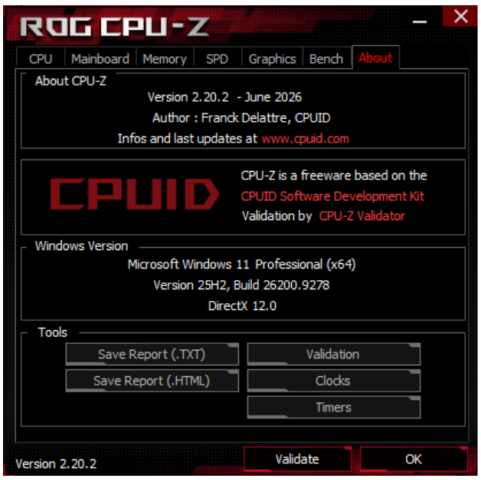




5. SPD / SLOT 2 6. BENCH 7. ABOUT







WHERE TO LOOK FIRST

Tab	What to check	How to read it
CPU / Mainboard	Model, stepping, BCLK, motherboard, BIOS, and microcode	Records the platform and CPU state for repeatability
Memory	DRAM Frequency, 4 x 32-bit, tCL/tRCD/tRP/tRAS/tRC, and CR	4100 MHz × 2 = DDR5-8200; these are the active parameters
SPD for every slot	Capacity, DRAM manufacturer, ranks, part/serial number, JEDEC, and XMP	SPD stores module profiles, but does not prove that XMP is currently active
Bench / About	Quick CPU score and exact CPU-Z version	Bench does not test memory; save the version with the screenshot

MEMORY AND SPD ANSWER DIFFERENT QUESTIONS

Memory shows what the system is running now. SPD shows the JEDEC/XMP profiles and identification data stored on the selected DIMM. CPU-Z Validation records the configuration and frequency, but does not confirm stability.

DOCUMENTATION REVIEWED: Official CPUID CPU-Z 3.01 and Validator V3 documentation. Screenshots: my system.

8.4 HWiNFO



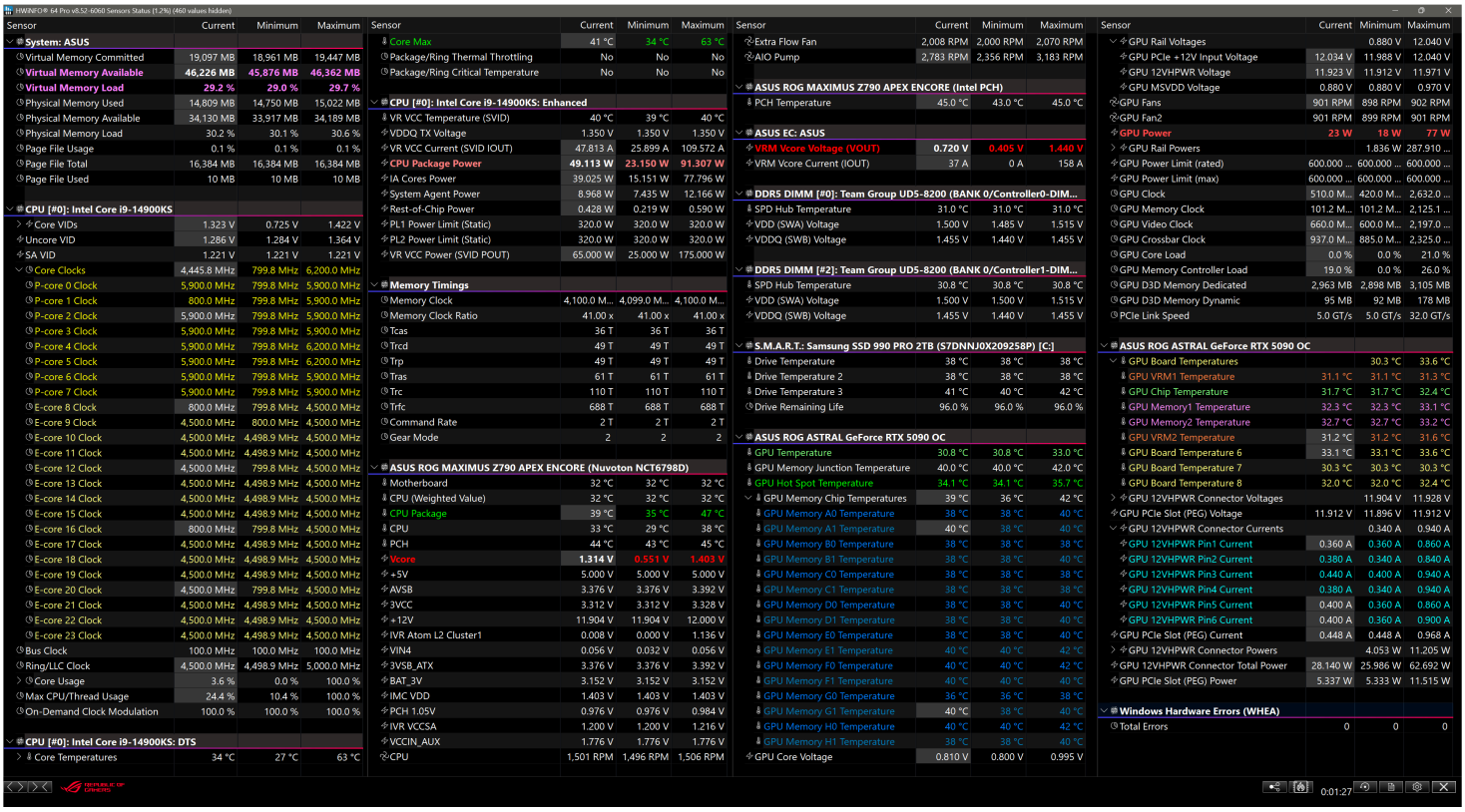
HWiNFO is my primary and, in my view, the best monitoring tool. It simultaneously shows module temperatures, actual* voltages, CPU/Ring frequencies, throttling, and WHEA counters.

* The readings are estimates: PMIC telemetry may be inaccurate. Actual voltage and ripple are checked with an oscilloscope.

MINIMUM SENSOR SET

Reading	What to save	Important nuance
SPD Hub Temperature	Current, Maximum, and Average for each DIMM separately	The sensor measures SPD Hub temperature; determining DRAM die temperature requires a separate measurement.
VDD / VDDQ	Readings from both modules	When supported; recheck anomalies with PMIC and software limitations in mind
Memory Timings	Memory Clock, Gear, and active timings	Quick check that the system loaded the intended profile
CPU / Ring	Frequencies, power limits, and indications of throttling	A different CPU mode changes benchmark results
WHEA	Counter before and after the run	An increase requires diagnosis, but does not automatically implicate RAM

MY WORKING SENSORS SCREEN



DOCUMENTATION REVIEWED: HWiNFO 8.55 beta documentation and developer guidance on SPD Hub Temperature and WHEA. Screenshots: my system.

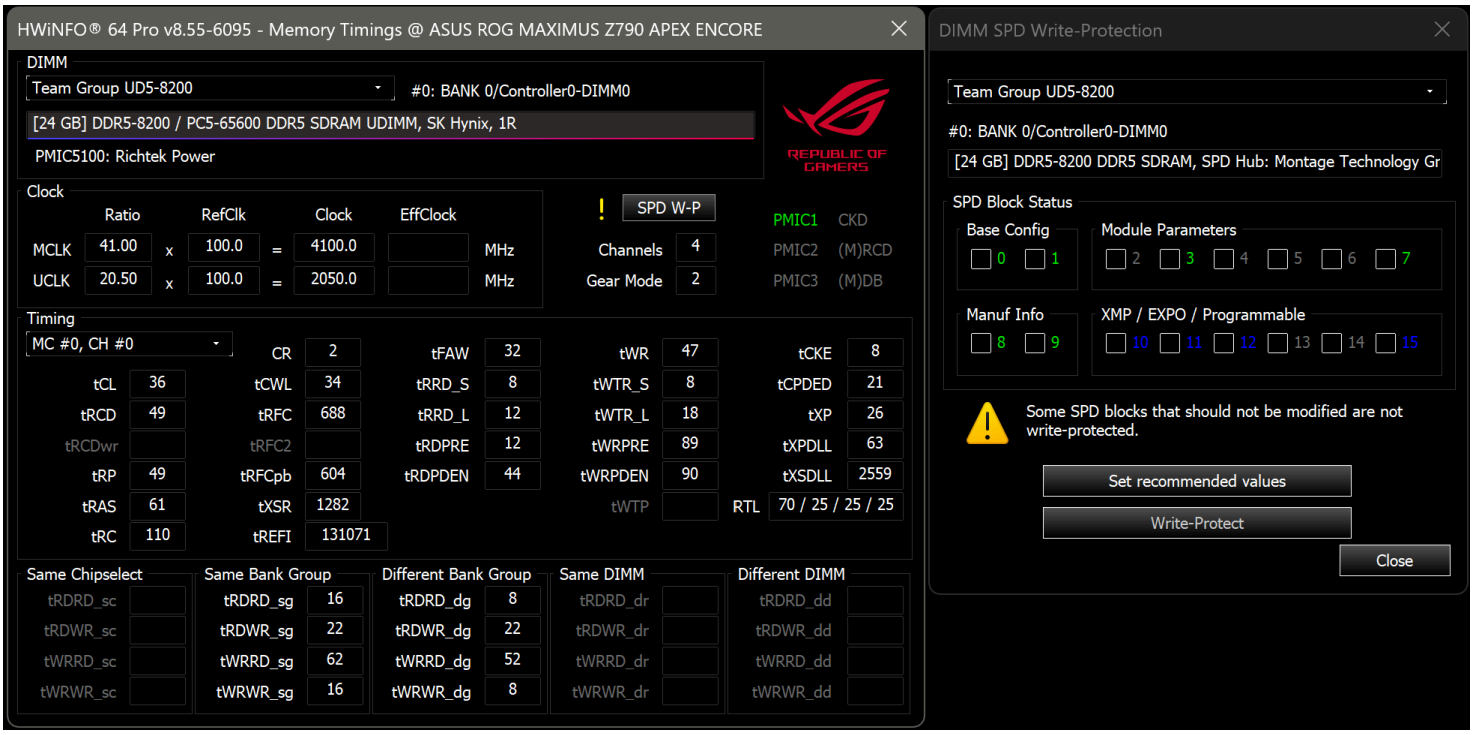
8.4.1 Memory Timings window

In addition to the basic Memory Timings section in Sensors, HWiNFO can open a separate ‘Memory Timings’ window with an expanded set of active memory parameters. This is convenient for checking the values actually applied after memory training, including AUTO settings calculated by the platform.

In Sensors-only mode, the window is available from the context menu of the HWiNFO notification-area icon.

WHAT THE SEPARATE WINDOW ADDS

Additional secondary, tertiary, and turnaround timings: tFAW, tRRD_S/L, tWTR_S/L, tRDPRE, tRDPDEN, tWRPRE, tWRPDEN, tRDRD/tRDWR/tWRRD/tWRWR sg/dg, and others; plus some internal parameters, including RTL. The available fields depend on the platform and HWiNFO version.



HWiNFO: advanced memory timings and SPD write-protection status

WARNING: DIMM SPD WRITE-PROTECTION

“Some SPD blocks that should not be modified are not write protected.”

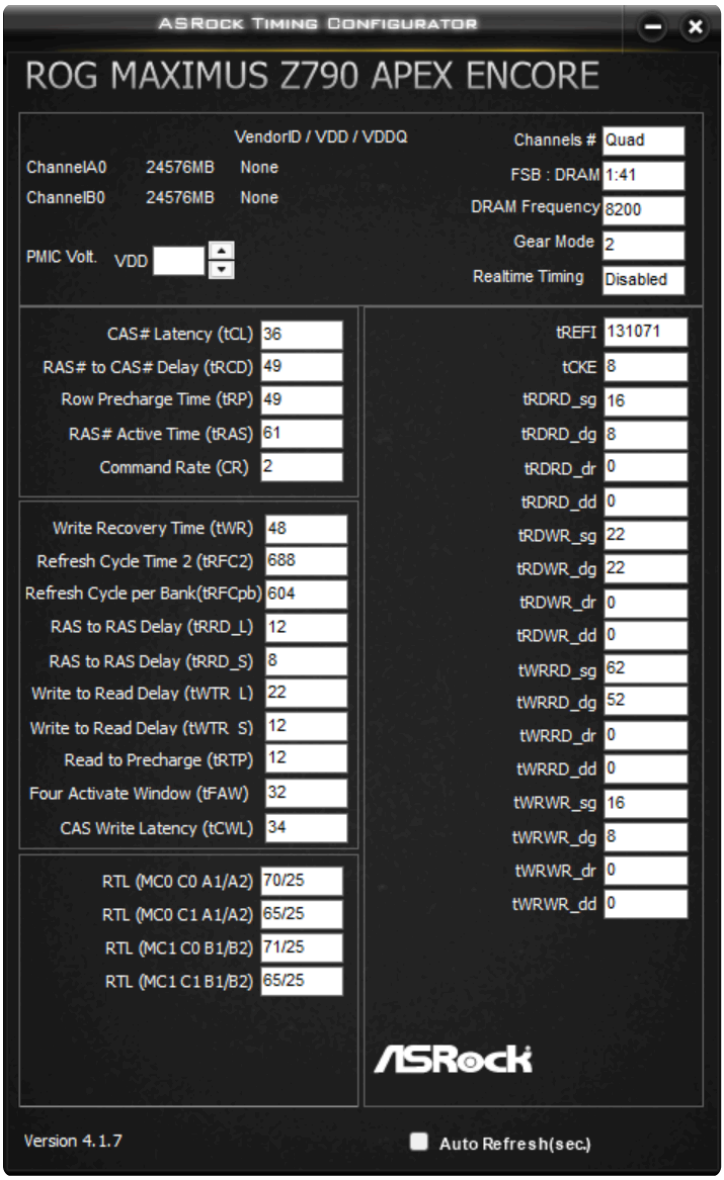
The message describes SPD write protection; it cannot establish the state of the timings. Changing SPD Write-Protection or using SPD write functions without understanding the consequences is not recommended. None of this is required for ordinary timing monitoring.

DOCUMENTATION REVIEWED: HWiNFO: DIMM SPD Write-Protection Management; screenshot version 8.55-6095. HWiNFO — developer explanation of SPD protection

8.5 ASRock Timing Configurator

ASRock Timing Configurator 4.1.7 is a convenient utility for viewing active primary, secondary, and tertiary timings directly in Windows. It provides a compact record of settings, including on compatible ASUS motherboards.

MY DDR5-8200 PROFILE ON Z790 APEX ENCORE



TOP

Motherboard, capacity, DRAM Frequency, FSB:DRAM, Gear Mode, and channel mode.

LEFT

Primary and major secondary timings, including tRFC and tFAW.

RIGHT

tREFI, tCKE, sg/dg/dr/dd transitions, and other BIOS-trained values.

IMPORTANT

Zeros indicate an inapplicable 1R/1DPC path for a 2x24 GB 1R configuration.

WINDOWS 11 CAVEAT

Memory Integrity/Core Isolation may block the utility's driver. I do not recommend disabling security specifically to capture a timing screenshot: if the program does not launch, use the BIOS, CPU-Z, and HWiNFO.

WTR calculations depend on the utility version; DDR4/DDR5 formulas and corrections are compared in 3.8.

DOCUMENTATION REVIEWED: Official ASRock Timing Configurator 4.1.7 CDN and ASRock FAQ 505. Screenshot: my system.

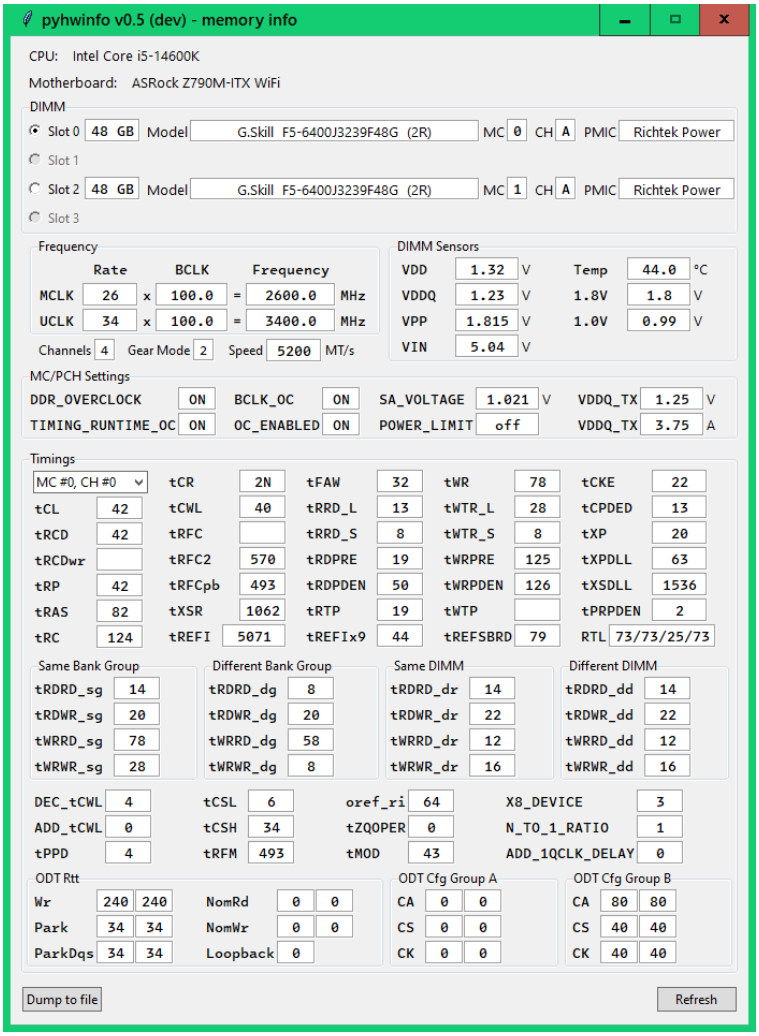
8.6 pyhwinfo

pyhwinfo 0.8 dev is a low-level diagnostic utility for DDR5 overclocking. It reads applied memory and IMC parameters that ordinary monitoring shows only partially or not at all.

WHAT IT LETS YOU CHECK

MCLK / UCLK / BCLK (interface fields), memory data rate, and Gear Mode; primary / secondary / tertiary timings by channel and MC0/MC1; RTL; ODT (Wr, Park, ParkDqs, NomRd, NomWr, and others); Vref; SA VID, VDDQ TX, AC_LL / DC_LL; DIMM, SPD / PMIC, and available module voltages and temperatures.

After Memory Training, it lets you compare BIOS settings with the values actually applied. Checking AUTO, tertiary/turnaround timings, RTL, ODT, and Vref is especially useful because the platform calculates them during training.



pyhwinfo: low-level DDR5 and memory-controller parameters

Screenshot shows v0.5 (dev): MC/PCH Settings section; separate Vref and AC_LL/DC_LL values are not shown here.

> **COMPATIBILITY LIMITATIONS**
>
> Supported systems use Windows 7 or later, Intel Core 12th/13th/14th/15th generations and DDR5. AMD and DDR4 support is not claimed. The project is in development: platforms, fields, and the interface may change. Low-level values require an understanding of DDR5/IMC; their purposes are covered in the relevant chapters.

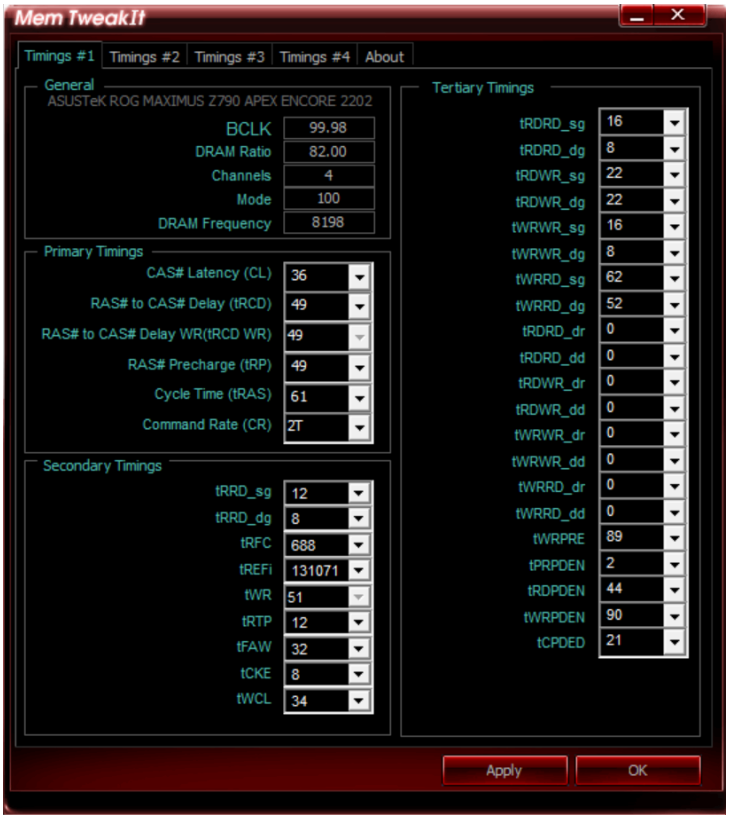
SOURCES: pyhwinfo README and source code (September 11, 2026); OCN — link to the dedicated discussion. GitHub — pyhwinfo / remittor OCN — pyhwinfo: open-source tool for showing memory timings

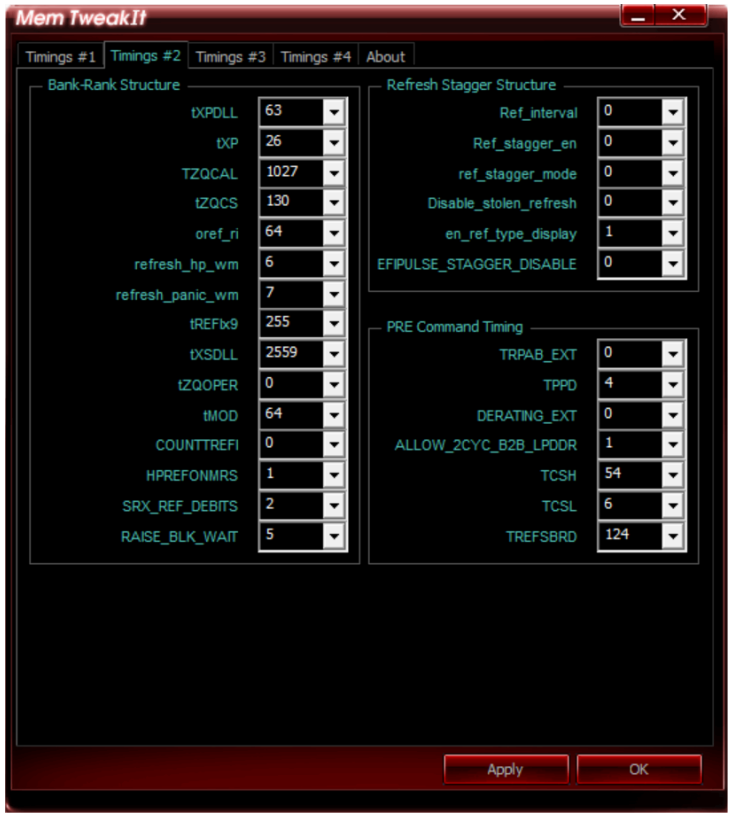
8.7 ASUS MemTweakIt

ASUS MemTweakIt shows more internal parameters than ASRock Timing Configurator (ATC). On my Z790 Apex Encore, four tabs collect the primary, secondary, and tertiary timings, refresh behavior, scheduler, and RTL. In this manual, I use it to capture a detailed record of settings.

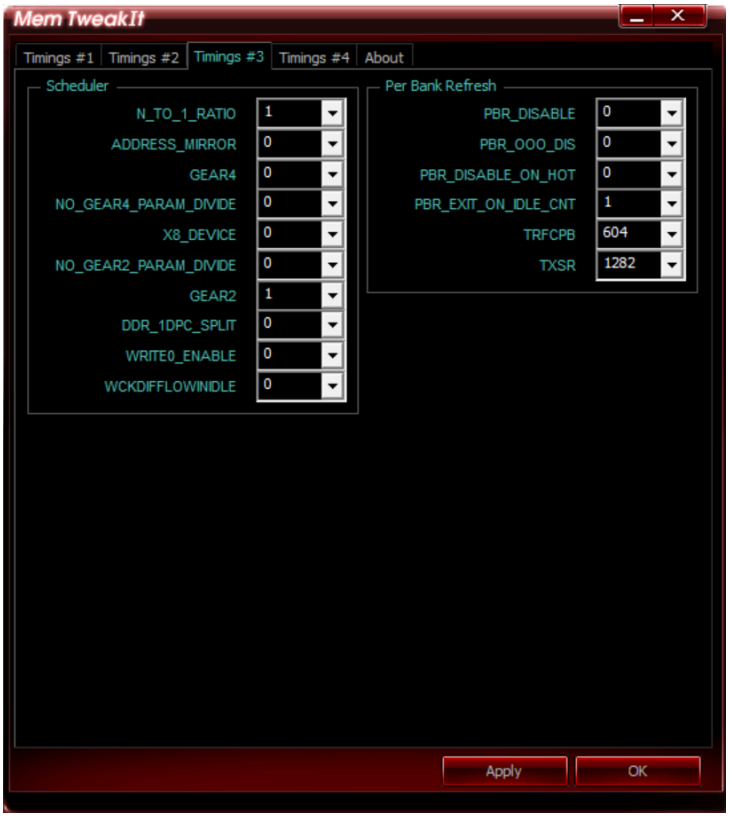
FOUR PAGES OF ONE DDR5-8200 CONFIGURATION

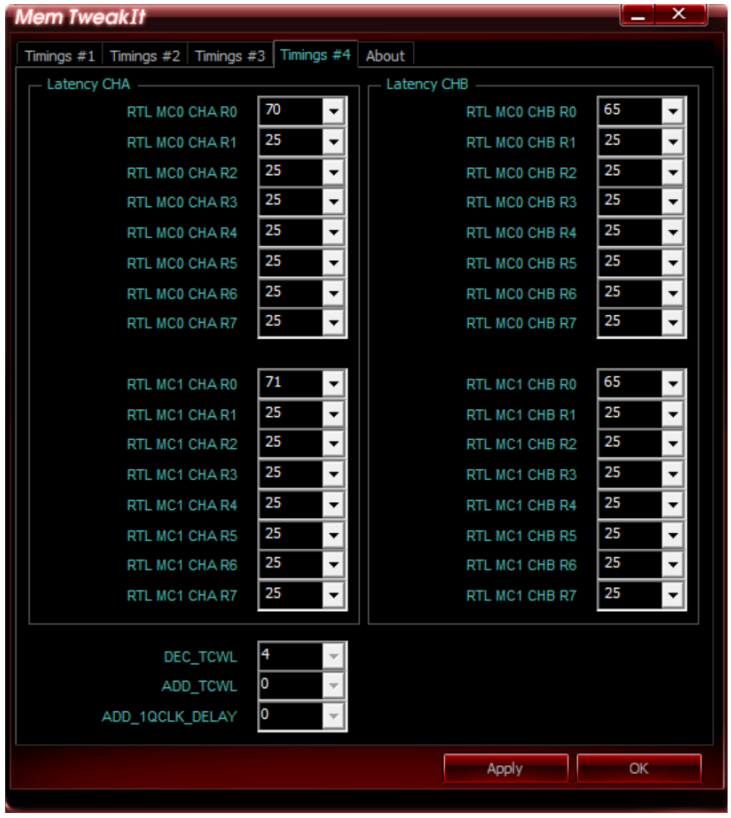
TIMINGS #1 / PRIMARY TIMINGS #2 / REFRESH





TIMINGS #3 / SCHEDULER TIMINGS #4 / RTL





CHANGING TIMINGS FROM WINDOWS

Even when the fields are active, I use MemTweakIt only for reading and screenshots. Writing can crash the system instantly, and some values depend on the BIOS version and the utility itself. The current build comes from the community; it is absent from the official ASUS catalog. Verify the archive before running it.

WR calculations depend on the MemTweakIt version; the old and DDR5 formulas are compared in chapter 11.

DOCUMENTATION REVIEWED: ASUS MemTweakIt manuals; HWBOT Z790 Apex community build and discussion. Screenshots: my system.

8.8 Additional performance tests

AIDA64 is usefully supplemented with one independent synthetic test and one real-world test. Results from different programs cannot be converted into one another: each uses its own working set and algorithm.

Tool	What it measures	When useful	Limitation
Intel MLC 3.13	Bandwidth and latency under increasing load	In-depth IMC and memory analysis	CLI; record launch parameters
OCCT 17.1.10	Latency & Bandwidth L1/L2/L3/RAM	Modern graphical alternative to AIDA64	Compare OCCT only with OCCT
7-Zip 26.05	Compression/ Decompression LZMA	Real-world response of CPU, cache, and RAM	Same dictionary and thread count
Cinebench 2026	Redshift scene rendering on the CPU	CPU score; tight timings sometimes add a few points	Measures CPU performance; the effect of memory tuning may fall within run-to-run variation.
CapFrameX / PresentMon	Frame time, average FPS, and low percentiles	Benefit in a CPU-limited game	A GPU limit hides the effect
RTP Benchmark	Read/Write/Copy and random-access latency	An additional data point within RAM Test Pro	Methodology still developing

8.9 Measurement protocol

Step	Action	What to record
1	Prepare an identical environment	BIOS, Windows, program versions, power, background activity, and cooling
2	Record the configuration	CPU-Z Memory/SPD and an ASRock Timing Configurator screenshot
3	Open HWiNFO Sensors	SPD Hub, VDD/VDDQ, WHEA, CPU/Ring, and throttling
4	Run five passes	Same test order, pauses, working set, and warm-up
5	Calculate the median and spread	Compare medians while accounting for run-to-run variation; do not count a small difference as a gain
6	Confirm with a workload	7-Zip, Cinebench, or a game; Chapter 07 searches for errors separately

MINIMUM REASONABLE TOOL SET

CPU-Z and Timing Configurator record the settings, HWiNFO records the conditions, AIDA64 provides the familiar synthetic test, MLC or OCCT provides an independent data point, and 7-Zip, Cinebench, or a CPU-limited game shows the practical effect.

DOCUMENTATION REVIEWED: Intel MLC 3.13; OCCT 17.1.10; 7-Zip 26.05; Cinebench 2026; CapFrameX; Intel PresentMon; RAM Test Pro: benchmark documentation.

09 / Programs: sources and downloads

Software links for chapters 07 and 08. Click a title to open its link. Links and versions checked on 27.10.2026.

y-cruncher § 7.2

Windows and Linux; free. The direct link below is the Windows 0.8.7.9547b archive.

Official website · **Windows archive** · **Help / FAQ**

Karhu RAM Test § 7.3

Karhu RAM Test 1.1.0.0; Windows; paid licence. The developer sends the distribution link after purchase.

Site / purchase · **README guide**

TestMem5 (TM5) § 7.4

TestMem5 0.13.1; Windows; free. CoolCmd branch; the archive includes the program and test configurations.

CoolCmd repository · **Latest 7z archive** · **README instructions**

MemTest86 § 7.5

MemTest86 11.7 Build 1000. Boots from a USB drive in UEFI mode. A free edition is available; the Pro distribution is supplied after purchase.

Official website · **Downloads** · **Free archive** · **PDF guide**

RAM Test Pro / RTP Benchmark § 7.6 / 8.8

PCSTONKS; free memory test and built-in benchmark. Windows 1.5.0 archive.

Website and guide · **Windows archive**

OCCT Personal § 7.7 / 8.8

OCCT 17.1.10; Windows and Linux. Personal and paid-edition terms are on the website.

Official website · **Downloads** · **Windows Stable** · **Guide**

HCI MemTest § 7.7

HCI MemTest 7.0; Windows. A free version is available for home/non-commercial use, along with the paid Pro edition.

Official website · **Free archive** · **Guide**

Monitoring · HWiNFO § 7.9 / 8.4

HWiNFO 8.54 (stable): sensors and logging. HWiNFO64 is free for non-commercial use.

Official website · **Downloads** · **EXE installer** · **Portable ZIP**

AIDA64 Extreme § 8.2

Version 8.40.5000; Read/Write/Copy and latency; limited 30-day trial.

Site / downloads · **EXE Windows** · **ZIP Portable** · **Guide**

CPU-Z / Validator § 8.3

CPU-Z 3.01: clocks, timings, SPD and configuration records.

Website and help · **EXE Windows** · **ZIP Windows** · **Validator V3** · **Validator: portal**

ASRock Timing Configurator 4.1.7 § 8.5

ASRock Timing Configurator 4.1.7; Windows; displays active timings. Official ASRock archive.

ASRock archive · **FAQ ASRock**

pyhwinfo § 8.6

Version 0.8 dev; Windows, Intel DDR5. In development; limitations are covered in 8.6.

Repository and instructions · **OCN thread** · **master branch ZIP**

ASUS MemTweakIt § 8.7

Timing viewer; the Z790 build is community-hosted.

Community build · **HWBOT thread** · **ASUS guide (Z390)**

Intel MLC § 8.8

Intel MLC 3.13: memory latency and bandwidth under load.

Intel downloads · **Description and commands**

7-Zip § 8.8

7-Zip 26.05: archiver and compression/decompression benchmark.

Downloads · **EXE Windows x64**

Cinebench § 8.8

Cinebench 2026: CPU/GPU rendering benchmark.

Downloads · **ZIP Windows x86-64** · **Description and requirements**

CapFrameX § 8.8

CapFrameX 1.9.1: frame times; requires .NET 10 Desktop Runtime x64.

Downloads · **Installer ZIP** · **Portable ZIP** · **Guide**

Intel PresentMon § 8.8

Intel PresentMon 2.6.0: frame-time capture; application and command-line versions.

Repository · **Release/downloads** · **MSI installer** · **Console EXE x64** · **Guide**

10 / OC reliability and repeatability

10.1 Memory cooling



Check stability at operating temperature once thermal conditions have stabilized. A successful test immediately after a boot after idle does not confirm memory stability an hour later, after the DIMMs, PMIC, case air, and area around the CPU have warmed up.

The SPD Hub sensor is useful, but it measures its own local temperature, not the hottest DRAM die. Some modules have no sensor at all. The trend for one kit and the temperature at the first error across repeated runs therefore matter more than a random number from someone else's screenshot.

WHAT TO RECORD DURING THE TEST

Metric	Why it is needed	How to interpret it
SPD Hub Temperature	SPD Hub temperature of each module where a sensor is available	Watch Current and Maximum; compare identical sensors on the same test bench
VDD / VDDQ and RPM	Links heat to voltage and actual airflow	Higher voltage may reduce thermal margin even if POST becomes easier
Time to first error	Helps check whether the error is related to warm-up	Repeat the same test with the same settings and different airflow
Case temperature	Distinguishes a cold test bench from a real scenario	Test the final profile in the normal closed case with heat from the GPU

THERMAL LOOP: RECORD THE ENTIRE CHAIN

AIR: room and case intake temperatures, plus heat from the GPU. →

DIMM / PMIC: module heating under load at the selected voltages. →

SPD HUB: an available reference point for monitoring temperature. →

FIRST ERROR: record the time, temperature and workload; the maximum sensor reading adds context.

PRACTICAL SEQUENCE

1. COLD BASELINE

Start the selected test and record the initial temperature, VDD/VDDQ, fan speed, and system background load.

2. STEADY-STATE WARM-UP

Wait for the temperature to plateau; an early successful pass does not confirm stability after warm-up. If DIMM Flex or another dynamic memory mode is enabled, record the actual operating frequency and timings at each temperature level.

3. REAL-WORLD WORST CASE

Repeat the workload in a closed case and, if typical for your use, with the graphics card warmed up.

4. DIAGNOSTIC AIRFLOW

With settings unchanged, direct airflow at the DIMMs. If the errors disappear, this indicates inadequate thermal margin, but it does not replace repeat testing.

PRACTICAL CONCLUSION

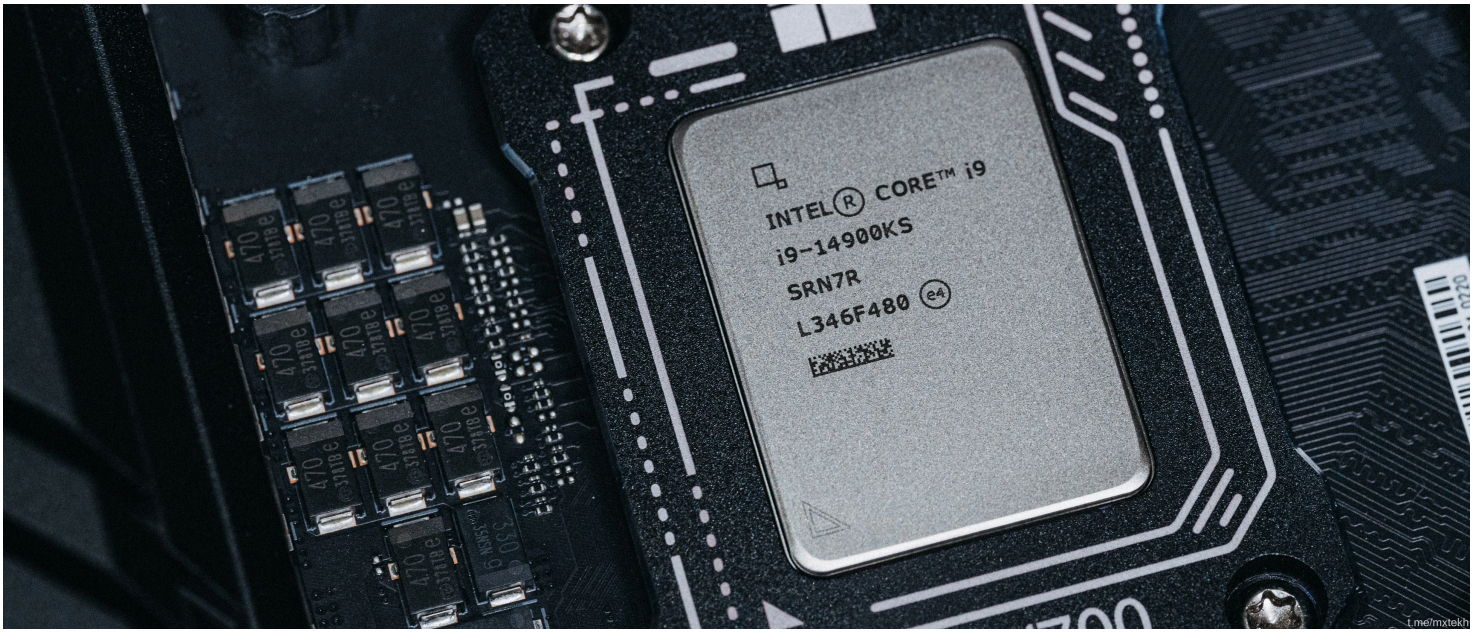
For high-frequency DDR5, directed airflow over the modules is part of the working configuration. If errors appear after warm-up, first check the effect of airflow. Then, if necessary, lower an excessively high tREFI; if tRFC was reduced, restore it to a previously verified value. Test one change at a time. Raising VDD/VDDQ without checking the effect of voltage may only increase heat.

PROFILE TEMPERATURE THRESHOLD

The threshold depends on the ICs, voltages, timings, DIMM construction, sensor and case. Determine thermal margin through repeated tests of your own profile. The documented 85 °C threshold applies to the operating conditions specified there; for overclocking, rely on the kit's actual stability after warm-up.

DOCUMENTATION REVIEWED: Micron DDR5 Key Module Features; Micron 16Gb DDR5 SDRAM datasheet; Renesas SPD5118; TEAMGROUP DDR5 specifications; ASUS DIMM Flex documentation.

10.2 CPU mounting and IMC potential



The IMC (Integrated Memory Controller) is located in the CPU, and its signals pass through the LGA contacts, motherboard traces, and DIMM slots. A missing channel, a sharp deterioration in training after remounting, or instability on one channel therefore calls first for mechanical diagnosis at JEDEC settings, not additional voltage.

A contact frame changes socket geometry and pressure distribution. It may affect temperature and contact, but it does not improve the IMC's intrinsic quality or guarantee a higher memory data rate.

SIGNAL PATH

CPU / IMC: the individual memory controller determines the starting margin. → **LGA CONTACTS:** seating, cleanliness and even mounting pressure. → **MOTHERBOARD:** topology, traces, BIOS and training. → **DIMM:** ICs, rank, SPD, voltage and temperature.

ISOLATE THE PROBLEM BEFORE TRYING TO FIX IT

Symptom	What to rule out	Action
A channel or DIMM is not detected	Module, slot, contamination, and socket contacts	One known-good DIMM in each recommended slot; then inspect the CPU and LGA
Training became worse after installing the cooler	Misalignment, tightening sequence, and tightening force	Return to the specified mounting procedure and retrain the memory completely
One channel is consistently weaker	Whether the error follows the module or the channel	Swap the DIMMs; repeat at JEDEC, then with the original profile
CPU temperature dropped after the frame was installed	Assuming an IMC improvement based on CPU temperature	Compare the maximum stable memory frequency and stability margin before and after installing the frame with the same settings

SAFE REINSTALLATION

1. JEDEC, THEN REMOVE POWER

Save the profile and test at JEDEC. Shut down the PC, switch off the power supply, and unplug the power cord; make sure standby power is gone.

2. INSPECT THE SEATING

Follow the motherboard's ESD instructions; hold the CPU and DIMMs by the edges. With the motherboard horizontal, place the CPU without sliding it or touching the LGA contacts.

3. FOLLOW ONE MANUAL

Tighten the cooler or frame only in the sequence and to the force specified by its manufacturer; do not transfer torque values from other hardware.

4. RETRAIN AND RETEST

After any remounting, clear the saved training results and repeat a power-cycled boot, a normal reboot, and the tests. Record the initial DIMM temperature separately: removing power does not mean the modules have already cooled down. As a rule, modules cool down slowly without direct airflow, especially 2R modules. For water-cooled modules, assess cooldown conditions separately.

HOW TO COMPARE IMC CAPABILITY

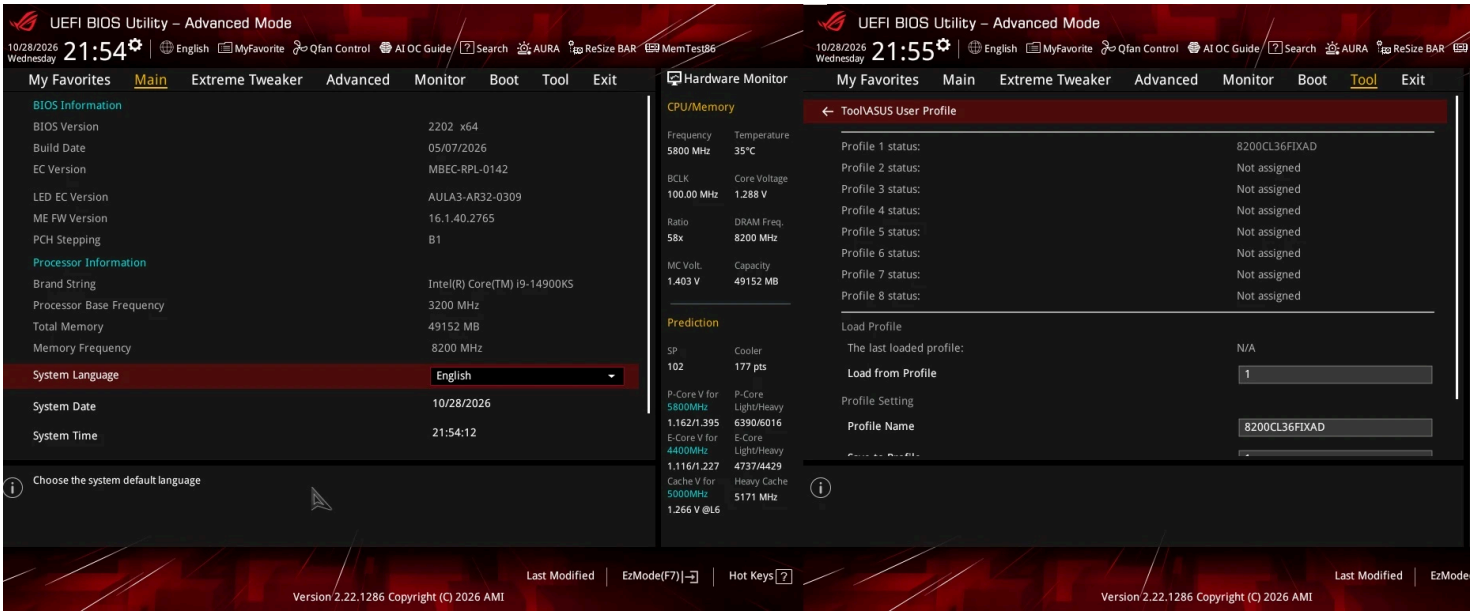
Even CPUs of the same model have different memory-controller headroom. Compare several training cycles on the same motherboard, with the same DIMMs and temperature. A random lucky POST and high SA are not measurements of IMC quality.

MOUNTING AND PRESSURE—FOLLOW THE MANUAL ONLY

LGA1700 and LGA1851 processors and sockets are incompatible, although cooler-mount geometry has been retained. Transfer contact frames, washers, and tightening torques only when supported by a component datasheet or manufacturer's manual.

DOCUMENTATION REVIEWED: Intel LGA1700/LGA1851 installation guidance; MSI DRAM LED troubleshooting; Noctua LGA1700/LGA1851 technical guides; cooler and frame manuals. **INTEL: LGA1700 INSTALLATION**, **INTEL: LGA1851 INSTALLATION**

10.3 BIOS and profile reproducibility



The BIOS version is part of the profile. An update may change MRC (Memory Reference Code, the memory-initialization code), CPU microcode, Intel ME, hidden Auto values, and Memory Fast Boot. Identical visible timings after a flash therefore do not guarantee the same training state. Memory Fast Boot concerns memory initialization in the BIOS; Windows Fast Startup is a separate OS startup mechanism.

For the Z790 Apex Encore, ASUS explicitly associates BIOS 2202 with the Intel IPU 2026.1 update and memory compatibility; ME changes at the same time, and its new version may remain after a BIOS rollback. Such a rollback does not always restore the previous software stack.

Stage	What to do	What to record
Before flashing	Screenshots and manual records of every changed setting	BIOS, ME/CSME, microcode, MRC/Silicon Init, Memory Fast Boot, and trained values
Safe baseline	Return to a stable profile or JEDEC before flashing	Control boot and absence of errors before the update
First boot	Reset to Defaults, JEDEC, and complete training	POST codes, training time, and values actually applied
Profile recovery	Enter settings manually; do not blindly load the old profile	Boot after idle, reboot, hot stress test, and sleep behavior
Comparison	Change only the BIOS while keeping hardware and conditions identical	If ME or microcode differs, mark the comparison as non-equivalent

> **NEW BIOS—NEW TEST PLATFORM**
>
> Use a profile from another version as a reference. After updating, repeat several boots after idle and normal reboots, and the set of checks in §7.9 “Error diagnosis”; verify stability after warm-up.

10.4 Data integrity

Unstable memory is dangerous for more than blue screens: an error can enter an archive, project, file system, or synchronized folder without any obvious warning. An experimental profile must not operate on the only copy of important data.

What to protect	Practical action	Verification
Important files	A 3-2-1 scheme, or at minimum a separate version on another medium/in the cloud	Open several files from the backup and know the restore procedure
OS and keys	Separate test installation/image; keep the BitLocker key off the test bench	Do not experiment in the only production environment
Firmware	Flash the BIOS only with known-stable memory and power	Before flashing, select a stable profile and perform the necessary retraining
Results	Store test logs, WHEA data, and settings outside a temporary folder	The last known-good point remains available after a failure

> **NO BENCHMARK IS WORTH DATA LOSS**
>
> Synchronization does not replace backups: if a file becomes corrupted, its corrupted version may spread to every device.

DOCUMENTATION REVIEWED: ASUS Z790 Apex Encore BIOS release notes and ROG Z790 BIOS Manual; Intel MRC/FSP; CISA Data Backup Options; Microsoft Windows Backup, BitLocker Recovery and WHEA. **ASUS: BIOS Z790 APEX ENCORE**

10.5 Real-world performance

AIDA64 and Intel MLC let you assess changes in memory bandwidth and latency, but their results do not directly indicate FPS gains, changes in frame time, or archiving speed. The real-world effect depends on the workload, CPU/GPU limit, working-set size, and background load.

THREE LEVELS OF MEASUREMENT

SYNTHETIC — AIDA64 / MLC:

bandwidth, latency and cache behavior.

APPLICATION TEST — 7-ZIP / CINEBENCH:

CPU, cache and memory working together in a specific algorithm.

REAL WORKLOAD — GAME OR PROJECT:

frame time, 1% low, operation time and result correctness.

Metric	What it shows	Main pitfall
Read / Write / Copy	Peak performance of the selected memory and cache path	The result depends on CPU/Ring frequencies, program version, and run conditions
Latency, ns	Synthetic end-to-end latency	Windows background activity, power state, and one lucky run can easily create a false win
Application score	Response of a specific algorithm to the entire platform	Does not let you attribute the entire gain to memory alone
1% low / frametime	Rare slow frames and smoothness in a CPU-limited scene	Different programs calculate percentiles differently; use one methodology and several repeats

RULE FOR A MEANINGFUL BENEFIT

First confirm the change in AIDA64/MLC, then in an application benchmark and a real-world scenario. Five runs under identical conditions, their median, and their spread are more reliable than a record score; in an A/B test, alternate profile order to reduce the effects of warm-up and background noise. Calculate P1 FPS as 1000 / P99 frame time (ms). Do not confuse this with the average FPS of the slowest 1% of frames.

10.6 Profile purposes

DAILY-USE PROFILE:

temperature and voltage margin, repeatable boots after idle, several tests and everyday work with data.

BENCHMARK PROFILE:

stability in a specific short task. Use an isolated environment and limit stability conclusions to that test.

SCREENSHOT PROFILE:

POST and a record of frequency and timings. Save the settings of the successful boot; check stability separately.

STATE THE PURPOSE OF THE PROFILE

Label the profile: daily, benchmark, or screenshot. Frequency without conditions, temperatures, BIOS version, and tests shows only that the system managed to boot and display those parameters.

HIERARCHY OF EVIDENCE

POST < Screenshot / Validation < Benchmark-stable-for-X < Daily-validated. Describe stability through the checks and operating conditions: “The profile passed the listed tests at the stated settings and temperatures.”

DOCUMENTATION REVIEWED: AIDA64; Intel MLC/XMP; PresentMon; CapFrameX metrics; CPU-Z Validator; HWBOT rules; 7-Zip; Maxon Cinebench 2026 technical information.

10.7 Four DIMMs and large capacities

Four modules, additional ranks, and higher electrical capacitance increase the load on the controller and signal path. Choose the configuration according to the required capacity: maximum frequency is a task for a 2-DIMM / 1SPC motherboard, while with four modules installed (2DPC), a QVL-tested configuration is preferable. Even that does not guarantee that all four modules will boot at the advertised frequency and timings. For 2DPC, target a frequency below the advertised figure to leave some margin.

Rank is determined by module organization, not by capacity alone. Two kits with the same gigabyte capacity can present different loads, so check the part number, rank count, and actual configuration of each DIMM.

Configuration	Priority	Practical conclusion
2 DIMM / 1DPC / 1R	Frequency and stability margin	Lowest load; best baseline for high-frequency overclocking
2 DIMM / 1DPC / 2R	Capacity without a second branch	More ranks may mean a lower frequency, but there is still only one DIMM per channel
4 DIMM / 2DPC / 1R	Capacity and availability	A second module per channel reduces electrical margin; two-DIMM XMP guarantees nothing
4 DIMM / 2DPC / 2R	Maximum capacity	Heaviest load; begin at JEDEC and raise the frequency gradually
CUDIMM	Clean CK clock signal	CKD restores CK, but does not train DQ/DQS or eliminate the load of four modules

ADVERTISED OVERCLOCKING DATA RATES FOR MSI Z790 GODLIKE MAX

For the MEG Z790 GODLIKE MAX, MSI lists overclocking data rates up to 7800+ MT/s for 1DPC1R, 6800+ MT/s for 1DPC2R, 6400+ MT/s for 2DPC1R, and 6000+ MT/s for 2DPC2R. These figures apply to one motherboard, but clearly show the stated ceiling dropping as load increases.

LARGE-CAPACITY TUNING SEQUENCE

1. CHOOSE THE CAPACITY IN ADVANCE

Buy the required capacity as one kit. Even the same part number may have a different IC revision if purchased later.

2. CHECK THE QVL

Match the exact part number, module count, capacity, BIOS, and recommended slots.

3. START AT JEDEC

Verify that every channel and module works before enabling XMP or manual voltages.

4. LOWER THE DATA RATE BEFORE ADJUSTING VOLTAGE

If XMP is not repeatable, lower the frequency by one or two steps, then find the minimum stable voltages.

5. TUNE TIMINGS AFTER FREQUENCY

First stabilize training and booting, then tighten the timings in small groups.

6. VALIDATE EVERY MODE

Several boots after idle and reboots, a hot memory test, and a normal workload.

> **CAPACITY FIRST, RECORDS SECOND**
>
> For a workstation, a stable 128–192 GB at a moderate speed is more valuable than an impressive POST. If maximum MT/s is the goal, choose a 2-DIMM / 1SPC motherboard and two suitably organized modules in advance.

DOCUMENTATION REVIEWED: MSI MEG Z790 GODLIKE MAX specifications; Intel 14th Gen desktop processor product brief; ASUS/MSI memory QVL; Micron DDR5 module documentation. **MSI: 1DPC / 2DPC MATRIX**

10.8 Profile documentation

To reproduce a profile, save its settings, test conditions and results. The materials must make it possible to reconstruct the test bench a month later and understand changes after a BIOS update, remount, or module replacement.

Material	What must be visible	Why
Platform record	CPU-Z CPU/Mainboard, BIOS, microcode, and Windows version	Distinguishes the profile from another firmware version and CPU sample
Memory + SPD	Frequency, Gear, primary timings, and every occupied SPD slot	Confirms the active mode and exact modules
Complete timings	ASRock Timing Configurator or MemTweakIt after boot	Shows the runtime values actually applied.
Sensors	HWiNFO Current/Minimum/Maximum: DIMM, VDD/VDDQ telemetry, CPU/Ring, WHEA	Records conditions, temperature, and logged WHEA events.
BIOS profile	File on USB plus screenshots of every changed page	The file may be incompatible with another version; screenshots remain readable
Tests and booting	Version, config, duration, result, boot after idle / reboot	Lets others repeat the test instead of merely trusting the word ‘stable’

> **THE FOLDER NAME IS ALSO PART OF THE PROTOCOL**
>
> Include the date, data rate, CL, BIOS version and profile purpose in the folder name. Example: 2026-09-03_8200_C36_BIOS2202_DAILY. Inside: BIOS, CPU-Z, SPD, timing tool, HWiNFO, test logs, and a short README with room temperature, airflow, and the latest change.

10.9 Evidence behind recommendations

Level	Basis	How we use it
A	Datasheet, Intel/JEDEC, manual, QVL, and release notes	Record what the manufacturer actually stated for the specific version
B	Repeatable A/B test on the described system	Practical conclusion with conditions, multiple runs, and original logs
C	Several independent community results	A starting point for a hypothesis; not a universal rule or substitute for your own testing
D	Single screenshot or retelling	Only a reason to investigate; without the platform and methodology, it is not used as evidence

REPRODUCIBILITY MATTERS MORE THAN A PERFECT SCREENSHOT

If a result cannot be reproduced from the saved conditions, it remains an observation. Revisions should distinguish specifications, my experience, conclusions from testing, and unconfirmed hypotheses.

DOCUMENTATION REVIEWED: ASUS ROG Z790 BIOS Manual; Microsoft WHEA documentation; vendor datasheets, manuals, QVL and BIOS release notes; reproducibility protocol of this manual. **ASUS USER PROFILE: LOAD / SAVE TO USB**

11 / Formulas

DDR5/BL16 without CRC. Examples: 8200 MT/s, CL36/CWL34. Timing values are in cycles and serve as overclocking guidelines.

PRIMARY TIMINGS

tCWL = tCL – 2 = 34; tCL, ns = tCL × 2000 / MT/s ≈ 8.78 ns.

tRAS = tRCD(RD) + tRTP - guideline for an early read; **tRC = tRAS + tRP**.

SECONDARY TIMINGS

tWR = 48 — the overclocking setting used in this manual; do not reduce it further.

tRTP = 12; do not go lower: this is the minimum MR6 code. At high data rates, stability may require **tRTP = 14**.

tRRD_L = tRRD_S + 2|4

tFAW, 1 KB (x8): 4 × tRRD_S = 4 × 8 = 32.

tFAW, 2 KB (x16): the greater of 4 × tRRD_S and 40 = 40 with RRD_S8.

tRFCpb ≈ tRFC – 30 × MT/s / 2000: at 8200, **688 – 123 = 565**. Hynix/FGR estimate, where tRFC means tRFC2; do not calculate this from tRFC1. **tRFC, cycles = tRFC, ns × MT/s / 2000**; round up. **I leave tRFCpb on Auto and do not tune it manually.**

TERTIARY TIMINGS: BASE CALCULATION AND UTILITY READOUTS

Parameter	DDR5 calculation*	Old DDR4-burst calculation
tWTR_L	= tWRRD_sg – tCWL – 10	= tWRRD_sg – tCWL – 6
tWTR_S	= tWRRD_dg – tCWL – 10	= tWRRD_dg – tCWL – 6
tWR	= tWRPRE – tCWL – 8	= tWRPRE – tCWL – 4

With CWL34/WRRD_dg52, the DDR5 calculation gives **8 and** the old **calculation gives 12**. Historically, ASRock had the WTR error and MemTweakIt the WR error; the result depends on the utility version. Details: Section 3.8.

*Read CWL from the controller. Corrections: **WR +1 with 2N**, **WTR –1** with a long write-signal ending. **S ↔ dg, L ↔ sg**; WTR refers to the write → read transition and is linked to WRRD. RDWR describes the reverse transition: read → write.

In reverse: **tWRRD = tCWL + 10 + tWTR***. With the same settings, WRRD +1 → WTR +1.

tRDRD_dg = tWRWR_dg = 8 - for DDR5/BL16, always leave these at **8** in the profile.

tWRWR_sg = 16 - the lowest effective value in my tests; lowering it further changes nothing. **My own research.**

ADDITIONAL TIMINGS: POWER AND REFRESH

tRDPDEN = tMRRPDEN = tCL + 8 + 1 = 45.

tWRPDEN = tWRAPDEN = tCWL + 8 + tWR + 1 = 34 + 8 + 48 + 1 = 91.

tACTPDEN = tPRPDEN = tREFPDEN = 2; tMRWPDEN = tMRD.

tXS = tRFC1; tXS_DLL = tDLLK for standard DDR5. Leave these parameters on Auto.

With **PD = 0** (Power Down Disabled), if the mode is actually disabled, **tCKE, tXP, and the PD-entry delays do not participate in this path**. **tCKE = 8 is a neutral setting; it does not improve performance. Auto** is also suitable.

For tXP with PD = 1, use the greater of 8 cycles and 7.5 ns: at 8200 MT/s, the minimum is **31** cycles. Sleep and self-refresh are separate modes.

OREF_RI = Auto; **0** removes the idle threshold for refresh; data refresh continues to operate. Test any gain.

tREFI = interval, µs × MT/s / 2; round down. At 8200 and up to 85 °C: normal mode 3.9 µs → 15 990; FGR 1.95 µs → 7995. Above 85 °C, halve the intervals.

Steps: 16 383 → 32 767 → 65 535 → 131 071 → 262 143. At 8200: **4.00 → 7.99 → 15.98 → 31.97 → 63.94 µs**. Field increment: 1; maximum **$2^{18} - 1$ (262 143)**. Use the maximum with active airflow or water cooling on the memory: stability depends strongly on temperature. Test with fully warmed memory.

RTL: ANTA777'S EMPIRICAL GUIDELINE

RTL ≈ MT/s / 800 + tCL + 19 = 8200 / 800 + 36 + 19 = 65.25. A guideline for assessing training; the values of each field in the RTL group are checked separately.

12 / Glossary

12.1 STANDARDS, PLATFORM, AND CONTROLLER

Basic terms for the standard and platform. The name column contains English names and expansions; the explanation column describes their meaning in DDR5 tuning.

Term	English name	Explanation
DDR5	Fifth-Generation Double Data Rate Synchronous Dynamic Random-Access Memory	The fifth generation of synchronous dynamic memory with data transfers on both clock edges.
SDRAM	Synchronous Dynamic Random-Access Memory	Dynamic memory whose operation is synchronized to a clock signal.
DRAM	Dynamic Random-Access Memory	Volatile memory: data is stored as charge in cell capacitors. Periodic refresh is required to retain data.
JEDEC	JEDEC Solid State Technology Association; formerly Joint Electron Device Engineering Council	A microelectronics standards organization that publishes standards for DDR5, SPD, and related components. Its current name is JEDEC Solid State Technology Association; Joint Electron Device Engineering Council is the historical expansion of the acronym.
JESD79-5	JEDEC Standard 79-5: DDR5 SDRAM	The primary DDR5 device standard; its letter and version number identify the revision.
MT/s	Megatransfers per Second	One million data transfers per second per DQ line. For example, DDR5-6400 transfers 6400 million bits per second on each line; total channel bandwidth also depends on channel width.
MHz	Megahertz	Megahertz: one million signal periods per second. For DDR5, the data rate in MT/s is twice the CK frequency in MHz: DDR5-6400 corresponds to a CK frequency of 3200 MHz.
fCK	Clock Frequency	The frequency of the external CK clock signal supplied to DRAM devices. It is distinct from the memory controller frequency and the internal DRAM clock domains.
QCLK	Memory Controller Clock	Intel memory-controller clock domain. In a confirmed Gear G mode, its period is tQCLK = G × 2000 / MT/s, in ns. Check the units used by the utility separately. See 5.7.
CPU	Central Processing Unit	Central processing unit; on LGA1700/LGA1851, it contains the memory controller.
Ring	Ring Interconnect	A ring interconnect linking cores, cache, and other CPU blocks on the LGA1700 platforms covered here. The memory controller (IMC) is a separate processor block.

Term	English name	Explanation
IMC	Integrated Memory Controller	Controller integrated into the CPU: accepts requests, schedules DRAM commands, and services memory channels.
MC	Memory Controller	Intel memory-controller block; MC0/MC1 are its indices. The MC/C labels in ATC are explained in 5.7. MC is also part of the MC/VDD2 BIOS name.
Intel ME	Intel Management Engine	Intel platform-management subsystem with its own firmware; ME in a BIOS/ME label refers to it.
MRC	Memory Reference Code	Intel code in the BIOS that initializes the memory controller (IMC) and physical interface (PHY) at boot and manages memory training.
FSP	Firmware Support Package	Intel package for platform initialization. Public FSP fields specify settings but do not expose the entire MRC algorithm.
PHY	Physical Layer	The physical interface layer, including transmitters, receivers, and circuitry for adjusting delays and calibrating signals.
BIOS	Basic Input/Output System	The common name for motherboard firmware and its settings menu. Modern motherboards generally use UEFI.
UEFI	Unified Extensible Firmware Interface	An interface between the operating system and platform firmware. MemTest86 also runs in the UEFI environment.
POST	Power-On Self-Test	Initial self-test after power-on; a successful POST still does not prove stability.
POR	Plan of Record	An Intel-supported operating mode for a specific number of DIMMs, ranks, and data rate.
SKU	Stock Keeping Unit	Inventory identifier for a product. One SKU does not guarantee the same DRAM ICs across every batch; check the hardware revision separately.
Microcode	Processor Microcode	Low-level code controlling some CPU operations. Updates can be loaded by BIOS/UEFI or the operating system and can change processor behavior.
LGA	Land Grid Array	An IC package type with contact pads. For LGA1700 and LGA1851 processors, the mating contacts are in the motherboard socket.
PCH	Platform Controller Hub	The platform chipset that handles peripherals. The memory controller (IMC) resides in the processor and has a separate role.

Term	English name	Explanation
QVL	Qualified Vendors List	A list of memory modules and kits tested by the motherboard or system manufacturer. The result applies to the specified part numbers, module count, and test conditions, including the CPU generation and BIOS version where stated.
OC	Overclocking	Operation beyond the stock operating conditions of a specific hardware configuration. Using XMP also counts as overclocking.
tQCLK	Memory Controller Clock Period	The duration of one QCLK memory-controller cycle. It can be calculated as tQCLK = Gear × tCK when that relationship is confirmed for the mode in use. Check the utility's readout units and scaling separately.
BCLK	Base Clock	A base reference clock from which operating frequencies are derived using multipliers. The frequencies tied to it depend on the platform.
RAM	Random-Access Memory	Working memory that holds data and programs in use by the system. The computers covered here use dynamic memory, DRAM, for this purpose.
LPDDR	Low-Power Double Data Rate	A family of dynamic memory designed for low power consumption. It has its own interface and tuning procedures; applicability of LPDDR descriptions to desktop DDR5 requires separate verification.
D2D	Die-to-Die	A connection that carries data between processor dies. On the Intel Core Ultra 200S platform covered here, the D2D frequency can be configured separately.
Uncore	Uncore	Processor components outside the compute cores, such as the memory controller, shared cache, and interconnects. Their composition and available settings depend on the architecture.
GPU	Graphics Processing Unit	A processor that handles graphics and other supported parallel computations. It may be integrated into the CPU or located on a separate graphics card.
Workstation	Workstation	A computer designed for professional work such as CAD, rendering or computation. System ECC support depends on the specific platform.

RTL/IOL ANALYSIS AND CALCULATION EXAMPLES — SECTION 5.7

DOCUMENTATION REVIEWED: Intel: Memory Controller, Microcode, FSP; JEDEC DDR5; Chapters 01-10, 14.

12.2 MODULE, ORGANIZATION, AND TOPOLOGY

Module formats, support ICs, and DRAM construction. Rank organization, package placement, and topology are covered below.

Term	English name	Explanation
DIMM	Dual In-line Memory Module	A memory module with electrically independent contacts on both sides of the PCB. Desktop DDR5 uses a full-size 288-pin DIMM; the compact format is designated SO-DIMM.
UDIMM	Unbuffered Dual In-line Memory Module	Ordinary unbuffered desktop module; commands reach DRAM without a register buffer.
SO-DIMM	Small Outline DIMM	Compact memory module for laptops and small systems; a standard DDR5 SO-DIMM has 262 contacts.
RDIMM	Registered DIMM	Module with a register that buffers commands, addresses, and the clock signal; used on compatible server platforms.
CUDIMM	Clocked Unbuffered Dual In-line Memory Module	UDIMM with a separate CKD driver that restores the clock signal.
CKD	Clock Driver	The clock driver on a CUDIMM: receives CK from the controller and generates output signals for DRAM. It uses phase locking in Single PLL and Dual PLL modes, and passes the clock around the PLL in Bypass mode.
RCD	Registering Clock Driver	A separate IC on an RDIMM that buffers commands, addresses, and the CK clock signal between the memory controller and the DRAM devices.
PMIC	Power Management Integrated Circuit	On-module controller generating VDD, VDDQ and VPP. Voltage range and control depend on the device model and configuration.
SPD	Serial Presence Detect	A data set stored in the module's nonvolatile memory: DRAM organization, supported JEDEC parameters, and module information. XMP/EXPO extensions may also be stored there. Reading SPD reveals the recorded capabilities and profiles; the current operating mode is checked separately.
SPD Hub	Serial Presence Detect Hub	A DDR5 support IC containing nonvolatile SPD memory and a bridge between the external I^2C/I^3C bus and local module devices, such as the PMIC. It may include a temperature sensor whose readings reflect the location of the SPD Hub.
EEPROM	Electrically Erasable Programmable Read-Only Memory	Rewritable nonvolatile memory in which SPD is stored.
XMP	Extreme Memory Profile	An Intel memory-overclocking profile specifying frequency, timings, and voltages.
EXPO	Extended Profiles for Overclocking	AMD memory-overclocking profile for a compatible platform. Profile support and operation of a particular kit depend on the CPU, motherboard, and BIOS.

Term	English name	Explanation
PCB	Printed Circuit Board	A printed circuit board. In this guide, PCB refers to the board of a memory module or motherboard; trace routing affects the signal.
IC	Integrated Circuit	Integrated circuit. In a module description, it often means the complete packaged device. The number of dies inside the package is a separate device characteristic.
Chip	Chip / Microchip	Colloquial name for a die or a complete DRAM device. When counting, clarify whether packages or dies are meant.
Package	IC Package	An IC package containing one or more dies and external contacts. In the DRAM packages discussed here, the substrate connects the dies to the contacts, and protective material covers the dies. Package counts refer to individual soldered components.
Substrate	Package Substrate	Small board inside a package: carries the die and connects it to the external contacts. Distinct from the module PCB.
FBGA	Fine-Pitch Ball Grid Array	A package with a fine-pitch array of solder balls underneath. Die count and rank organization are separate characteristics.
Die	Semiconductor Die	Piece of silicon on which the DRAM circuitry is fabricated: memory cells and control circuits.
Density	DRAM Die Density	The capacity of one DRAM die, usually specified in Gbit. It differs from the capacity of a finished module in GB and is used to determine the applicable refresh requirements.
SDP / DDP	Single-Die Package / Dual-Die Package	SDP is a single-die package; DDP contains two dies. Rank count depends on how the dies are organized and selected.
MMR	Hynix MMR (Device Designation)	A Hynix device designation from the RAMGuide example: two 4 Gbit MFR dies (a DRAM revision) in a DDP package. The designation describes the device; module rank organization is a separate property.
Low-loss	Low-Loss PCB Material	PCB material with low signal loss. The achievable memory data rate must be assessed for the specific configuration; the material property alone is insufficient to establish it.
Back-drilling	Back Drilling	Removal of unused plated via stubs to reduce signal reflections.

Term	English name	Explanation
RDL	Redistribution Layer	Layer that redistributes die contact pads. In the DRAM packages discussed here, moving pads toward the edges facilitates wire bonding.
Monolithic DDR5	Monolithic DDR5 SDRAM	DDR5 devices with one DRAM die per package, without a 3DS stack. The term describes the device construction. The number of devices and ranks on the DIMM is specified separately.
3DS / TSV	3D-Stacked DRAM / Through-Silicon Via	3DS is a stack of DRAM dies linked vertically by through-silicon vias (TSVs). DDP specifies two dies in a package; their interconnection method requires separate confirmation.
SS / DS	Single-Sided / Double-Sided	DRAM packages are soldered on one or both sides of the PCB. Package placement on the PCB sides and rank organization are separate module characteristics.
Rank	Memory Rank	Group of DRAM devices selected together by Chip Select; in DDR5, selection occurs by subchannel. Rank membership is determined by electrical organization; package placement on the PCB sides is described separately.
Rank Interleaving	Rank Interleaving	Alternating accesses between ranks: while one rank is busy with an internal operation, the controller can access another.
1R / 2R; R0 / R1	Single / Dual Rank; Rank 0 / Rank 1	1R denotes one rank on a module; 2R denotes two. R0 and R1 are rank numbers: a 1R module has R0, while a 2R module has R0 and R1.
x4 / x8 / x16	DRAM Device Data Width	The data interface width of an individual DRAM device: 4, 8, or 16 DQ lines. Die density, package count, and rank count are specified separately. See 2.7.
1Rx4 / 1Rx8 / 1Rx16 / 2Rx8	Rank Count and Device Width	Notation for rank count and DRAM device width. For example, 1Rx16 means one rank built from x16 devices; 2Rx8 means two ranks built from x8 devices. The number after x denotes the data interface width of one device.
Matched Kit	Factory-Matched Memory Kit	A memory kit whose modules have been tested together by the manufacturer.
Speed Bin	Speed Grade / Component Binning	A class assigned to memory ICs after selection for a specified operating mode. XMP specifies an overclocking profile; the limits of the particular memory must be determined separately.
Non-binary DDR5	Non-Binary-Density DDR5	DDR5 with a die density that is not a power of two; for example, 24 Gbit with typical module capacities of 24 and 48 GB.

Term	English name	Explanation
Channel	Memory Channel	Independent logical path between the IMC and memory.
Subchannel	Independent Memory Subchannel	One of two independent subchannels on a DDR5 DIMM, each carrying 32 data bits. System ECC adds check bits; their number depends on the module organization. Both subchannels belong to one CPU memory channel.
DPC / 1DPC / 2DPC	DIMMs Per Channel / One or Two DIMMs Per Channel	Number of modules actually installed per channel; a key measure of the current electrical load.
SPC / 1SPC / 2SPC	Slots Per Channel / One or Two Slots Per Channel	The number of slots physically routed per memory channel. This is a motherboard property; DPC describes the number of installed modules per channel.
true-1DPC	Community/Vendor Shorthand for True One-Slot-Per-Channel Topology	An informal name for a motherboard with one slot per channel. This guide uses SPC for the number of routed slots per channel and DPC for the number of installed modules per channel.
2-DIMM / 4-DIMM	Two / Four DIMM Slots	Motherboard slot count; 2-DIMM models are generally optimized for memory overclocking.
Point-to-point	Point-to-point Memory Topology	A connection from the controller to the only DIMM slot on each channel. At the slot level, this routing corresponds to 1SPC.
Daisy Chain	Daisy-Chain Memory Topology	Sequential routing of slots on a memory channel, generally preferred with one DIMM per channel.
T-topology	T-Topology Memory Routing	Branched routing with similar trace lengths to two slots, intended for 2SPC.
Gear	Memory Controller Gear Ratio	The IMC-to-DRAM clock ratio. G1 = 1:1, G2 = 1:2, G4 = 1:4. The Intel DDR5 platforms covered here use G2/G4; G1 is included for comparison with DDR4. See 2.2.
OEM / reference	Original Equipment Manufacturer / Reference Module	A supply category used in the catalog for desktop modules and reference products. IC type, rank organization and system ECC support are specified separately.
P/N / SKU	Part Number / Stock Keeping Unit	P/N is the manufacturer part number; SKU identifies a stock item. For a kit, keep the full code and suffix to distinguish capacity, profile and variant.
BOM	Bill of Materials	List of components making up a product. The manufacturer may change it between batches while retaining the product SKU.

Term	English name	Explanation
DRAM revision	DRAM Die Revision	A revision of a DRAM die. Labels such as A-die and M-die are meaningful together with the manufacturer, generation, and density. In this guide's notation, S32M denotes Samsung DDR5, 32 Gbit, and M-die; PCB revision and speed grade are specified separately.
Native JEDEC	Native JEDEC Speed Grade	The stock JEDEC speed grade of a component or module, without XMP/EXPO. For a finished module, check its specification and SPD: the speed grade of an individual die does not by itself establish the module's operating mode. The actual mode also depends on CPU and motherboard support and the memory configuration.

Package construction, rank organization, and component placement on the PCB sides are separate properties. The following entries cover DRAM width, channels, and slot routing.

DOCUMENTATION REVIEWED: JEDEC DDR5; AMD EXPO; module manufacturer documentation; Chapters 02, 14.

DOCUMENTATION REVIEWED: Micron: Monolithic RDIMM; Invensas: 3D Packaging; Chapters 02, 14.

12.3 Commands, buses, and signal paths

DDR5 commands operate on banks, rows, and columns. Bus names distinguish the paths used to carry commands, addresses, and data.

Term	English name	Explanation
Bank	Memory Bank	Independent array of rows and columns within DRAM.
Bank Group	Bank Group	Group of banks; transitions within one bank group and between different bank groups have different timings.
Row	Memory Row	Row of cells opened into the row buffer by an ACT command.
Row Buffer	DRAM Row Buffer	A bank buffer that holds data from the row opened by ACT. READ and WRITE access selected columns of that row; PRE closes it.
DRAM Page	DRAM Page / Page Size	The data in one bank row of an individual DRAM device. For the 16-Gbit devices covered in 2.7, the page size is 1 KB for x4/x8 and 2 KB for x16.
Column	Memory Column	Part of an open row accessed by read or write commands.
ACT	Activate	A command that opens the selected bank row before data access.
PRE	Precharge	A command that closes an open row and prepares the bank for the next activation.
PREab	Precharge All Banks	A command that closes open rows in every bank of the selected rank.

Term	English name	Explanation
PREpb / PREsb	Precharge Per Bank / Same Bank	The PREpb command closes the selected bank; PREsb closes the bank with the same number in every bank group of the selected logical rank.
RD	Read Command	Command that reads data from an open row.
WR	Write Command	Command that writes data to an open row.
CAS	Column Address Strobe	Historical name for the column-access phase; retained in the names of CL and CAS-to-CAS timings.
RAS	Row Address Strobe	Historical name for the row-access phase; retained in the names of ACT/PRE timings.
DQ	Data Input/Output	Bidirectional data lines: the memory controller is the transmitter during writes, and DRAM is the transmitter during reads.
DQS	Data Strobe	A differential data strobe. It travels with DQ and defines when the receiver captures the data.
CA	Command and Address	Command and address bus from the controller to the module.
CK	Clock	Primary differential memory clock signal.
CS / CS0 / CS1	Chip Select / Chip Select 0 / 1	A rank-select signal: CS0 corresponds to R0, and CS1 to R1. In DDR5, the select signals are independent for each subchannel.
CKE	Clock Enable (Legacy/Controller Term)	Historical and controller-side mode name; DDR5 has no separate CKE pin.
CMD / CTL	Command / Control	General labels for command and control signals.
MR / MRW / MRR	Mode Register / Mode Register Write / Read	MR is a DRAM mode register; MRW and MRR are commands for writing and reading these registers. They configure operating modes and provide device-defined information. SPD holds a separate set of module data.
WCK	Data Clock (LPDDR5)	A differential clock signal for the LPDDR5 data interface, used for both reads and writes. Desktop DDR5 has no separate WCK.
BL16	Burst Length 16	A burst of 16 data transfers; the baseline burst length for DDR5.
BC8	Burst Chop 8	A shortened burst of eight data transfers, half the length of BL16, used in supported scenarios.
Bus	Electrical Bus	A set of signal lines used to carry data, addresses, commands, or clock signals.
Turnaround	Bus Turnaround	Reversal of bus direction or change of bus target requiring a guard interval.

Term	English name	Explanation
RMW	Read-Modify-Write	An operation that reads a block, modifies part of it, and writes it back.

DOCUMENTATION REVIEWED: SK hynix DDR5 32Gb Rev.1.2: PRE/MR commands; Intel; Chapters 02-03.

12.4 Primary, secondary, and tertiary timings

The letter t means time. Main BIOS timing fields are usually in CK cycles; other fields may use different units. The same number of CK cycles represents a different time in nanoseconds at different memory data rates.

Term	English name	Explanation
Timing	Memory Timing	A parameter that specifies a memory delay, duration, or interval between events.
tCK	Clock Period	Duration of one physical clock cycle: tCK, ns = 2000 / MT/s.
tCL	CAS Latency	Latency from the READ command until the first data appears.
tRCDRD	Row-to-Column Delay for Read	The minimum interval from ACT to a READ command in the same bank.
tRCDWR	Row-to-Column Delay for Write	The minimum interval from ACT to a WRITE command in the same bank.
tRP	Row Precharge Time	The minimum interval from PRE to the next ACT in the same bank.
tRAS	Row Active Time	Minimum time for which a row remains open.
tRC	Row Cycle Time	Calculated row cycle time: tRC = tRAS + tRP. The actual ACT-to-ACT interval for the same bank can be longer because of the last READ/WRITE command. See 3.3.
CR / 1N / 2N / 3N	Command Rate / One-N / Two-N / Three-N	A setting for command issuance and command-cycle stretching (command stretch). The Z790 menu described here offers 1N/2N/3N; Z890 offers 1N/2N. Because of Gear, the CR number does not equal the duration of every DDR5 command. See 2.2.
N:1	N-to-One Command Stretch	A command-stretch mode covered here for Z790. Intel defines N valid command cycles in succession, then one gap; N = 1–7. ASUS describes N to 1 ratio as the number of gaps between cycles, so the number alone does not establish the tuning direction. See 2.2.
tCWL	CAS Write Latency	Latency from WRITE to the start of data transfer.
tWR	Write Recovery Time	Minimum interval from the end of a write data burst to PRE for the same bank.
tRTP	Read-to-Precharge Time	Minimum interval from a READ command to PRE for the same bank.

Term	English name	Explanation
tRRD_S / L	Row-to-Row Delay Short / Long	Interval between ACT commands: S for different bank groups, L for the same bank group.
tFAW	Four Activate Window	The minimum interval between the first and fifth ACT commands in one rank. The constraint applies to every sequence of five ACT commands.
tCCD_S / L	CAS-to-CAS Delay Short / Long	Interval between column commands: S for different bank groups, L for the same bank group.
tCCD_L_WR	Long CAS-to-CAS Write Delay	The WR → WR interval within one bank group when the second WRITE requires Read-Modify-Write.
tCCD_L_WR2	Long CAS-to-CAS Write Delay 2	A shortened WR → WR interval within one bank group when the second WRITE does not require Read-Modify-Write.
tWTR_S / L	Write-to-Read Delay Short / Long	Interval from the end of a write data burst to READ: S for a different bank group, L for the same one.
tRDRD	Read-to-Read Delay	A family of tertiary timings that specify intervals between two reads.
tWRWR	Write-to-Write Delay	A family of tertiary timings that specify intervals between two writes.
tRDWR	Read-to-Write Delay	A family of minimum intervals from a READ command to a WRITE command; the variant depends on the bank group, rank, and module.
tWRRD	Write-to-Read Delay	A family of minimum intervals from a WRITE command to a READ command; the variant depends on the bank group, rank, and module.
S / L	Short / Long	Suffixes for short and long timing variants. Their exact meaning depends on the timing family. Trace length is a separate property of the board routing.
sg / dg	Same Group / Different Group	Timing suffixes: sg means the same bank group; dg means a different bank group.
dr / dd	Different Rank / Different DIMM	Timing suffixes: dr means a different rank on the same DIMM; dd means a different DIMM on the same memory bus.
tRCD	Row-to-Column Delay	General term for the delay from the row-activation command ACT to a read or write command. tRCDRD applies to reads and tRCDWR to writes. How these values are linked depends on BIOS/MRC.

DOCUMENTATION REVIEWED: JEDEC DDR5, Intel and DRAM manufacturer documentation; Chapters 01-10, 14.

12.5 Refresh and maintenance intervals

Refresh restores cell charge. Higher tREFI means less frequent refresh; lower tRFC means shorter refresh pauses. Both reduce overhead but increase sensitivity to temperature and the retention capability of the specific ICs.

Term	English name	Explanation
Refresh	DRAM Refresh	Periodic restoration of charge in memory cells.
Retention	Data Retention	A cell's ability to retain data between refresh operations.
REFab	All-Bank Refresh	Refresh of the next portion of rows in all banks of the selected logical rank.
REFsb	Same-Bank Refresh	Refresh of the next portion of rows in same-numbered banks across all groups of the selected logical rank. In DDR5, it is used in FGR mode.
PBR	Per-Bank Refresh	Generic name for partial refresh. In Intel BIOS, Per Bank may refer to REFsb; it does not necessarily mean refreshing just one bank.
FGR	Fine Granularity Refresh	A DDR5 mode that halves the average interval between REFab operations and uses a shorter tRFC2; it also permits REFsb.
tREFI	Refresh Interval Time	The configured average interval between refresh operations. The maximum permitted value depends on the DRAM mode and temperature; increasing the interval reduces refresh frequency and the data-retention margin.
tRFC	Refresh Cycle Time	The refresh-cycle duration set by BIOS/MRC. A value in clock cycles is converted to nanoseconds using the current memory data rate.
tRFC1 / tRFC2	Refresh Cycle Time 1 / 2	Refresh-cycle time requirements for normal REFab and REFab in 2x FGR mode, respectively. The standard distinguishes these modes; the available settings depend on the BIOS implementation.
tRFCsb / tRFCpb	Same-Bank / Per-Bank Refresh Cycle Time	tRFCsb is the minimum time for REFsb to complete before the refreshed banks can be accessed again. tRFCpb is a controller field name; its correspondence to tRFCsb depends on the platform.
tREFIx9	Controller Refresh Deadline	The controller's limit on the interval between refresh operations for one rank. In the Intel registers covered here, it is measured in units of 1024 DCLK; the field name does not define a universal formula.

Term	English name	Explanation
Power Down	DRAM Power-Down State	A low-power state in which some DRAM input and output buffers are deactivated. For refresh, the memory must exit this state and receive commands from the controller.
Self Refresh	Self-Refresh Mode	A power-saving mode in which DRAM performs refresh itself using an internal timer. Power is maintained; the external clock signal may be stopped.
tCKE	Clock-Enable Timing (Controller Field)	Historical name of an Intel controller field specifying the minimum intervals for transitions from Power Down to the active state and back. DDR5 has no separate CKE pin.
tXP	Exit Power-Down Time	Delay from exiting Power Down until the next command.
tXS	Exit Self-Refresh Time	Delay when exiting Self Refresh.
tXS_DLL / tDLLK	Exit Self-Refresh DLL / DLL Locking Time	After Self Refresh, commands requiring the DLL must wait for it to be ready: tXS_DLL = tDLLK. This is a separate requirement from tXS.
tRDPDEN	Read-to-Power-Down Entry Delay	Interval from READ to entry into Power Down.
tWRPDEN	Write-to-Power-Down Entry Delay	Interval from WRITE to entry into Power Down.
tMRD / tMOD	Mode-Register Delay / Update Delay	Delays associated with DRAM mode-register commands and the application of register settings.
tMRR	Mode Register Read Command Period	The minimum interval between Mode Register Read (MRR) commands.
ZQ Calibration	Impedance Calibration against ZQ	Calibration of DRAM output-driver and on-die termination resistances against an external ZQ resistor.
tZQCSPeriod	ZQ Calibration Period (BIOS Field)	The repetition period of ZQ calibration, as labeled in the BIOS. The operation sequence and field units depend on the platform.
tZQOPER	ZQ Calibration Timing (BIOS Field)	A platform-specific delay field for ZQ calibration. Its relationship to the DDR5 tZQCAL and tZQLAT durations depends on the BIOS/MRC implementation.
RFM	Refresh Management	A mechanism for additional refresh under frequent activations. The ordinary refresh-cycle duration remains governed by tRFC.
tRFM	Refresh Management Cycle Time	The minimum duration of a Refresh Management (RFM) cycle.
tRPab	All-Bank Precharge Time	Interval after PREab. Check the controller-specific scope of the field; do not automatically substitute the tRP setting.

Term	English name	Explanation
tCA2CS	Command/Address-to-Chip-Select Delay	Internal interval between the CA path and CS selection.
Vendor fields	Controller/Vendor-Specific Timing Fields	Timing fields specific to a controller or motherboard vendor, such as tSR, tOSCO, and tXPDLL. Their meaning must be checked in the documentation. Keep Auto unless a specific tuning task requires changing them.

DOCUMENTATION REVIEWED: SK hynix DDR5 32Gb Rev.1.2: Mode Register Timing, Self Refresh; Intel; Chapter 03.

12.6 Voltages and power domains

The VDDQ name is used for different physical power rails. Record it together with the measurement source and platform.

Term	English name	Explanation
Rail	Power Rail	A separate supply line that delivers power to a particular block or group of circuits.
DRAM VDD	DRAM Core Supply Voltage	The supply voltage for the array and internal peripheral circuits of DRAM devices.
DRAM VDDQ	DRAM I/O Supply Voltage	The supply voltage for the I/O circuitry of DRAM devices, nominally 1.1 V for DDR5. This is a memory-side rail; CPU VDDQ TX supplies the transmitter on the processor side.
CPU VDDQ TX	CPU Transmit I/O Supply Voltage	The supply voltage for the memory-interface transmitter inside the CPU. DRAM VDDQ supplies the data interface on the module side.
MC VDD / VDD2	Memory-Controller I/O Supply Voltage	Platform-specific names for the supply voltage of the memory-controller (IMC) interface. In this context, both names refer to one power rail.
SA / VCCSA	System Agent Supply Voltage	The supply voltage for the Intel System Agent. The effect of adjusting it on achievable memory speed depends on the specific system.
VPP	DRAM Wordline Pump Supply Voltage	The supply voltage for DRAM row-activation circuitry, nominally about 1.8 V.
VDDIO	Input/Output Supply Voltage	A generic name for the supply voltage of a particular block's input/output circuitry.
VLDO	Low-Dropout-Regulator Output Voltage	The output voltage of a local linear regulator, for example inside an SPD Hub.
LDO	Low-Dropout Regulator	A linear regulator that needs only a small input-to-output voltage difference to maintain the specified output. The minimum permitted difference is called dropout; it depends on load current and operating conditions.

Term	English name	Explanation
IVR	Integrated Voltage Regulator	Integrated CPU voltage regulator.
PMIC Sync All	Synchronize All PMICs	A mode that applies common control settings to the PMICs of all installed memory modules.
Per-PMIC	Per-Power-Management-IC Control	Separate PMIC configuration for each module.
High DRAM Voltage	Extended DRAM-Voltage Range Mode	A mode that enables an extended VDD/VDDQ range on compatible PMICs. Voltage values are set separately.
VOUT	Voltage Output	The regulator's output voltage; in monitoring software, its telemetry reading.
VID	Voltage Identification	A voltage request code sent to the regulator, often displayed by a utility in volts. VID describes the request; the actual voltage at the measurement point also depends on the load, power delivery path, and regulator settings.
SVID	Serial Voltage Identification	Intel digital interface for power control and telemetry.
LLC	Load-Line Calibration	Compensation for voltage droop under load; aggressive LLC settings may cause voltage overshoot.
PLL	Phase-Locked Loop	A loop that synchronizes and recovers a signal's frequency and phase.
DLL	Delay-Locked Loop	Loop that aligns delays without synthesizing a new frequency.
TDDB	Time-Dependent Dielectric Breakdown	Time-dependent dielectric breakdown: insulation damage from prolonged electrical stress.
ppm	Parts Per Million	One millionth; 1 ppm = 1 in 1,000,000. In the TI chart, this is the calculated failure fraction.
TCASE	DRAM Package Case Temperature	DRAM package case temperature at the specified measurement point. The SPD Hub sensor measures temperature at a different point on the module; determining TCASE requires the corresponding measurement on the DRAM package.
VRM	Voltage Regulator Module	Power circuitry for the CPU or another hardware block. Phase count and power-stage ratings alone are insufficient to assess memory-overclocking capability.
PWM	Pulse-Width Modulation	Pulse-width modulation controls a signal by varying pulse duration. A PWM controller uses this principle to control the phases of a power converter.
SPS	Smart Power Stage	An integrated power stage with a driver and protection functions. The current rating applies to the individual stage; the current capability of the whole board must be assessed separately.

Term	English name	Explanation
PMIC5120	JEDEC PMIC5120	JEDEC PMIC class for client DDR5; Renesas RRG5332 is one example. PMIC class and silicon revision are separate characteristics.

DOCUMENTATION REVIEWED: JEDEC DDR5, Intel and DRAM manufacturer documentation; Chapters 01-10, 14.

12.7 TERMINATION AND SIGNAL INTEGRITY

ODT, driver resistance, and Vref define the electrical conditions for signal reception. Tuning selects values that preserve signal quality and operating margin in every bus state.

Term	English name	Explanation
ODT	On-Die Termination	Line termination using resistors integrated into the die. Active termination depends on transfer direction and rank state.
RTT	Termination Resistance	Designation for the resistance of on-die termination (ODT).
RTT_NOM	Nominal Termination Resistance	In DDR5, the nominal data termination resistance on a non-target rank when the controller activates NT ODT: RTT_NOM_RD during reads from another rank and RTT_NOM_WR during writes to another rank.
RTT_WR	Write Termination Resistance	The data termination resistance of the target rank during writes. In DDR5, it is controlled by commands and mode registers; DQS termination is configured separately.
RTT_PARK	Park Termination Resistance	The baseline DQ termination in the parked state. Its application is determined by commands and ODT-state priorities.
RON	Driver On-Resistance	Output resistance of the active transmitter.
PU / PD	Pull-Up / Pull-Down	Upper and lower parts of the driver or termination.
Vref	Reference Voltage	Reference voltage used to distinguish a logical zero from a logical one.
VrefDQ	Data Reference Voltage	Reference voltage for receiving DQ data signals.
VrefCA	Command/Address Reference Voltage	Reference voltage for receiving CA command/address signals.
VrefCS	Chip-Select Reference Voltage	Reference voltage for receiving the chip-select signal, CS. VrefCS, VrefCA, and VrefDQ apply to different signals; VrefCS can be adjusted when the platform provides a corresponding setting.
Drive Strength	Transmitter Drive Strength	The ability of an output stage to drive the electrical load on a signal line. Select the setting according to signal quality in the specific configuration.

Term	English name	Explanation
Power Training	DDR I/O Power Training	MRC stage that selects ODT, driver strength, and related buffer settings to reduce DDR I/O power while preserving operating margin.
Slew Rate	Signal Slew Rate	Rate at which the signal level changes during rising and falling transitions.
EQ	Equalization	Compensation for frequency-dependent channel loss and distortion.
CTLE	Continuous-Time Linear Equalizer	Continuous-time linear equalizer in the receiver.
DFE	Decision-Feedback Equalization	Distortion correction based on previously received symbols.
DCC	Duty-Cycle Correction	Duty-cycle correction for CK, DQS, DQ and other PHY signals.
DCA	Duty-Cycle Adjuster / Adjustment	Adjustment of the duty cycle of DRAM DQ and DQS output signals through mode registers.
PVT	Process, Voltage, Temperature	Variation in manufacturing process, voltage, and temperature accounted for during calibration.
Eye	Eye Diagram	An eye diagram superimposes many bit intervals of a signal. Its opening shows the timing and voltage margin at the selected measurement point. Put simply: the permissible timing and voltage ranges for correct signal reception.
Margin	Signal Margin	Signal margin to the onset of errors. Operating-system stability requires separate testing.
Crosstalk	Signal Crosstalk	Electromagnetic coupling between adjacent lines.
Tap	Delay Tap / Equalizer Tap	In a delay line, an individual tap or adjustment step; in DFE, a coefficient that corrects the contribution of one of the preceding symbols.
Bypass	Bypass Mode	Bypassing a circuit or a signal or power path. VccDLL Bypass reroutes power while the DLL remains active.

DOCUMENTATION REVIEWED: JEDEC DDR5, Intel and DRAM manufacturer documentation; Chapters 01-10, 14.

12.8 TRAINING, BOOT AND RECOVERY

Training selects delays, Vref, and compensation for the current boot. One successful POST may not be repeatable, so boots after idle and reboots must be checked.

Term	English name	Explanation
Memory Training	Memory Interface Training	Selection of delays, reference voltages (Vref), on-die termination (ODT), and memory-interface compensation.

Term	English name	Explanation
Auto	Automatic Firmware-Controlled Value	Mode in which BIOS/MRC automatically selects a parameter value. The selected value may differ from the standard or minimum value.
Trained Value	Value Determined by Training	A value obtained during memory-interface training. To speed up a boot, the firmware may reuse a saved result from previous training.
Full Training	Full Memory Training	The complete training cycle provided by BIOS/MRC for the current configuration. Its stages depend on the platform and settings.
Full Retrain	Full Memory Retraining	Another full training cycle after conditions change.
Cold Training	Training after a Cold Start	Memory training during a boot after power removal. Such a boot does not always run the full MRC cycle.
1D / 2D	One-/Two-Dimensional Training	A search for an operating point along one or two coordinates. In memory training, 1D may tune delay at a fixed Vref, while 2D may explore combinations of delay and Vref. The specific coordinates depend on the training stage.
RDTC2D	Read Timing Centering 2D	Switch for the two-dimensional read timing centering stage in Intel FSP and corresponding BIOS implementations. It controls whether that training stage runs; its exact use depends on the firmware.
Per-Bit	Per-Bit Training	Individual calibration of each DQ bit.
MPR	Multi-Purpose Register	In DDR4, MPR holds training patterns. In DDR5, these patterns are configured through mode registers (MRs).
WL	Write Leveling	Alignment of the write data strobe, DQS, relative to the clock signal, CK.
RTL	Round-Trip Latency	On Intel Alder Lake and Raptor Lake, this field represents the per-rank delay from a READ command to the first data at the memory controller, in QCLK units. The utility's display scale and conversion to nanoseconds require verification. See Section 5.7.
RTLA / RTLB	Round-Trip Latency A / B	RTL designations for sides A and B in the empirical formula in Section 5.7. Their mapping to MC/C rows in ATC must be checked for the specific display.
IOL	I/O Latency	A separate I/O delay parameter in the BIOS of some DDR4 platforms. Section 5.7 describes how the DDR5 parameters and access to them differ.
RTL Init	Round Trip Latency Initial Value	Initial value for the RTL search during training. The final value may differ from this starting value.
RTL Max	Round Trip Latency Maximum	Upper bound of the RTL search during training in ASUS BIOS. The final value may be below this bound.

Term	English name	Explanation
RTL Offset	Round Trip Latency Offset	RTL offset in ASUS BIOS, with the sign and magnitude set separately. Its behavior depends on the implementation; whether a reduction of 1–2 is appropriate must be checked for the specific firmware.
TAT	Turn-Around Timing	Timing intervals when changing the data-transfer direction or target on the bus.
RMT	Rank Margin Tool	An Intel tool for assessing timing and voltage margin of the memory interface for ranks and available signal groups. The results show the boundaries within which the built-in checks pass; everyday profile stability is verified with separate workloads.
Cold Boot	Cold Boot / Cold Start	Boot after shutdown; the state of standby power must be specified.
AC Cold Start	Cold Start after AC-Power Removal	Power-cycled boot after complete removal of external and standby power.
Warm Restart	Warm Boot / Warm Restart	Reboot without complete power removal. Warm in the firmware name denotes the type of startup; component temperature is considered separately.
S5	ACPI S5 Soft-Off State	ACPI soft-off state in which standby power may remain available.
MRC Fast Boot	Memory Reference Code Fast Boot	An accelerated Intel memory initialization path in which firmware may reuse saved training results and skip some training steps. The reuse conditions and the set of steps performed depend on the BIOS/MRC.
BIOS Fast Boot	Firmware Fast Boot	Mode that shortens POST. MRC Fast Boot separately controls shortened memory reinitialization.
Windows Fast Startup	Operating-System Fast Startup	Windows startup acceleration through hybrid shutdown: user sessions are closed, while the kernel and driver state is saved in the hibernation file and restored on the next boot. The Restart command initializes Windows anew regardless of Fast Startup.
No-POST	Failure to Complete POST	The system did not complete hardware initialization.
Recovery	Firmware Recovery Procedure	Return to bootable settings after a failed POST.
Clear CMOS	Clear CMOS Settings (CMOS: Complementary Metal-Oxide-Semiconductor)	Reset of saved BIOS settings; CMOS is a historical name here.
DIMM Fit	ASUS DIMM Fit	An ASUS feature that automatically tunes memory parameters for the current configuration and saves the result in the selected Store. Completed tuning produces a candidate operating profile; its stability is checked with separate tests.

Term	English name	Explanation
DIMM Fit Pro	ASUS DIMM Fit Pro	An extended ASUS DIMM Fit mode that lets users select parameters, ranges, and the number of automatic tuning passes, including available voltage settings. The result is saved in a Store and requires testing under load. The available options depend on the motherboard and BIOS.
Training Consistency	Memory-Training Consistency	Feature intended to improve memory-training repeatability. Stress testing is performed separately.
Memory Preset	Firmware Memory Preset	Manufacturer-prepared set of baseline memory settings.

RTL/IOL ANALYSIS AND CALCULATION EXAMPLES — SECTION 5.7

DOCUMENTATION REVIEWED: Intel FSP Raptor Lake-S: RDTC2D; ASUS BIOS manuals; Chapter 05.

BOOT AND REBOOT: AGREED TERMS

Boot — A normal system startup.

Boot after idle — A system startup after a period of inactivity.

Reboot — A normal system restart.

Power-cycled boot — A cold system startup after power has been completely removed.

Cold-system reboot — A reboot of a cold system that has not been warmed up by tests.

Warm-system reboot — A reboot of a hot system, after or during testing, with its components warmed up.

12.9 PROFILES, ERRORS, AND STABILITY

Stability is assessed under stated conditions. A successful POST, a benchmark pass, a screenshot, and validated daily operation provide different levels of evidence for a stability claim.

Term	English name	Explanation
Baseline	Baseline Configuration	Recorded starting configuration for a controlled comparison.
Profile	Saved Configuration Profile	Saved set of settings and operating conditions. Its stability must be established through separate testing.
Daily	Daily-Use Profile	A profile for everyday use, verified in selected tests and real workloads at expected temperatures. The test conditions, voltages, and tuning margin are recorded with the profile.
Benchmark profile	Benchmark-Stable Profile	Settings whose operation has been validated only by the specified benchmark.
Screenshot profile	Screenshot-Only Profile	Profile for capturing settings without full validation.
Safe JEDEC	Safe JEDEC Baseline	Backup stock profile for system recovery.

Term	English name	Explanation
Validation	Configuration Validation	Verification against specified conditions. In CPU-Z and HWBOT, the term also refers to registering settings or a result; stability requires separate testing.
Stability	Operational Stability	Absence of errors under the listed conditions and scenarios.
Pass	Successful Test Pass	Completed pass without logged errors.
Fail / Error	Test Failure / Detected Error	Test error or failure; the result requires diagnosis and does not count as a pass.
Coverage	Test Coverage Percentage	A counter of completed testing in a particular program, often expressed as a percentage. A value of 100% does not mean that all possible errors have been checked, and equal percentages in different programs do not represent equal amounts of testing.
Cycle	Test Cycle	One complete run through the algorithms of a particular test.
A/B Test	Controlled A/B Comparison	Comparison of two variants with one variable changed.
Sweet Spot	Optimal Operating Window	Best balance of results, temperature, voltage, and repeatability.
Hot Stability	Stability at Thermal Equilibrium	Stability after memory and system temperatures settle under load.
Thermal Margin	Temperature Margin	Margin to the temperature at which errors appear.
Pre-OS	Pre-Operating-System Environment	Environment before the operating system starts, such as MemTest86 running in UEFI.
System ECC	System-level Error-Correcting Code	Error correction performed by the CPU memory controller. A separate layer of correction typically used in server or workstation systems.
on-die ECC	On-Die Error-Correcting Code	Error correction inside a DRAM IC (chip). The IC stores its own check bits and corrects a single-bit error in its internal data block before returning it. This is a basic feature of all standard DDR5 memory, including ordinary desktop UDIMMs and CUDIMMs.
non-ECC	non-ECC Memory	In a module designation, this means the absence of system ECC. DDR5 modules of this type retain internal on-die ECC.
ECS	Error Check and Scrub	A separate scan of the DRAM array using on-die ECC, with corrected data written back. The counters refer to the ECS scan; reading them requires platform support.
Corrected ECC errors	Corrected ECC Error Events	Errors corrected by system ECC and logged by the platform.

Term	English name	Explanation
ECC injection	Error-Correcting Code Error Injection	Deliberate introduction of an error to verify system ECC operation on a supported platform.
WHEA	Windows Hardware Error Architecture	The Windows architecture for receiving and processing hardware error reports, including CPU, cache, memory, and PCIe errors. A WHEA entry requires analysis of its source; the absence of such entries does not confirm that RAM is error-free.
DMA	Direct Memory Access	Direct data transfer between a device and memory. Hardware carries out the transfer, freeing the processor from copying each data item.
NUMA	Non-Uniform Memory Access	A memory architecture in which access latency depends on where the memory is located relative to the processor accessing it.
CRC	Cyclic Redundancy Check	A cyclic redundancy code for detecting data corruption. DDR5 provides CRC mechanisms for interface transfers; their use depends on the operating mode and controller support.
Row disturbance / Row Hammer	Row-Disturbance Bit Flips / Row Hammer	Data errors in victim rows caused by repeated activations of aggressor rows. A particular scenario can involve multiple rows.
PPR	Post-Package Repair	Replacement of defective DRAM rows with spare rows. Soft PPR is temporary; the result of Hard PPR persists after power is removed.

DOCUMENTATION REVIEWED: SK hynix DDR5 32Gb Rev.1.2: ECS; test documentation; Chapters 07, 10.

12.10 TOOLS, WORKLOADS, AND METRICS

A stress test looks for errors. A benchmark measures how quickly a workload runs.

Term	English name	Explanation
Stress Test	Stress Test	A test that applies load to find errors. Performance is measured with a separate benchmark.
Component Stress	Component-Specific Stress Test	Algorithm that deliberately loads the CPU, IMC, or RAM.
y-cruncher	y-cruncher Component Stress Tester	Program with computational workloads for the CPU, memory controller, and RAM.
SVT	Small In-Cache VT3	Small VT3 variant with an in-cache working set. It primarily tests the CPU and cache while using a small amount of RAM.
VT3	Vector-Scalable Transform, Version 3	A demanding floating-point workload with a large data set that stresses the CPU, memory controller, and RAM. It replaces the obsolete VST.

Term	English name	Explanation
FFT	Fast Fourier Transform	Fast Fourier transform. In stress tests, it involves intensive floating-point computations and memory accesses.
NTT	Number-Theoretic Transform	A number-theoretic transform operates on integers using modular arithmetic. In y-cruncher, it is used for fast multiplication of large numbers.
AVX	Advanced Vector Extensions	Set of wide vector instructions for the CPU.
FPU	Floating-Point Unit	Compute unit for floating-point operations.
TM5	TestMem5	Memory-testing program for Windows with configurable test profiles.
Karhu	Karhu RAM Test	Program for testing an allocated amount of RAM in Windows. Its coverage metric reports the amount of testing completed.
MemTest86	PassMark MemTest86	UEFI memory test run before the operating system starts.
RAM Test Pro	PCSTONKS RAM Test Pro	Windows utility with configurable memory tests, error logging and WHEA monitoring.
OCCT	Historically: OverClock Checking Tool	Suite of platform stress tests and benchmarks; the product's current name is OCCT.
AIDA64	AIDA64 Cache & Memory Benchmark	Its Cache & Memory Benchmark measures data read, write, and copy speeds, along with memory-access latency.
MLC	Memory Latency Checker	Intel tool for measuring memory-access latency and bandwidth.
CPU-Z	CPU-Z	Program that displays CPU and motherboard information, active memory settings, and SPD data.
ATC	ASRock Timing Configurator	Utility for viewing memory timings and RTL; the set of fields depends on the platform and version. See 5.7.
HWiNFO	HWiNFO	Software for monitoring sensor readings, minimums, and maximums.
Benchmark	Performance Benchmark	A test that measures performance. Stability is assessed through separate validation tests.
Latency	Access Latency	The time between a request and a response. In a memory test, the overall latency includes time spent in the controller, queues, and access path.

Term	English name	Explanation
Bandwidth	Memory Bandwidth	Memory bandwidth, usually expressed in GB/s. The theoretical limit is calculated from the data rate and the total data-bus width; the measured value depends on the workload, timings, controller, and the share of accesses served by the cache.
Throughput	Sustained Throughput	Actual rate of data transfer or processing, including overhead.
GB/s / ns	Gigabytes per Second / Nanoseconds	GB/s means gigabytes per second, a bandwidth unit; ns means nanoseconds, a latency unit.
Median / P1 / P99	Median / First / Ninety-Ninth Percentile	The median is the 50th percentile: the central value of an ordered sample. P1 and P99 mark the boundaries of the lowest 1% and lowest 99% of values. The percentile calculation method, measured quantity, and direction of improvement are stated with the result.
FPS / 1% Low	Frames per Second / Slowest-One-Percent Frame Metric	FPS denotes the frame rate in frames per second. 1% Low characterizes rare slow frames; state its calculation method with the result.
Frametime	Frame Time / Frame Interval	Interval between consecutive frames or Present events; the precise meaning depends on the selected metric.
CPU-/GPU-limit	CPU-/GPU-Limited Workload	A situation in which performance is limited by the CPU or GPU. This affects how strongly RAM performance influences the result.
Throttling	Thermal/Power Throttling	Automatic frequency reduction due to temperature, current, or a power limit.
Gbit / GB	Gigabit / Gigabyte	Gbit means gigabit, and GB means gigabyte; one byte contains 8 bits. DRAM specifications traditionally also use Gb/GB for binary capacities: a 16 Gb die contains 2^{34} bits. The strict notation for 2^{30} bytes is GiB.
HCI MemTest	HCI MemTest	A RAM-testing program by HCI Design. The standard and Pro versions run in Windows and test memory available to the program; Deluxe includes a separate bootable version for CSM/legacy BIOS systems.
Large Pages	Large Pages	Memory pages larger than the standard page size. They map more memory with one address-translation entry and can reduce translation overhead.
RNG	Random Number Generator	A random or pseudorandom number generator. Memory tests use such sequences to generate test data.
Working set	Working set	For a test algorithm, the data it accesses while running. Keeping these data in the CPU cache reduces DRAM traffic. In Windows terminology, a process's working set is a different measure: its pageable memory currently resident in physical RAM.

Term	English name	Explanation
Paging	Paging	In this guide, transferring pages between RAM and a paging file on storage. Active paging during a memory test changes the workload and can slow the test considerably.

DOCUMENTATION REVIEWED: JEDEC DDR5, Intel and DRAM manufacturer documentation; Chapters 01-10, 14.

12.11 ADVANCED TRAINING ALGORITHMS

Terms used in the advanced analysis of memory training.

Term	English name	Explanation
RxVref	Receiver Reference Voltage	The CPU receiver's decision threshold during reads. It is adjusted separately from DRAM VrefDQ, which is used during writes.
DQS gating	DQS Receive Gating	Controls the DQS receive window so that the receiver opens for the expected start of a read transfer.
Deskew	Timing Deskew	Compensation for timing differences between signal lines. Per-bit deskew adjusts the timing of individual DQ bits separately.
FIFO	First In, First Out	A buffer that releases data in the order received. Receive-FIFO delays help align returning data with the memory controller.
PI	Phase Interpolator	A phase interpolator positions a signal edge between available clock phases.
LVR	Linear Voltage Regulator	A linear voltage regulator. In the Intel architecture discussed here, these regulators supply internal memory-PHY circuits.
LFSR	Linear Feedback Shift Register	A shift register with linear feedback that generates pseudorandom bit sequences used in training patterns.
Swizzle	DQ/DQS Swizzle	The mapping of logical DQ/DQS signals to physical routing, accounting for permitted signal permutations.
Address aliasing	Address Aliasing	Different logical addresses refer to the same physical memory location. An incorrectly described DRAM organization can cause this.
BDAT	BIOS Data ACPI Table	An interface for passing BIOS diagnostic data to software. The BDAT ACPI table points to a region containing data structures, which may include RMT results. The availability and content of these data depend on the firmware and enabled diagnostic features.

13 / Documentation consulted

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- ASUS ROG Z890 Series BIOS Manual E25061; ROG Maximus Z890 Apex specifications, QVL and BIOS notes; DIMM Fit, DIMM Fit Pro, Flex, Memory Gear and XMP documentation.
- MSI Intel 600/700/800 Series BIOS guides; MEG Z790 GODLIKE MAX specifications and QVL.
- ASRock Timing Configurator 4.1.7 and ASRock FAQ 505.
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- Micron DDR5 SDRAM Core Data Sheet, Rev. E (November 2024): commands, timing reference points, and CWL.
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- Samsung DDR5 x8/x16 component datasheets and timing tables; DDR4 8-Gbit B-die comparison material.
- Renesas SPD5108/SPD5118 datasheet R10DS0299EU0111 Rev. 1.11; RG5C172 CKD R10DO0011EU0100 Rev. 1.00; P8911 PMIC documentation.
- Kingston DDR5 overview, non-binary-memory FAQ and part-number information; G.SKILL, Corsair and TEAMGROUP product specifications.
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- Karhu RAM Test 1.1.0.0 documentation, README and developer guidance.
- CoolCmd TestMem5 0.13.1 documentation; community configurations by Serj, LMHz, anta777 and 1usmus.
- PassMark MemTest86 11.7 Build 1000 documentation.
- PCSTONKS RAM Test Pro 1.5.0 guide and release notes.
- OCCT 17.1.10 documentation and HCI Design MemTest 7 documentation.

Benchmarks and monitoring

- AIDA64 Extreme 8.40.5000 benchmark manuals.
- CPUID CPU-Z 3.01 and CPU-Z Validator V3 documentation.
- HWiNFO 8.54 documentation; Martin Malik: DDR5 PMIC telemetry and monitoring conflicts (2022-2026).
- Intel Memory Latency Checker 3.13; Intel PresentMon; CapFrameX documentation.
- 7-Zip 26.05, Cinebench 2026 and HWBOT benchmark rules.

TESTS AND MONITORING TOOLS (CONTINUED)

- ASUS MemTweakIt manuals and compatible community-build discussion.

DATA INTEGRITY AND OPERATION

- Microsoft Windows Hardware Error Architecture documentation.
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13.1 TRAINING ALGORITHMS: sources

Sources for Chapter 06: ASUS menus, the Intel FSP interface, and memory-interface training documentation.

- **ASUS ROG Z790 Series BIOS Manual — E21287** — Z790 training labels and available settings in the earlier manual.
- **ASUS ROG Z790 Series (Intel® 14th) BIOS Manual — E22758** — Z790 training labels, including Periodic DCC.
- **ASUS ROG Z890 Series BIOS Manual — E25061** — Z890 training labels and menu differences from Z790.
- **Intel FSP — RaptorLakeS / FspmUpd.h** — Raptor Lake-S training and diagnostic interface fields.
- **Intel FSP — ArrowLakeS IoT / FspmUpd.h** — Arrow Lake-S interface fields; not the full ASUS BIOS implementation.
- **Intel MRC — MrcCrosser.c (Tiger Lake)** — Historical source code for ODT, drive strength, equalization and compensation.
- **Intel MRC — MrcReadReceiveEnable.c (Ice Lake)** — Historical source code for Receive Enable, RTL and receive FIFO.
- **Intel MRC — MrcMemoryScrub.c (Tiger Lake)** — SPD-geometry checks and limitations of the historical Alias Test.
- **SK hynix 16Gb DDR5 SDRAM** — DDR5 training patterns, Vref, ODT, DFE/DCA and PPR.
- **8.4GTS LPDDR5x and 6.4GTS DDR5 Combo PHY — EPEPS 2025** — Intel authors' abstract: PI and LVR circuits in the Meteor Lake/Arrow Lake PHY.

> **REVISIONS AND ACCESS DATE**
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> Revision numbers and historical dates are preserved. Current downloads and links were checked on October 20, 2026. AIDA64 downloads have been updated to 8.40.5000; the Chapter 8 results refer to version 8.35, as stated there.